AN10853

ESD and EMC sensitivity of IC

Rev. 01 — 10 November 2010 **Application note**

Document information

Info	Content
Keywords	ESD, EMC
Abstract	This application note describes basics of the ESD and EMC sensitivity of IC

Revision history

Rev	Date	Description
01	20101110	initial release

Contact information

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1. Introduction

Integrated circuits are sensitive to electrostatic discharge (a sudden and short-time flow of currents) and electromagnetic fields (at which they can be source or victim of both of it).

This application note shall be understood as an introductive basic description of

- what electrostatic discharge is
- how sensitive devices can be protected against electrostatic discharges
- what electromagnetic compatibility means
- and how electromagnetic sensitivity can be tested.

But by no means, this application note does not substitute any of the corresponding engineering standards and standard operation procedures.

2. Electrostatic charging and discharging

ElectroStatic Discharge (ESD) is the transfer of an electrostatic charge between objects at different electrical potentials and occurs with direct contact or when induced by an electrostatic field. Many pins of NXP devices are protected against ESD up to a certain level defined in the Quality and Reliability Specification (Ref. 12 “NX2-00001”). However, we recommend that ESD precautions are complied with when handling such components.

2.1 Triboelectric charging and ESD events

Nearly all electrostatic discharges are caused by static or frictional electricity. This kind of electricity is produced due to triboelectric charging, which means, that two materials which came in contact with another are electrically charged while being separated (like through rubbing) (see Figure 1).

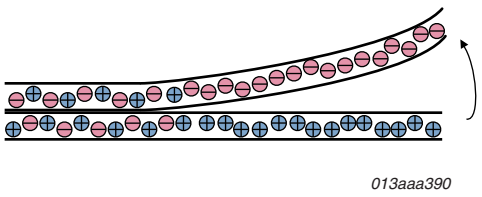

Fig 1. Triboelectric effect

This happens because the two materials being in contact with another are exchanging electrons (Figure 2) to equalize their electrochemical potential. When separated, some materials tend to give electrons away, whereas others tend to keep extra electrons. The result is that both materials are on different electrical potentials. Friction increases the possibility to exchange electrons because it enhances the contact surface of the two materials.

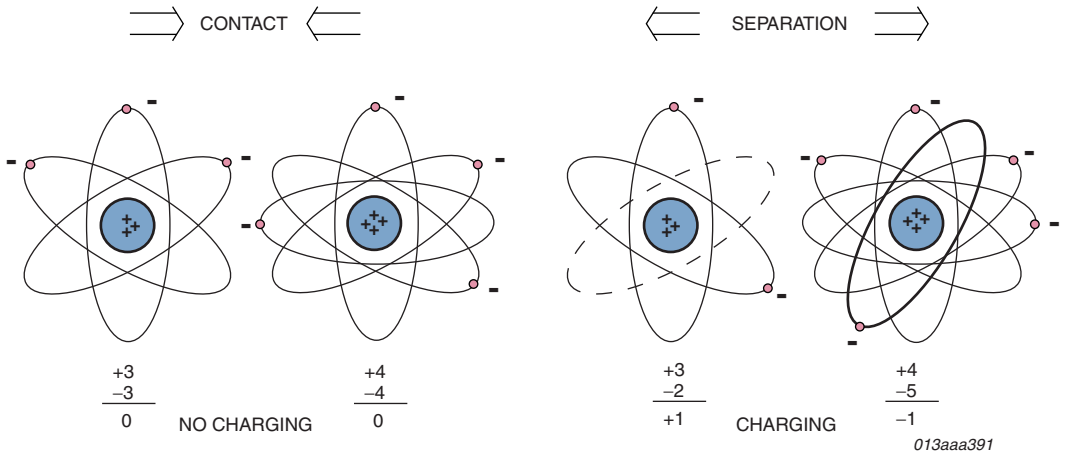

Fig 2. Exchange of electrons

The electrostatic attractive force of an electron and a proton seems to be marginal but it is about 40 orders of magnitude stronger compared to the gravitational force interacting between them.

Examples of triboelectric charging are:

- Walking on a rug
- Ascending from a fabric covered car seat
- Combing dry hair with a plastic comb
- Removing a plastic packing foil

An ESD event is the electrical discharge between two objects of different electrostatic potential,

- like in thunderstorms between the water droplets in the cloud and the earth (see Figure 3)
- touching a door handle after charging while walking on a rug (see Figure 4)
- during product assembling without sufficient ESD protection.

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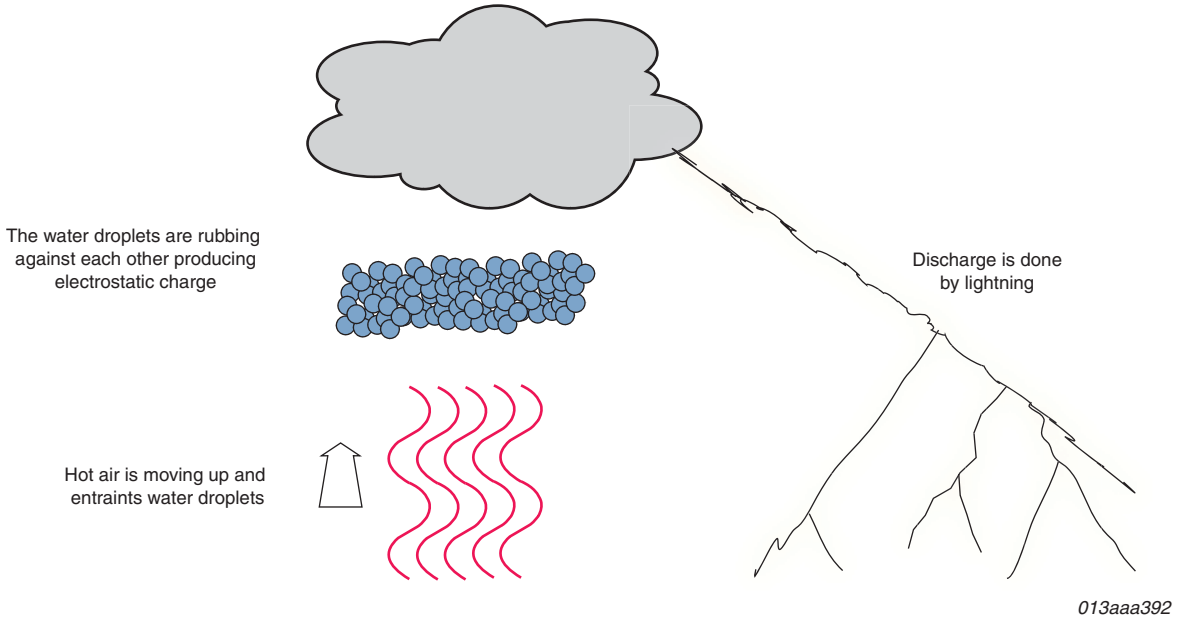

Fig 3. Electrostatic charging and discharging in a thunderstorm

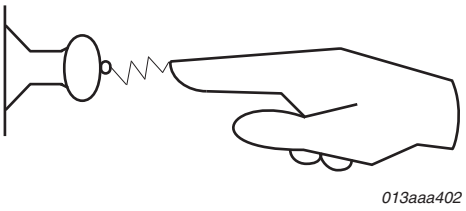

Fig 4. Electrostatic discharging of a human body

2.1.1 ESD order of magnitude

Electrostatic charges can be stored in many things; for example, man-made fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people (see Figure 5).

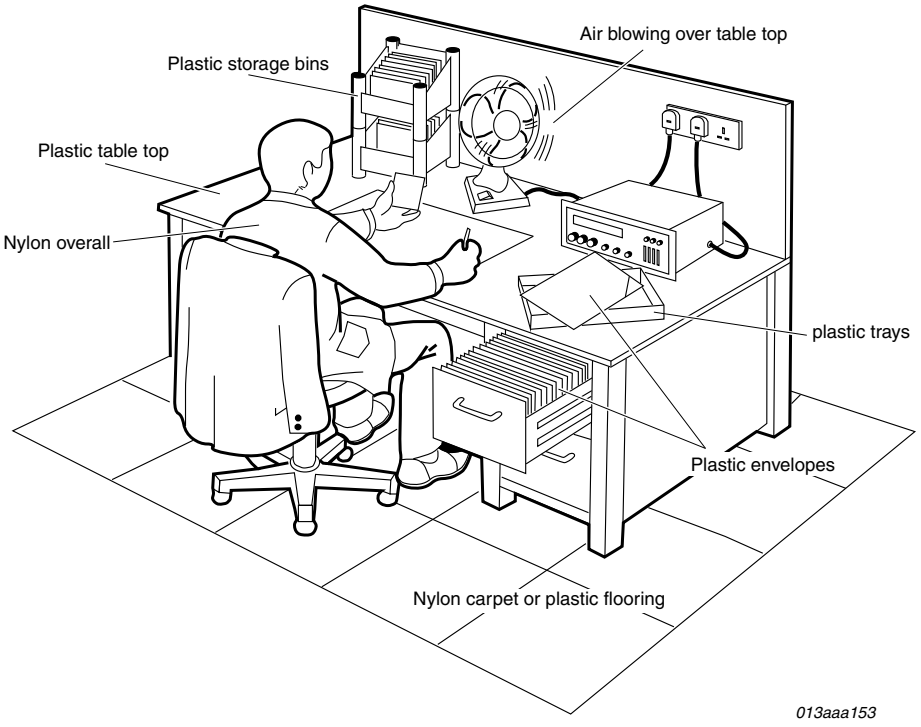

Fig 5. Dangerous environment for handling electronic components

The charges are caused by friction between two surfaces, where at least one is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force, and the humidity of surrounding air (see Table 1).

Table 1. Static generation

Means of static generation	Humidity		Unit
	10 % to 20 %	65 % to 90 %	
walking across carpet	35000	1500	V
walking over vinyl floor	12000	250	V
worker handling components at bench	6000	100	V
rubbing of vinyl sheet protectors	7000	600	V
lifting common poly bag from bench	20000	1200	V
sliding on chair padded with polyurethane foam	18000	1500	V

2.1.2 ESD sensitivity of ICs

The sensitivity of an IC depends to some extend on the product package:

- Packaged IC are very sensitive to ESD because they are single parts and peak effects can occur on the pins.
- Bare die and sawn wafer are less sensitive than packaged IC because they are single parts but charges are dissipated to the entire surface so peak effects on pins may not occur.

- Wafer are less sensitive than bare die and sawn wafer because charges are dissipated to the entire surface of the wafer and therefore affecting all IC in the same way. Peak effects on pins may not occur. Also, touching one single pin at packaged parts is much easier than on bare die.
- Due to the constantly shrinking IC process technology, the silicon die are becoming smaller and smaller. The smaller the geometry of the silicon die the lower is its ESD robustness. Figure 6 shows the size of the IC area which is needed to get a 2 kV HBM ESD protection compared to the chip size and the thickness of the gate oxide.

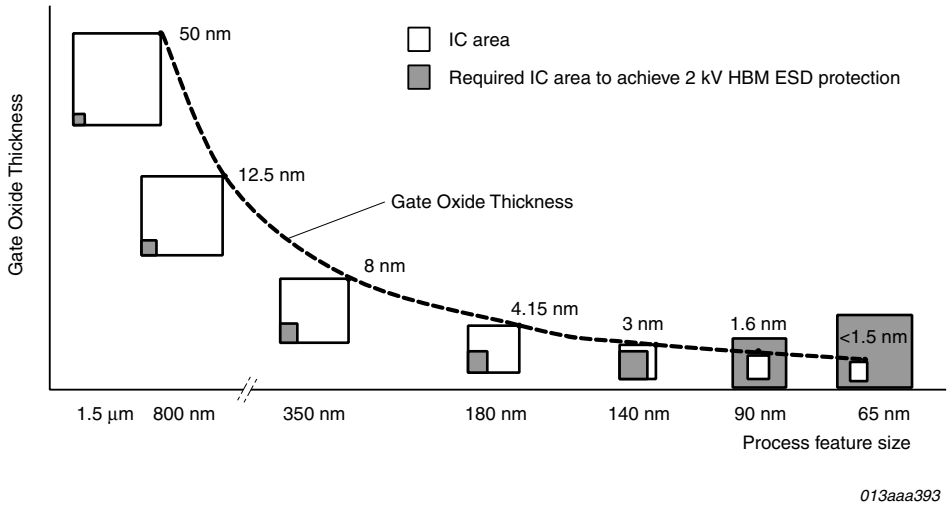

Fig 6. Required IC area to achieve 2 kV HBM ESD protection

2.2 ESD protection

2.2.1 Electrostatic Protected Area (EPA): work area for handling electrostatic-sensitive devices

Figure 7 shows a working area suitable for safely handling electrostatic-sensitive devices. The surface of the workbench is conductive and anti-static. The floor should also be covered with anti-static material.

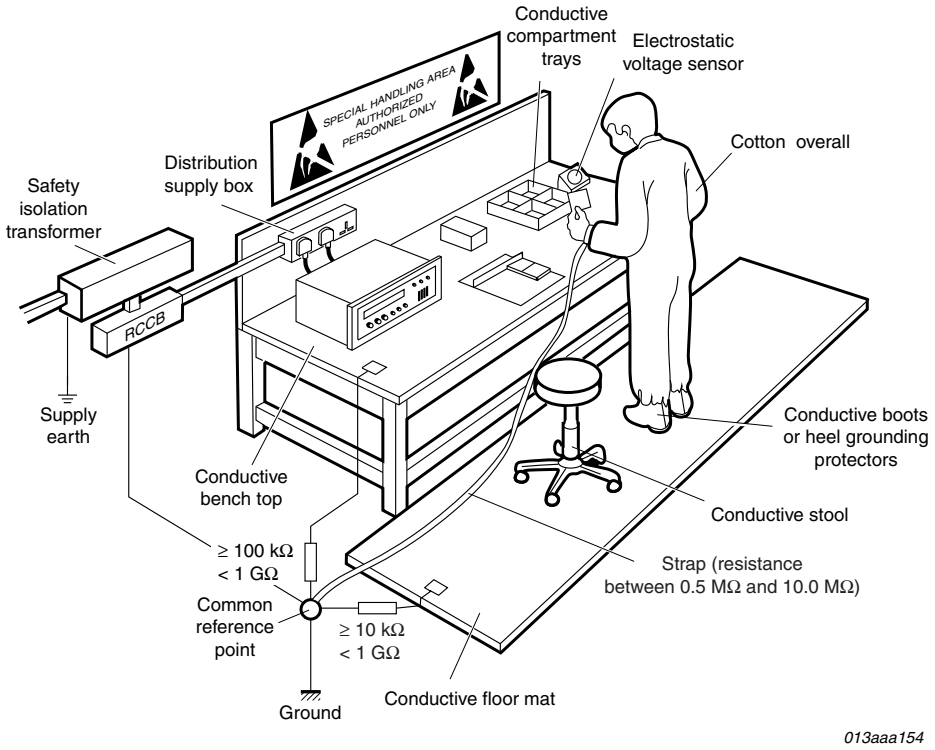

Fig 7. Essential features of an ESD-protected work area

The following precautions should be observed:

- At the entrance of an Electrostatic Protected Area (EPA) the electrostatic conductivity has to be checked (see Figure 8).

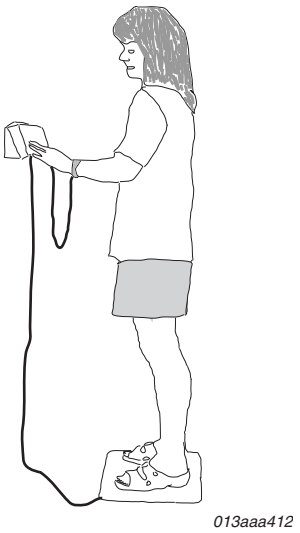

Fig 8. ESD entrance control

- Entrance and exit of an EPA has to be labeled with warning signs (see Figure 9).

a. Entering ESD protected area

b. Leaving ESD protected area

Fig 9. Warning signs of an Electrostatic Protected Area (EPA)

- People at a workbench should be earthed via a wrist straps and a resistor (see Figure 10).

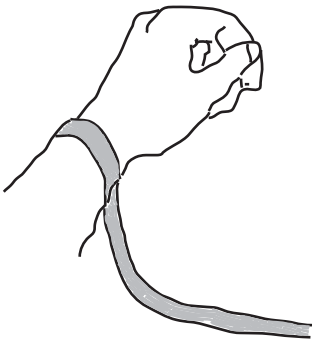

Fig 10. Wrist strap

- Use gloves, protective footwear, and cotton garment (see Figure 11).

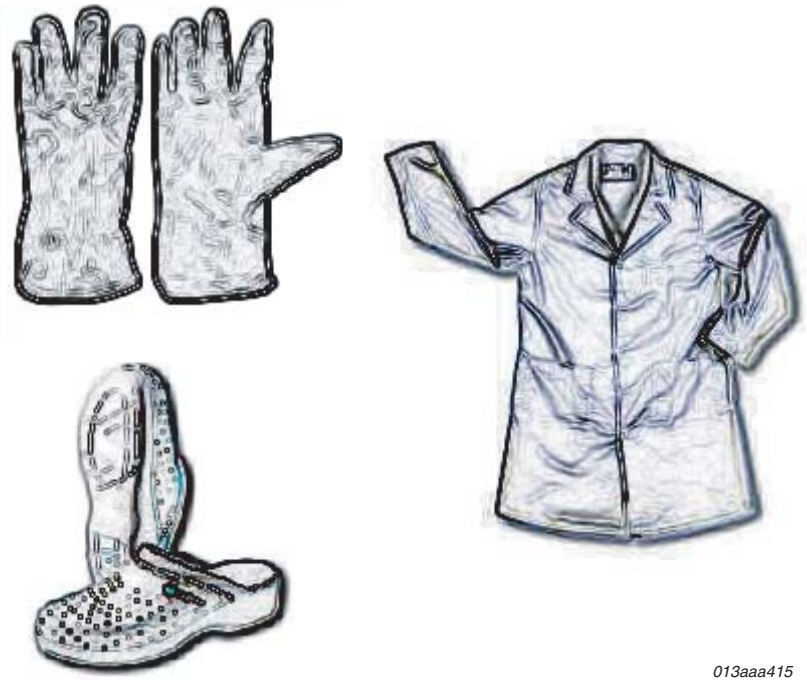

Fig 11. Protective clothes

- If needed, neutralized or reduced electrostatic fields to less than ±1000 V with an ionizer.
- All mains-powered equipment should be connected to the mains via an earth-leakage switch.
- Equipment cases should be grounded.
- Relative humidity should be maintained between 45 % and 60 %.

- Keep static materials, such as plastic envelopes and plastic trays etc., away from the workbench. If there are any static materials on the workbench, remove them before handling the semiconductor devices.
- Refer to the current version of Ref. 4 “IEC 61340-5”, that explains in more detail how to arrange an ESD protective area for handling ESD sensitive devices.

2.2.2 Receipt and storage of components

Electrostatic-sensitive devices are packed for dispatch in anti-static/conductive containers, usually boxes, tubes or blister tapes wrapped in a static shielding bag (see Figure 12 and Figure 13).

Fig 12. Bare die in ESD protected tray

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Fig 13. Static shielding bag

Warning labels on both primary and secondary packing show that the contents are sensitive to electrostatic discharge (see Figure 14 and Figure 15).

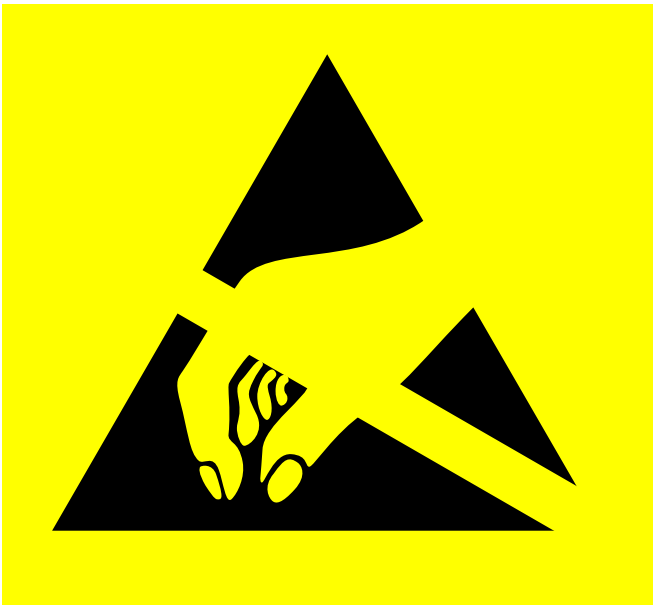

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Fig 14. Warning label for an electrostatic sensitive device, denoting that the device is susceptible to damage

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Fig 15. Typical warning label of ESD sensitive devices

Such devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be done at a protected working area. Any components that are stored temporarily should be packed in conductive or anti-static packing or carriers. The environment humidity must be controlled and has to be between 45 % and 60 % of relative humidity otherwise a ionizer must be used.

2.2.3 PCB assembly

Electrostatic-sensitive devices must be removed from their protective packing with grounded component-pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering, cleaning and drying processes. Do not remove more components from the storage packing than are needed at any one time. Production and assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken. During assembly, ensure that the electrostatic-sensitive devices are the last of the components to be mounted and that this is done at a protected work area.

All tools used during assembly, including soldering tools and solder baths, must be grounded. All hand-tools should be of conductive or anti-static material and, where possible, should not be insulated.

2.2.4 Testing PCBs

Completed PCBs must be tested at a protected work area. Place the soldered side of the circuit board on conductive or anti-static foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the workbench. After testing, replace the PCB on the conductive foam to await packing.

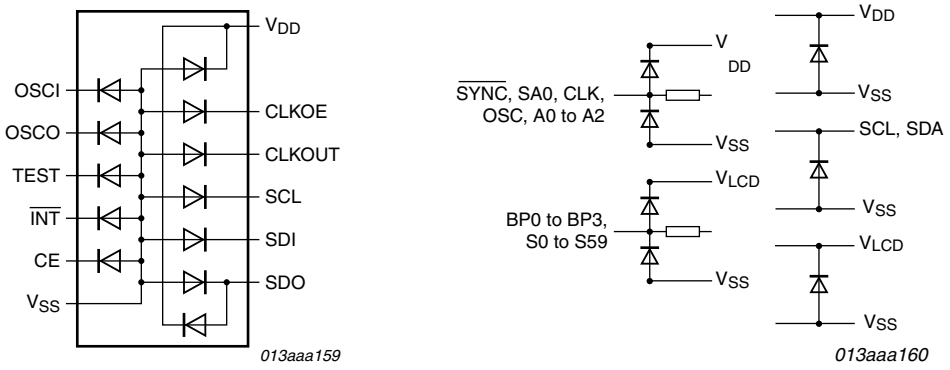
Assembled circuit boards containing electrostatic-sensitive devices should always be handled in the same way as unmounted components. They should also carry warning labels and be packed in conductive or anti-static packing.

2.2.5 Internal ESD protection circuits

Internal device protection diodes are connected to the pins to protect the IC against destructive ElectroStatic Discharge (ESD) and load disconnection spikes. If an ESD event occurs, the ESD protection circuits will shunt the charge in a controlled way, such that neither the functional parts nor the shunt path will be damaged by the discharge.

The device protection diodes are designed such that they allow the assembling of the IC but they are not sufficient to protect the assembled IC on the circuit board in any case. Therefore additional device protection circuits in the application may be necessary.

ESD protection diagrams are typically shown as overview circuit diagrams or particularized circuit diagrams (see Figure 16):



a. Overview circuit diagram. b. Particularized circuit diagram.

Fig 16. ESD protection circuit

Figure 17 shows typical internal device protection diode or transistor circuits of input and output pins:

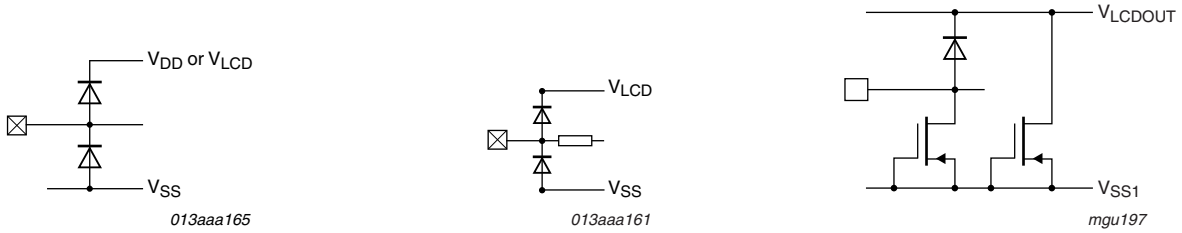


Fig 17. Protection of input and output pins (2 diodes/2 transistors)

Figure 18 shows internal device protection diode circuits of input and output pins but allowing an external supply that is unrelated to the protection circuit:

Fig 18. Protection of input and output pins with an unprotected external supply

Figure 19 shows the protection of supply rails where usually an ESD diode with a large current flow capability is put across the supply rails:

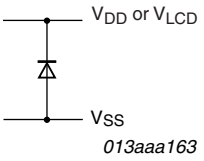


Fig 19. Protection of supplies

2.2.6 Verification of ESD protection

The ESD protection is verified by applying a defined energy on the terminals or leads of the IC. There are three models commonly in use:

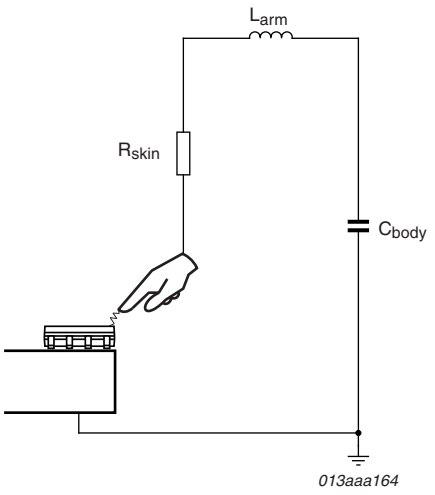
2.2.6.1 Human Body Model (HBM)

It simulates the electrical charging and then discharging of a person via the protection circuits.

The main criteria for this test is:

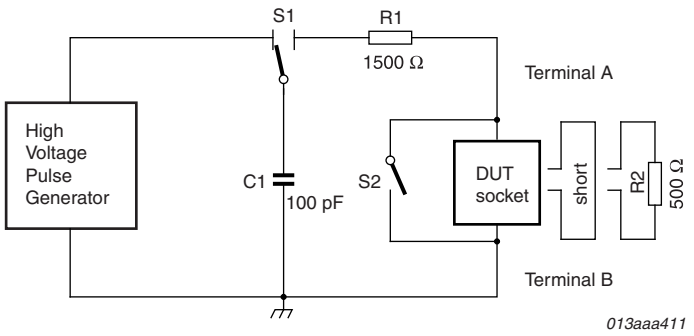
- Each sample for the stress test has to consist of 3 devices
- During the test, the devices don't need to operate fully, but they must not be damaged
- The test is performed at room temperature (25 °C)
- The test is made at different voltage levels (250 V, 500 V, 1000 V, 2000 V, 4000 V)
- The rise time is specified to be in a range of 2 ns to 10 ns
- The pulse duration is in a range of 100 ns to 200 ns

After each test at a certain voltage level, the stressed devices are tested according the requirements used in the parametric and functional tests. A failure is, when a device doesn't pass the parametric and functional tests anymore (device is destructed); the pass level indicates the highest voltage stress level after which all tested devices have still passed the parametric and functional tests without false.



R_{skin} = 1500 Ω, C_{body} = 100 pF, L_{arm} = 7.5 μH.

Fig 20. Schematic HBM ESD test circuit



DUT: Device Under Test.

Fig 21. Typical equivalent HBM ESD test circuit

A human body can easily reach the voltages used in this test (see Table 1). The HBM ESD test results are classified as shown in Table 2.

Table 2. HBM ESD classification table

Class	Voltage range
0	< 250 V
1A	250 V to < 500 V
1B	500 V to < 1000 V
1C	1000 V to < 2000 V
2	2000 V to < 4000 V
3A	4000 V to < 8000 V
3B	≥ 8000 V

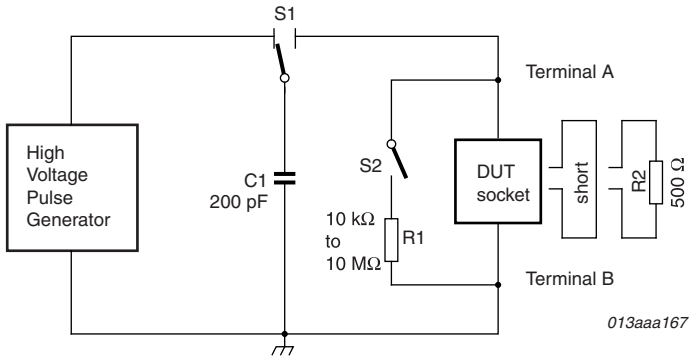
2.2.6.2 Machine Model (MM)

It simulates abrupt discharges, which are caused by contact with charged equipment. Therefore, the circuits are tested with rather moderate voltage, but with higher currents, as could occur with coupling of energy spikes.

The main criteria for this test is:

- The stress test has to be performed with 3 devices
- During the test, the devices don't need to operate fully, but they must not be damaged
- The test is performed at room temperature (25 °C)
- The test is made at different voltage levels (100 V, 200 V, 400 V)
- Each sample will be stressed at one voltage level using 1 positive and 1 negative pulse with a minimum of 0.5 second between pulses per pin
- The test is made with defined oscillation frequency and defined positive current peaks

After each test at a certain voltage level, the stressed devices are tested according the requirements used in the parametric and functional tests. A failure is, when a device does not pass the parametric and functional tests anymore (device is destructed); the pass level indicates the highest voltage stress level after which all tested devices have still passed the parametric and functional tests without false.



DUT: Device Under Test.

Fig 22. Typical equivalent MM ESD test circuit

The MM ESD test results are classified as shown in Table 3.

Table 3. MM ESD classification table

Class	Voltage range
M1	< 100 V
M2	100 V to < 200 V
M3	200 V to < 400 V
M4	≥ 400 V

2.2.6.3 Charged-Device Model (CDM)

It models the discharge of a charged IC to a grounded surface.

The main criteria for this test is:

- The stress test has to be performed with 3 devices
- The test is performed at room temperature (25 °C) with an ambient humidity of less or equal 60 %
- The test is made at different voltage levels (100 V, 200 V, 500 V, 1000 V, 2000 V)
- Each sample will be stressed at one voltage level using 3 positive and 3 negative discharges to each pin

After each test at a certain voltage level, the stressed devices are tested according the requirements used in the parametric and functional tests. A failure is, when a device doesn't pass the parametric and functional tests anymore (device is destructed); the pass level indicates the highest voltage stress level after which all tested devices have still passed the parametric and functional tests without false.

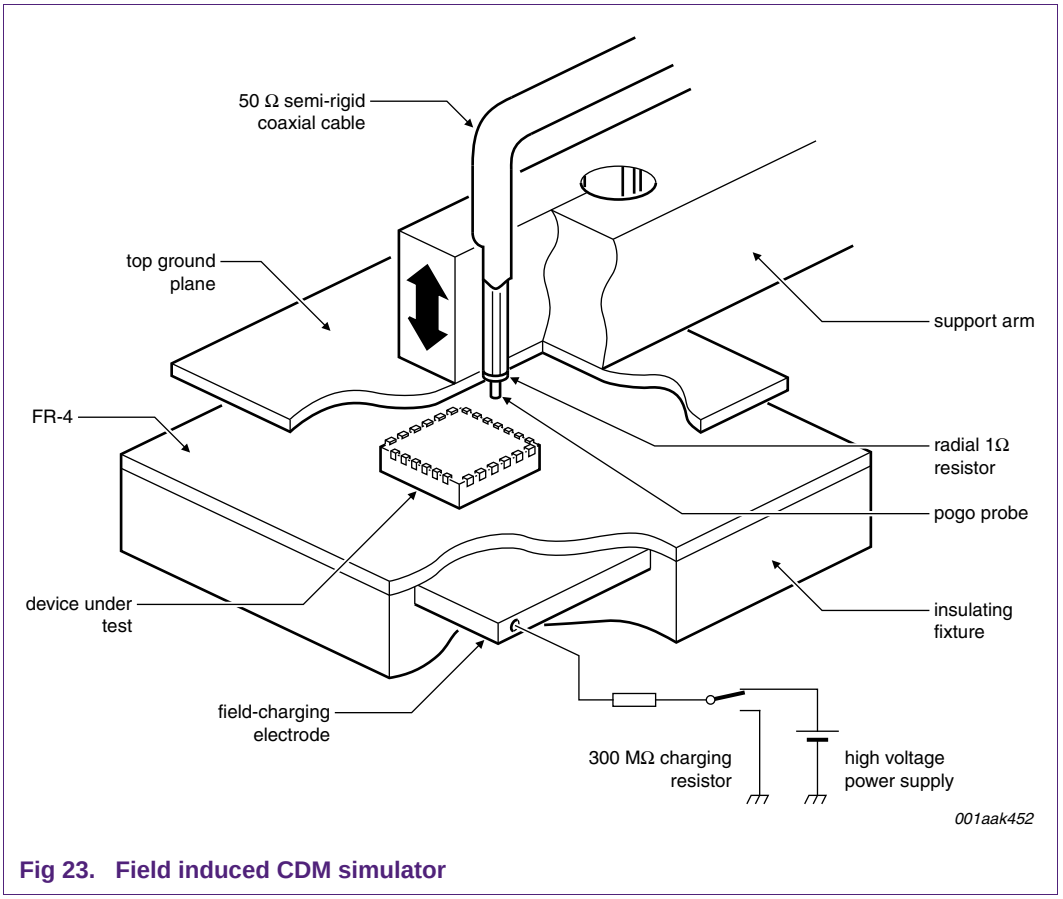


Fig 23. Field induced CDM simulator

The CDM ESD test results are classified as shown in Table 4.

Table 4. CDM ESD classification table

Class	Voltage range
C1	< 125 V
C2	125 V to < 250 V
C3	250 V to < 500 V
C4	500 V to < 1000 V
C5	1000 V to < 1500 V
C6	1500 V to < 2000 V
C7	≥ 2000 V

2.2.6.4 Latch-Up (LU) test

Latch-up is the transition of a semiconductor device in a low-impedance state which can lead to a short circuit and may destroy the device or bring it into an undefined state from which it can not be recovered other than switching the power supply off. The effect compares to the function of a thyristor. An ESD or a voltage peak may be the root-cause for generating such a large current. The latch-up test shows the quality of the protection of the device.

Latch-up tests are temperature sensitive. Therefore, there are two classes of latch-up tests:

- Class I: testing at room temperature
- Class II: testing at
  - maximum operating ambient temperature ($T_{amb(max)}$)

    or
  - maximum operating case temperature ($T_{case(max)}$)

    or
  - maximum operating junction temperature ($T_{j(max)}$)

In addition, there are two test methods:

- I-test (see testing circuit in Figure 24) where positive and negative current pulses are supplied to the input or input/output pin under test
- Power supply pin overvoltage test (see testing circuit in Figure 25) where overvoltage pulses are supplied to the supply pin under test

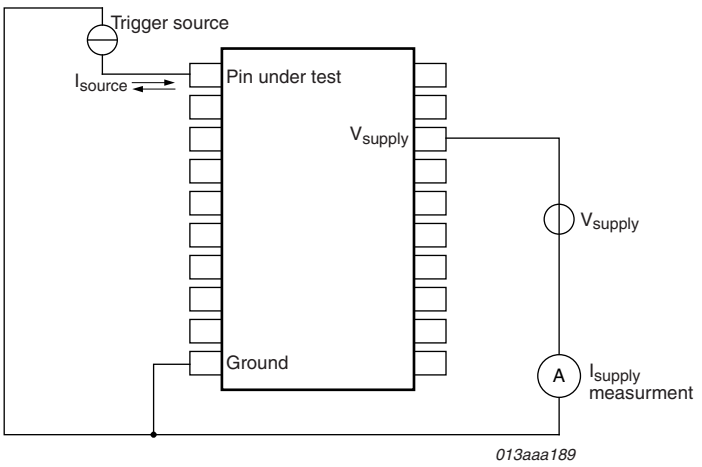


Fig 24. Typical equivalent circuit for input and input/output latch-up testing

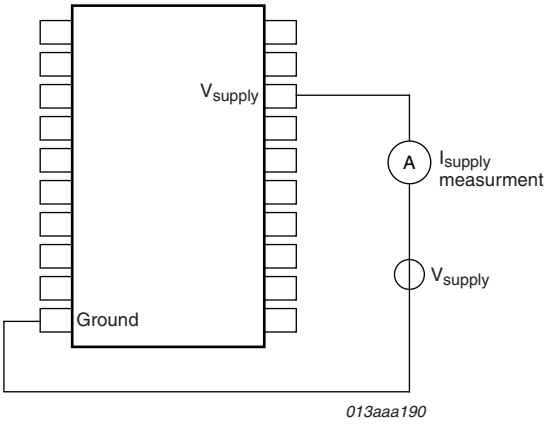


Fig 25. Typical equivalent circuit for supply overvoltage latch-up testing

The main criteria for this test is:

- Ground pins will not be latch-up tested
- The stress test has to be performed with 6 devices using the I-test and overvoltage test

There are two pass levels:

- Pass level A: devices passed $1.4 \times I_{nom}$ or I_{nom} + 10 mA (whichever is greater) without latching and passing the parametric and functional tests without false. The pass level indicates the highest current stress level where all tested devices have passed.
- Pass level B: devices passed below the values of level A but above the product maximum ratings and passing the parametric and functional tests without false. The pass level indicates the highest current stress level where all tested devices have passed.

A failure is, when a device neither passed level A nor level B.

3. ElectroMagnetic Compatibility (EMC)

All electrical and electronic products, apparatus, appliances, equipment, and installations marketed in countries of the European community must comply with a strict EMC directive. The EMC directive itself does not contain any technical requirements or limits but makes reference to generic or product-specific EMC requirements which will apply for both RF emission as well as immunity.

In the EMC directive, the European community gives the following definitions:

Electromagnetic compatibility — means the ability of a device, unit of equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment.

Electromagnetic disturbance — means any electromagnetic phenomenon which may degrade the performance of a device, unit of equipment or system. An electromagnetic disturbance may be electromagnetic noise, an unwanted signal or a change in the propagation medium itself.

Immunity — means the ability of a device, unit of equipment or system to perform without degradation of quality in the presence of an electromagnetic disturbance.

EMC differentiates between two different conditions:

1. **Emission** of unwanted electromagnetic energy by a source, and what kind of countermeasures can be taken to reduce or eliminate such emissions.
2. **Susceptibility** to electromagnetic energy by a victim, and what kind of protective measures can be taken to reduce or eliminate the susceptibility.

In terms of EMC, the victim is always an electronic device whereas the source can be an electronic device or a natural phenomenon such as a lightning.

3.1 Coupling modes

The EMC standards are covering the electromagnetic interference modes of conductive and radiative coupling (see Figure 26).

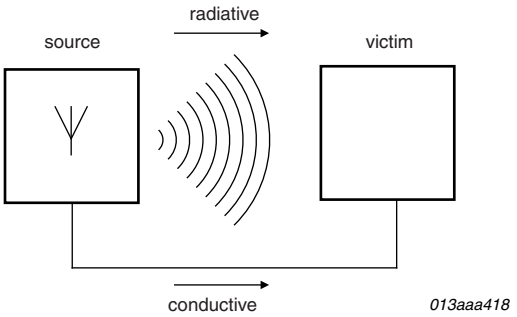


Fig 26. Conductive and radiative coupling

Conductive coupling requires a direct contact with a conducting hardware (transmission line, wire, cable, PCB trace) between the source and the victim.

Radiative coupling: The source emits an electromagnetic wave which is received by the victim.

3.2 EMC test methods and equipment

Devices will be tested for its emission and immunity of conductive and radiative coupling (see Table 5).

Table 5. EMC test methods

Test type	Coupling method	Method name	Reference
Conducted tests			
conducted emission	direct coupling via 150 Ω / 1 Ω network	150 Ω / 1 Ω method	IEC61967-4
conducted immunity	direct RF-power injection via DC block capacitor	Direct Power Injection (DPI)	IEC62132-4
Radiated tests			
radiated emission	E- and H-field radiation of entire IC	TEM-cell method	IEC61967-2
radiated immunity	E- and H-field radiation on entire IC	TEM-cell method	IEC62132-2

Emission tests are made with a TEM cell (see Figure 27) and immunity tests with GTEM cell (see Figure 28).

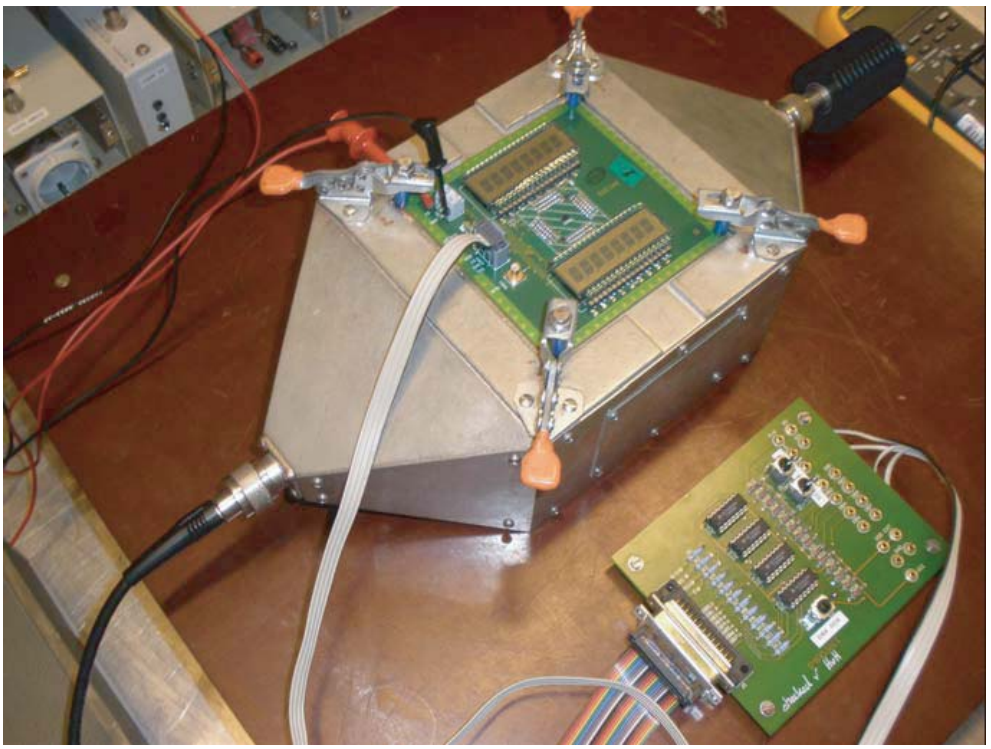


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Fig 27. TEM cell for emission tests

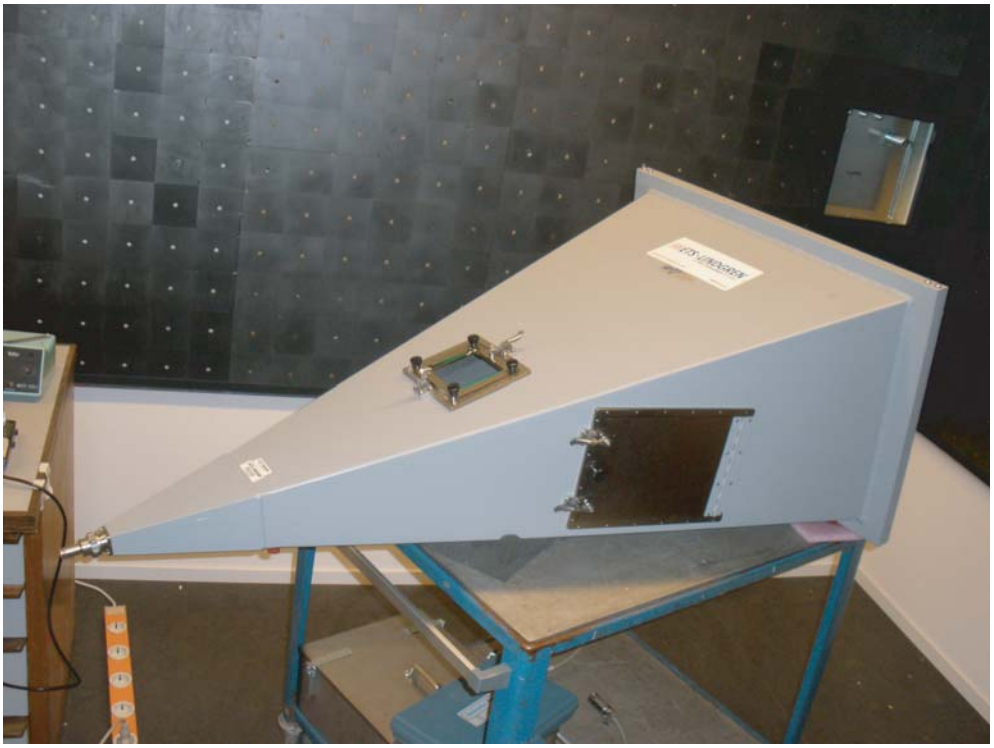

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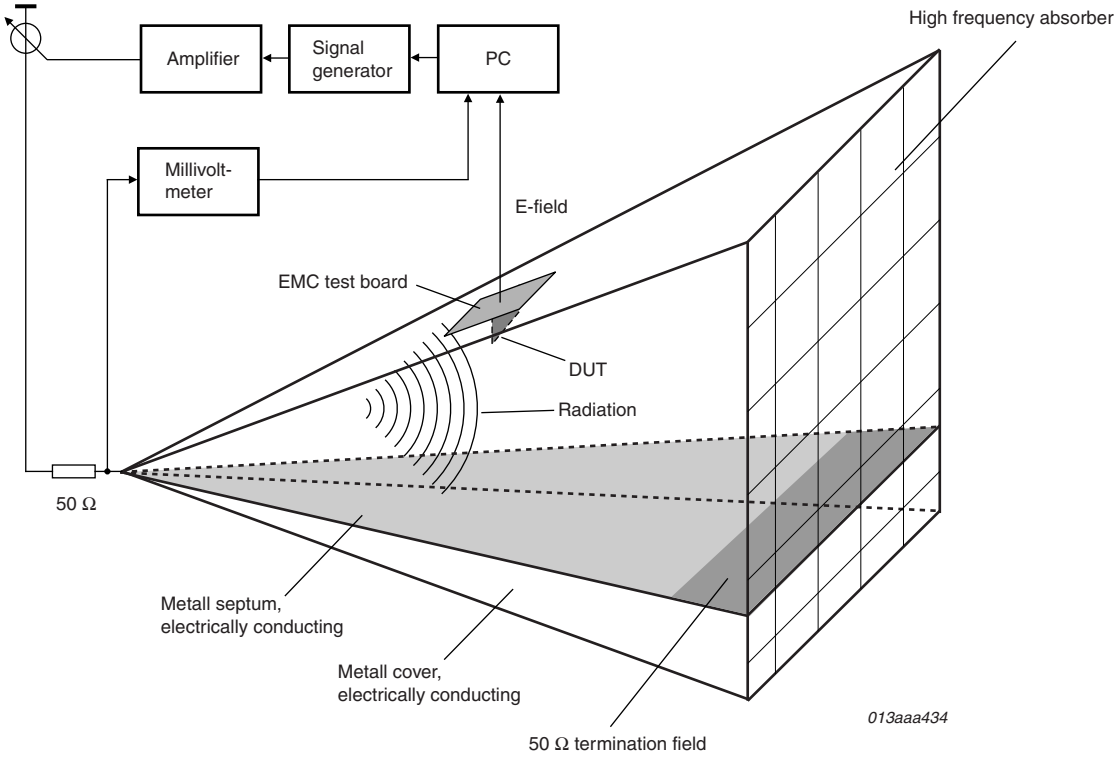
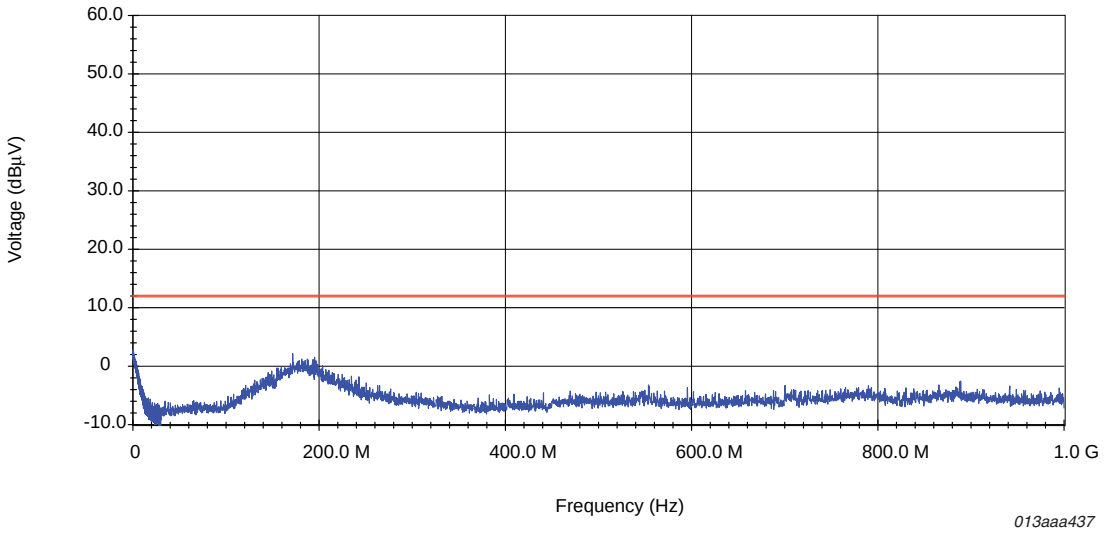
Fig 28. GTEM cell for immunity tests



DUT: Device Under Test.

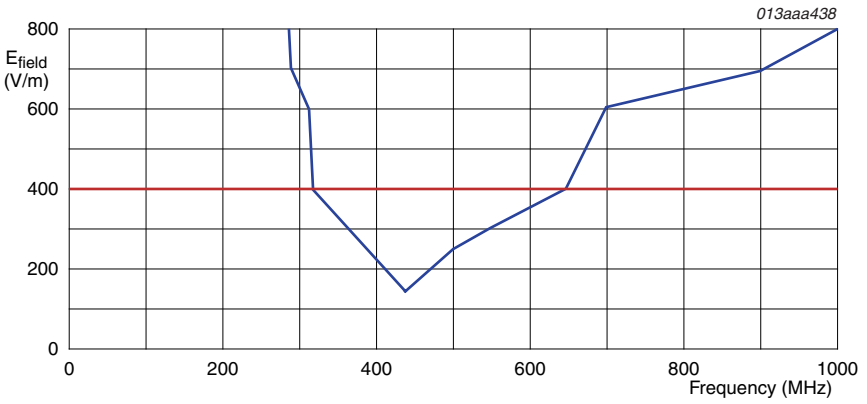
Fig 29. Schematic test configuration in a GTEM cell

3.3 EMC test results



12 dBµV is the reference limit.

Fig 30. Example result of a radiated emission test



400 V/m is the reference limit.

Fig 31. Example result of a radiated immunity test

4. References

[1] **AN10706 —** Handling bare die

[2] **AN10897 —** A guide to designing for ESD and EMC

[3] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[4] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[5] **IEC 61967 —** Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz
Part 1: General conditions and definitions
Part 2: Measurement of radiated emissions – TEM cell and wideband TEM cell method
Part 3: Measurement of radiated emissions – Surface scan method
Part 4: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method
Part 5: Measurement of conducted emissions – Workbench Faraday Cage method
Part 6: Measurement of conducted emissions – Magnetic probe method

[6] **IEC 62132 —** Measurement of electromagnetic immunity, 150 kHz to 1 GHz
Part 1: General conditions and definitions
Part 2: Measurement of radiated immunity – TEM cell and wideband TEM cell method
Part 3: Bulk current injection (BCI) method
Part 4: Direct RF power injection method
Part 5: Workbench Faraday cage method

[7] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[8] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[9] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[10] **JESD78 —** IC Latch-Up Test

[11] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[12] **NX2-00001 —** NXP Semiconductors Quality and Reliability Specification

[13] **NX3-00092 —** NXP store and transport requirements

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6. Contents

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Date of release: 10 November 2010
Document identifier: AN10853