DESIGNING WITH 88MW320/322

System Design Considerations
Technical Overview

AUGUST 10, 2020

SECURE CONNECTIONS
FOR A SMARTER WORLD

PUBLIC

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Introducing 88MW320/322

- Functional Overview
- Key considerations
- Collaterals

Single PCB Design Overview

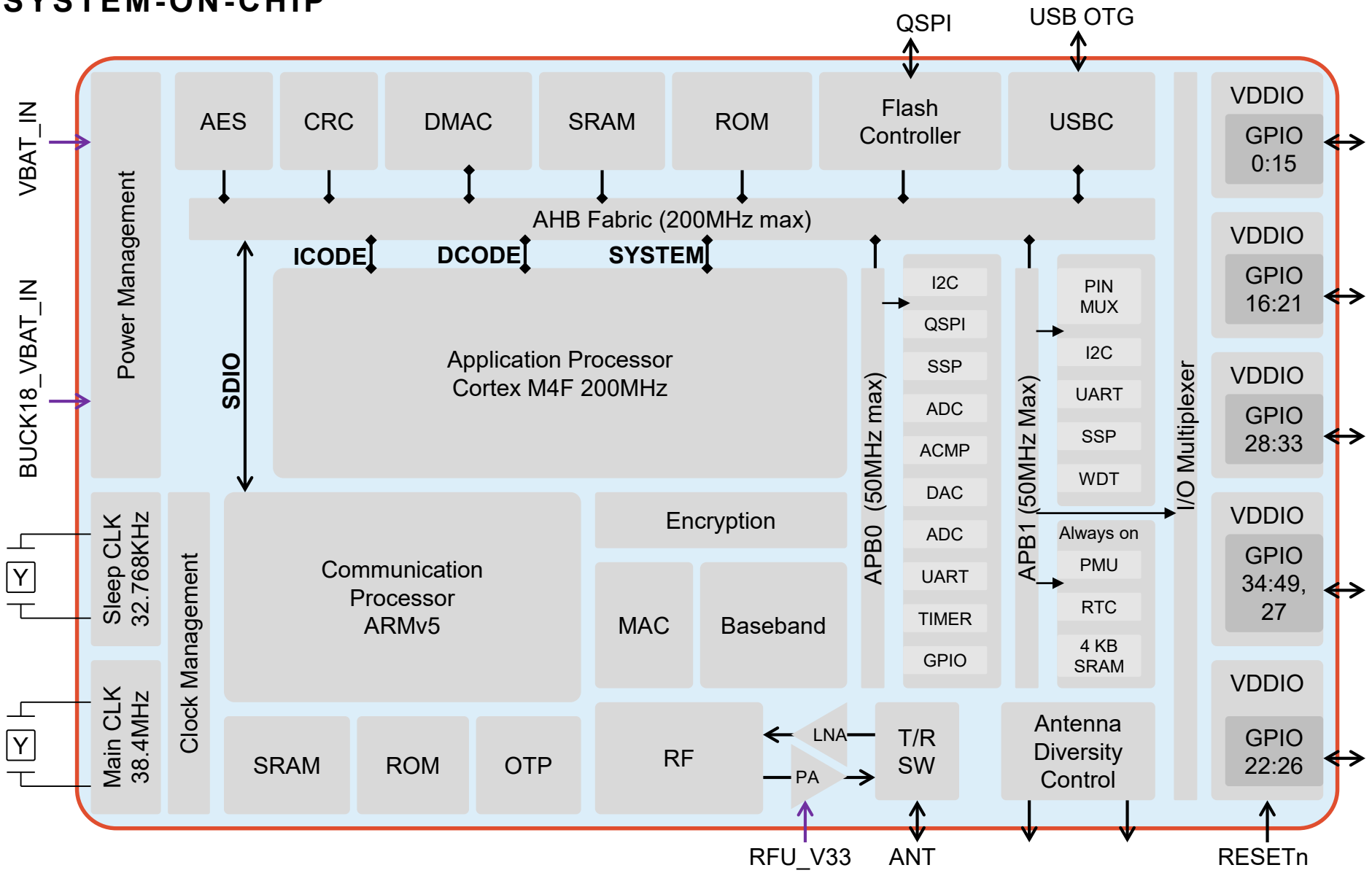
Introducing 88MW320 and 88MW322

SECURE CONNECTIONS
FOR A SMARTER WORLD

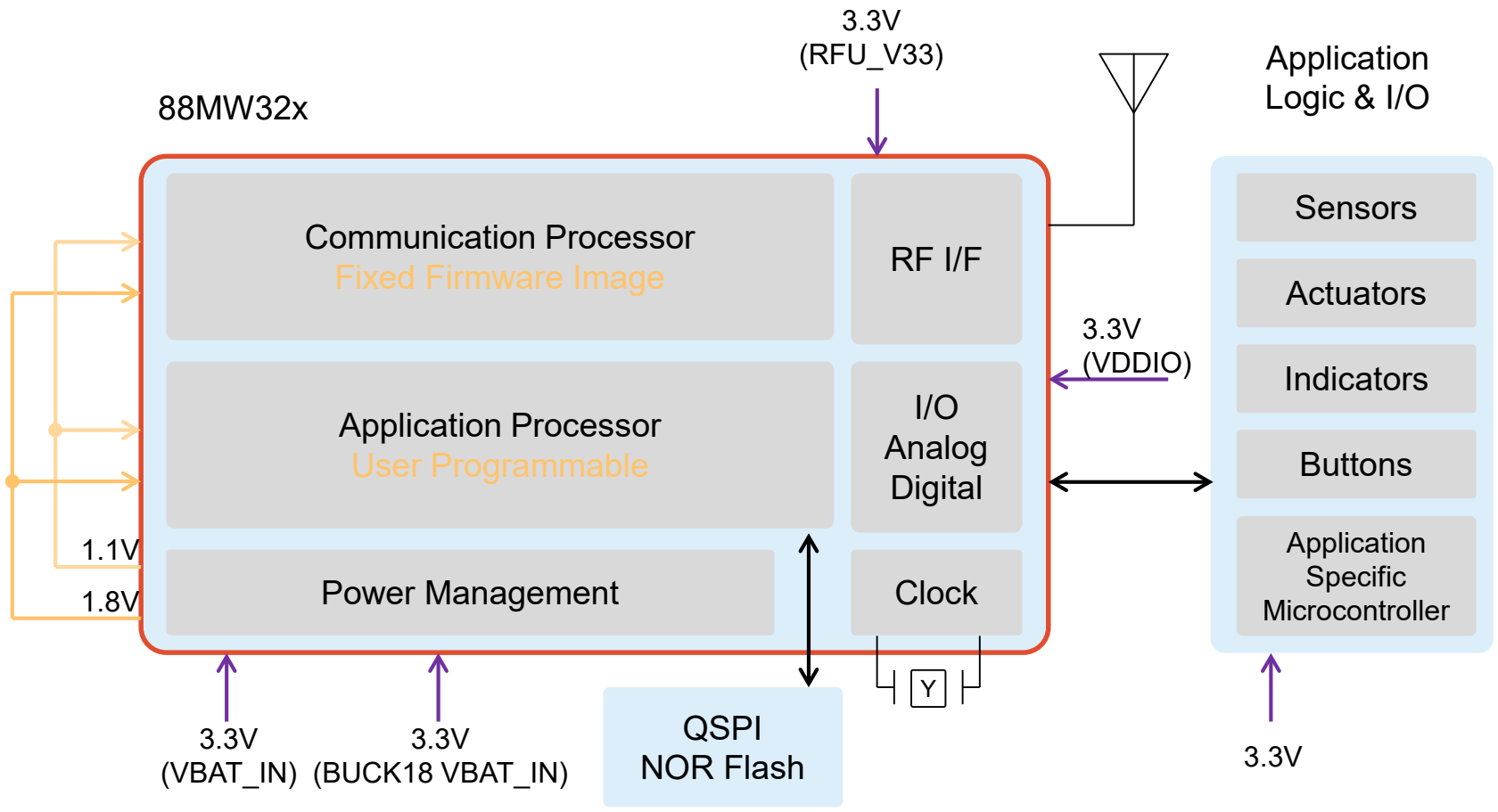
MAIN FEATURES

- Major system blocks
  - Microcontroller sub-system
  - Wi-Fi connectivity sub-system
- Device interface overview
  - Power
  - Clock
  - QSPI and Flash memory interface
  - Antenna interface
- Operating modes
- Always-on circuit and power saving features

88MW322 SYSTEM-ON-CHIP



88MW32X BASIC SYSTEM TOPOLOGY

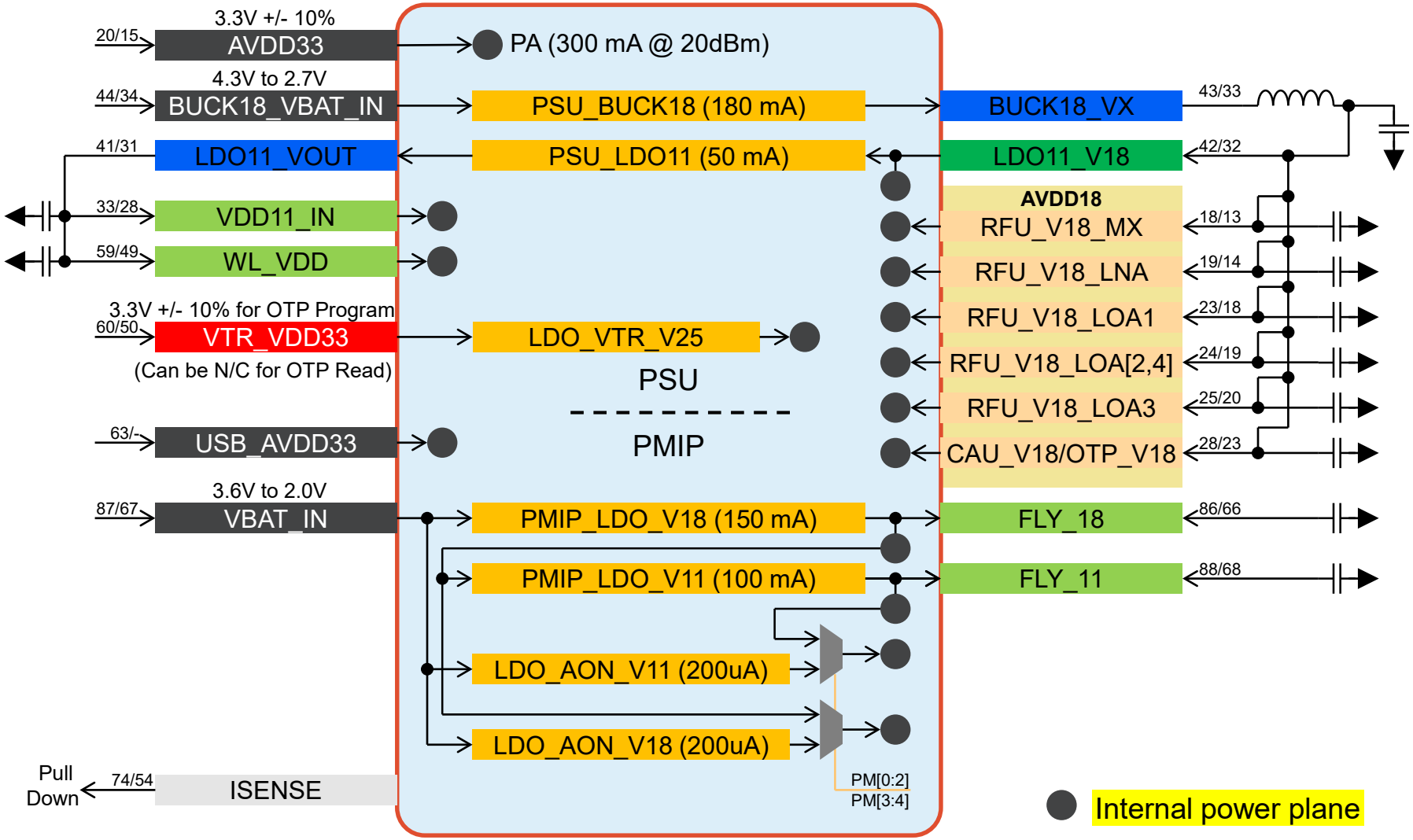


88MW32x integrates voltage regulators for 3.3V system power

KEY CONSIDERATIONS

- Power
  - On-chip BUCK regulator for 1.8V for Wi-Fi sub-system analog and digital
  - On-chip LDOs for application sub-system running at 1.8V and 1.1V
  - 3.3V +/- 10% for Wi-Fi TX PA
  - Multiple I/O bias rails
- Clock
  - Two internal and two external sources
    - Main clock reference at 38.4 MHz
    - Sleep clock / RTC reference clock at 32.768 kHz or ~32 kHz
- External Flash memory with Quad-bit SPI up to 50 MHz
  - Execute-In-Place (XIP) support for optimal performance
- Antenna
  - Low pass filter to single antenna for basic configuration
  - External RF switch needed for antenna diversity support

88MW322/320 POWER MANAGEMENT



POWER PIN TABLE AND DESIGN REFERENCE

Power pin	QFN88	QFN68
VBAT_IN (PMIP)	87	67
FLY18	86	66
FLY11	88	68
BUCK18_VBAT_IN (PSU)	44	34
BUCK18_VX	43	33
LDO11_V18	42	32
LDO11_VOUT	41	31
VDD11_IN	33	28
WL_VDD	59	49
AVDD33	20	15
AVDD18	18,19,23,24, 25,28	13,14,18,19, 20,23

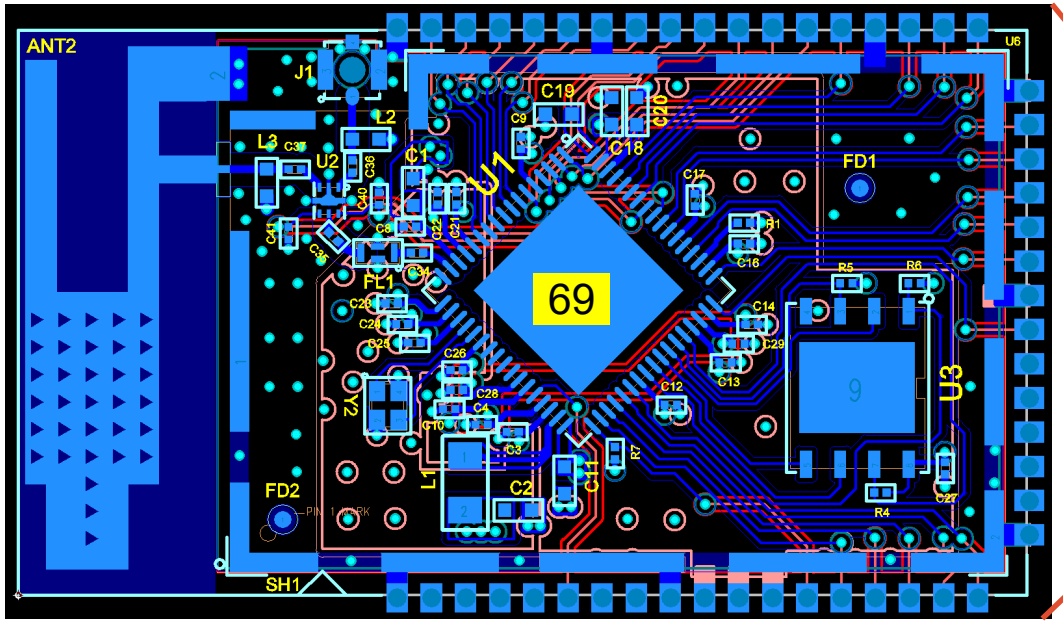
Refer to Schematics and Layout for:

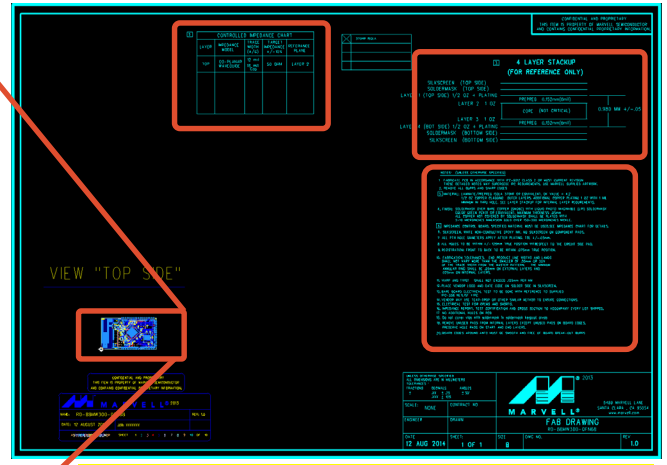
RD-88MW320-QFN-1B-2A_v1 “Stamp Module”,

RD-88MW322-QFN-1B-2A_v1 “Stamp Module”,

Free PADS viewer can be downloaded from:
http://www.pads.com/downloads/pads-pcb-viewer/

GENERAL GUIDELINES FOR LAYOUT (1/2)

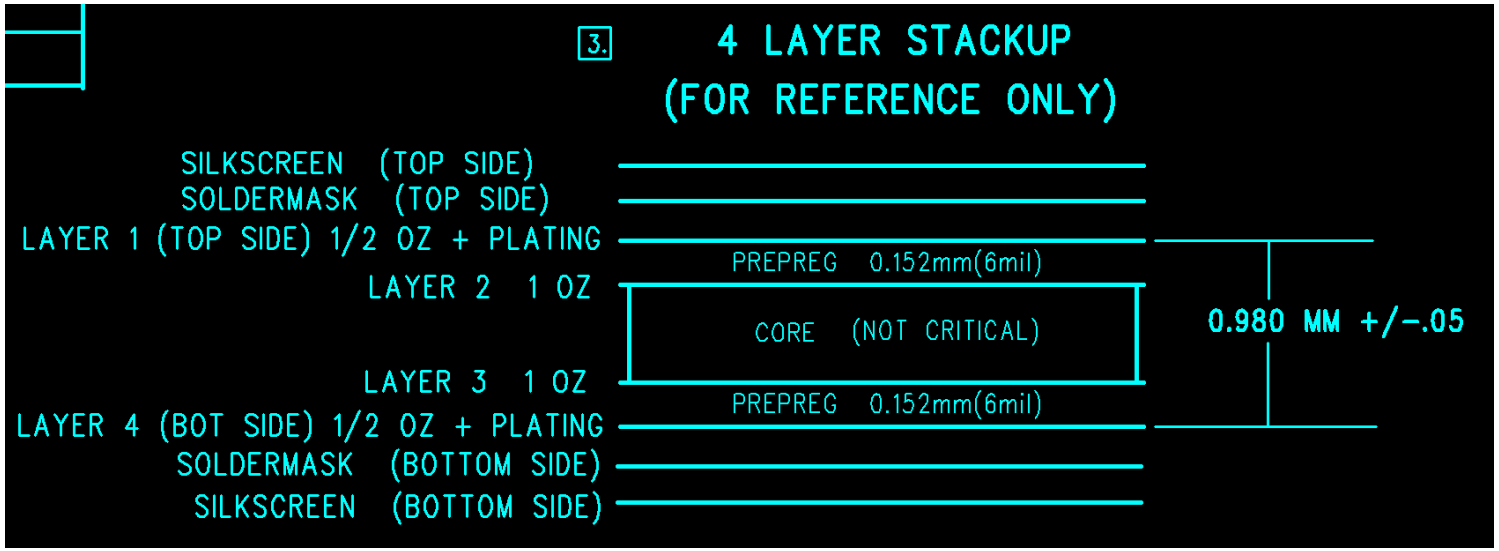




RD-88MW320-QFN-1B-2A_v1 Layout file has useful information for PCB stack-up and material details

- Fill the empty spaces of board with ground and connect them to ground plane with multiple vias
- GND pad from 69 should be connected to ground plane with maximum number of vias for better ground connectivity and heat sink capability
  - 25 vias are recommended.
- Traces of power should be as thick as possible

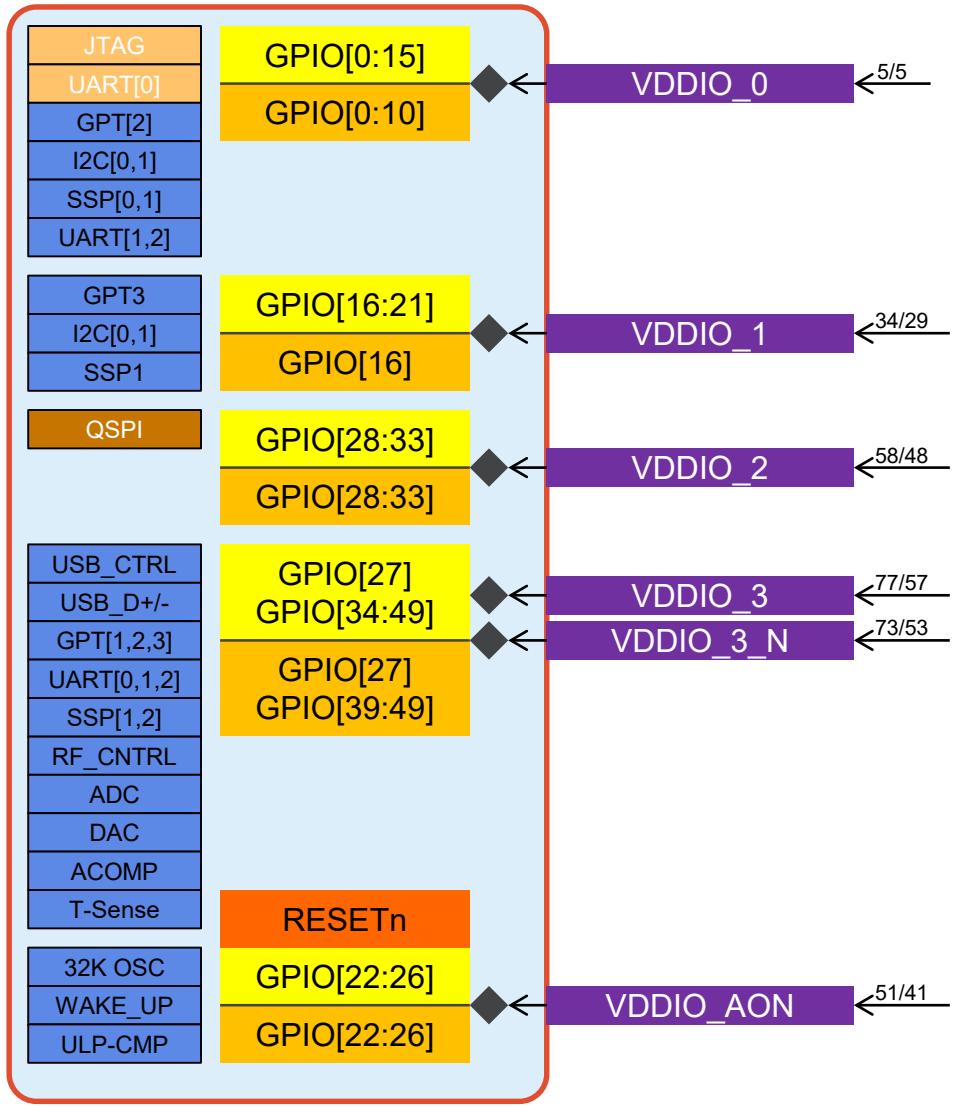
GENERAL GUIDELINES FOR LAYOUT (2/2)



- Layer #2 should be a uniform ground plane to reduce return path for current from other components
- Place decoupling capacitors as close to pin as possible
- Connect each ground pin of the chip to ground plane with separate via(s)
- Try not to share ground via for decoupling capacitors

See the detailed Layout Guidelines in “Single PCB Design Section”

88MW322/320 I/O RAILS



- Each I/O domain can be powered with 1.8V/2.5V/3.3V +/- 10%
  - RESETn bias is on VDDIO_AON
  - VDDIO_3/_3_N 1.8V +10%/-5%
- QSPI bus on VDDIO_2 dedicated for Flash device I/F for majority of applications
  - Majority of QSPI devices operate in 1.8V or 3.0/3.3V range
- JTAG and UART[0] signals useful for development, programming, monitoring, and provisioning

88MW322
88MW320

◆ I/O Bias power plane

MULTIFUNCTION MAPPING : VDDIO_0

VDDIO_0 Group : 16 for 88MW322, 11 for 88MW320

QFN88	QFN68	Reset	ALT 0	ALT 1	ALT 2	ALT 3	ALT 04	ALT 5	ALT 06	ALT 7
1	1	PU	GPIO_0	GPT0_CH0	UART0_CSTn	SSP0_CLK	-	-	-	-
2	2	PU	GPIO_1	GPT0_CH1	UART0_RTSn	SSP0_FRM	-	-	-	-
3	3	PU	GPIO_2	GPT0_CH2	UART0_TXD	SSP0_TXD	-	-	-	-
4	4	PU	GPIO_3	GPT0_CH3	UART0_RXD	SSP0_RXD	-	-	-	-
6	6	PU	GPIO_4	GPT0_CH4	I2C0_SDA	AUDIO_CLK	-	-	-	-
7	7	PU	GPIO_5	GPT0_CH5	I2C0_SCL	-	-	-	-	-
8	8	PU	TDO	GPIO_6	I2C0_SDA	-	-	-	-	-
9	9	PU	TCK	GPIO_7	UART2_CSTn	SSP2_CLK	I2C0_SDA	-	-	-
10	10	PU	TMS	GPIO_8	UART2_RTSn	SSP2_FRM	I2C0_SCL	-	-	-
11	11	PU	TDI	GPIO_9	UART2_TXD	SSP2_TXD	I2C1_SDA	-	-	-
12	12	PU	TRSTn	GPIO_10	UART2_RXD	SSP2_RXD	I2C1_SCL	-	-	-
13	n/a	PU	GPIO_11	GPT1_CH0	UART1_CSTn	SSP1_CLK	-	-	-	-
14	n/a	PU	GPIO_12	GPT1_CH1	UART1_RTSn	SSP1_FRM	-	-	-	-
15	n/a	PU	GPIO_13	GPT1_CH2	UART1_TXD	SSP1_TXD	-	-	-	-
16	n/a	PU	GPIO_14	GPT1_CH3	UART1_RXD	SSP1_RXD	-	-	-	-
17	n/a	PU	GPIO_15	GPT1_CH4	-	-	-	-	-	-

MULTIFUNCTION MAPPING : VDDIO_1 AND VDDIO_2

VDDIO_1 Group : 6 for 88MW322, 1 for 88MW320

QFN88	QFN68	Reset	ALT 0	ALT 1	ALT 2	ALT 3	ALT 04	ALT 5	ALT 06	ALT 7
35	30	PU	GPIO_16	CON[5]	-	AUDIO_CLK	-	-	-	-
36	n/a	PU	GPIO_17	GPT3_CH0	I2C1_SCL	-	-	-	-	-
37	n/a	PU	GPIO_18	GPT3_CH1	I2C1_SDA	SSP1_CLK	-	-	-	-
38	n/a	PU	GPIO_19	GPT3_CH2	I2C1_SCL	SSP1_FRM	-	-	-	-
39	n/a	PU	GPIO_20	GPT3_CH3	I2C0_SDA	SSP1_TXD	-	-	-	-
40	n/a	PU	GPIO_21	GPT3_CH4	I2C0_SCL	SSP1_RXD	-	-	-	-

VDDIO_2 Group : 6 for 88MW322, 6 for 88MW320

QFN88	QFN68	Reset	ALT 0	ALT 1	ALT 2	ALT 3	ALT 04	ALT 5	ALT 06	ALT 7
52	42	PU	GPIO_28	QSPI_SSn	GPIO_28	I2C0_SDA	-	-	GPT1_CH0	-
53	43	PU	GPIO_29	QSPI_CLK	GPIO_29	I2C0_SCL	-	-	GPT1_CH1	-
54	44	PU	GPIO_30	QSPI_D0	GPIO_30	UART0_CTS	SSP0_CLK	-	GPT1_CH2	-
55	45	PU	GPIO_31	QSPI_D1	GPIO_31	UART0_RTS	SSP0_FRM	-	GPT1_CH3	-
56	46	PU	GPIO_32	QSPI_D2	GPIO_32	UART0_TXD	SSP0_TXD	-	GPT1_CH4	-
57	47	PU	GPIO_33	QSPI_D3	GPIO_33	UART0_RXD	SSP0_RXD	-	GPT1_CH5	-

MULTIFUNCTION MAPPING : VDDIO_3

VDDIO_3 Group : 17 for 88MW322, 12 for 88MW320

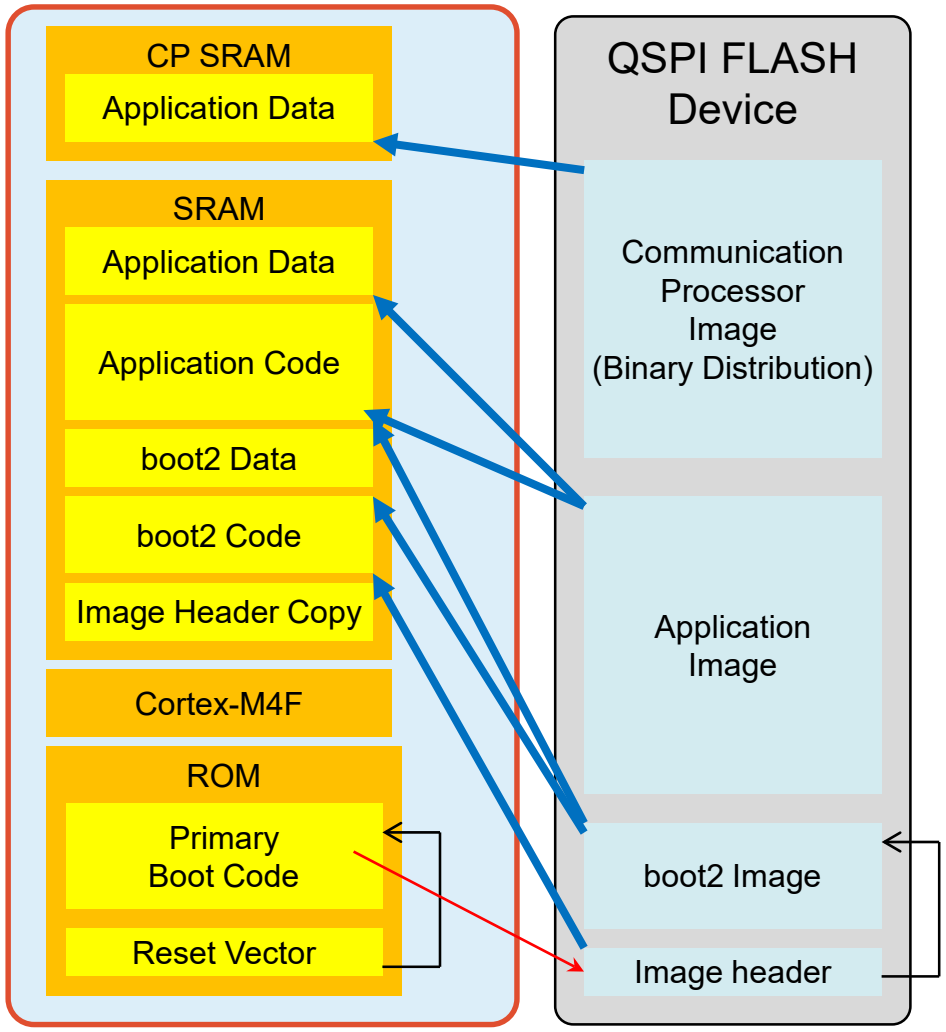
Q88	Q68	Reset	ALT 0	ALT 1	ALT2	ALT3	A-4	A-5	A-6	ALT7
66	51	PU	GPIO_27	CON[4]	UART0_TXD	USB_DRV_VBUS	-	-	-	-
67	n/a	PU	GPIO_34	GPT3_CH5	-	-	-	-	-	-
68	n/a	PU	GPIO_35	GPT0_CLKIN	UART1_CSTn	SSP0_CLK	-	-	-	-
69	n/a	PU	GPIO_36	GPT1_CLKIN	UART1_RTSn	SSP0_FRM	-	-	-	-
70	n/a	PU	GPIO_37	GPT2_CH5	UART0_RTSn	SSP0_TXD	-	-	-	-
71	n/a	PU	GPIO_38	GPT2_CLKIN	UART1_TXD	SSP0_RXD	-	-	-	-
72	52	PU	GPIO_39	GPT3_CLKIN	UART1_RXD	-	-	-	-	-
75	55	PU	GPIO_40	ADC_DAC_TRIGGER0	ACOMP0_GPIO_OUT	ACOMP1_GPIO_OUT	-	-	-	-
76	56	PU	GPIO_41	ADC_DAC_TRIGGER1	ACOMP0_EDGE_PULSE	ACOMP1_EDGE_PULSE	-	-	-	-
78	58	PU	GPIO_42	ADC0_0/AOMP0/ TS_INP/VOICE_P	UART1_CTSn	SSP1_CLK	-	-	-	-
79	59	PU	GPIO_43	ADC0_1/AOMP1/ DACB/TS_INN/VOICE_N	UART1_RTSn	SSP1_FRM	-	-	-	-
80	60	PU	GPIO_44	ADC0_2/ACOMP2/DACA	UART1_TXD	SSP1_TXD	-	-	-	RF_CNTL0_P
81	61	PU	GPIO_45	ADC0_3/ACOMP3/ EXT_VREF	UART1_RXD	SSP1_RXD	-	-	-	RF_CNTL0_N
82	62	PU	GPIO_46	ADC0_4/ACOMP4	UART2_CTSn	SSP2_CLK	-	-	-	-
83	63	PU	GPIO_47	ADC0_5/ACOMP5	UART2_RTSn	SSP2_FRM	-	-	-	-
84	64	PU	GPIO_48	ADC0_6/ACOMP6	UART2_TXD	SSP2_TXD	-	-	-	-
85	65	PU	GPIO_49	ADC0_7/ACOMP7	UART2_RXD	SSP2_RXD				

MULTIFUNCTION MAPPING : VDDIO_AON

VDDIO_AON Group : 5 for 88MW322 and 88MW320

QFN88	QFN68	Reset	ALT 0	ALT 1	ALT 2	ALT 3	ALT 04	ALT 5	ALT 06	ALT 7
46	36	PU	WAKE_UP0	GPIO_22	-	AUDIO_CLK	-	-	-	-
47	37	PU	WAKE_UP1	GPIO_23	UART0_CTSn	-	-	CMP_IN_P	-	-
48	38	PU	OSC32K	GPIO_24	UART0_RXD	SSP1_CLK	GPT1_CH5	CMP_IN_N	-	-
49	39	PU	XTAL32K_IN	GPIO_25	I2C1_SDA	SSP1_FRM	-	-	-	-
50	40	PU	XTAL32K_OUT	GPIO_26	I2C1_SCL	SSP1_TXD	-	-	-	-

EXECUTION SEQUENCE OUT OF RESET



"boot2" and application program image created with **WMSDKA**
(Wireless Microcontroller Software Development Kit)

- Out of RESET, C-M4F CPU fetches RESET vector from internal ROM that transfers execution to the Primary Boot Code (PBC) in the ROM itself
  - Reset vector and PBC are permanently programmed in the 88MW32x device and cannot be modified ever
- PBC loads the "image header" from external "serial Flash" device to internal SRAM
- Based on the header content, PBC loads second level "boot2" image from external serial Flash to internal SRAM and then executes it from SRAM
- "boot2" code then loads the application image in SRAM along with its data, and executes the application program
- C-M4F CPU also transfers the image for the Communication Processor (CP), which resides in its own SRAM

DESIGN NOTE: RESETN AND CONFIGURATION

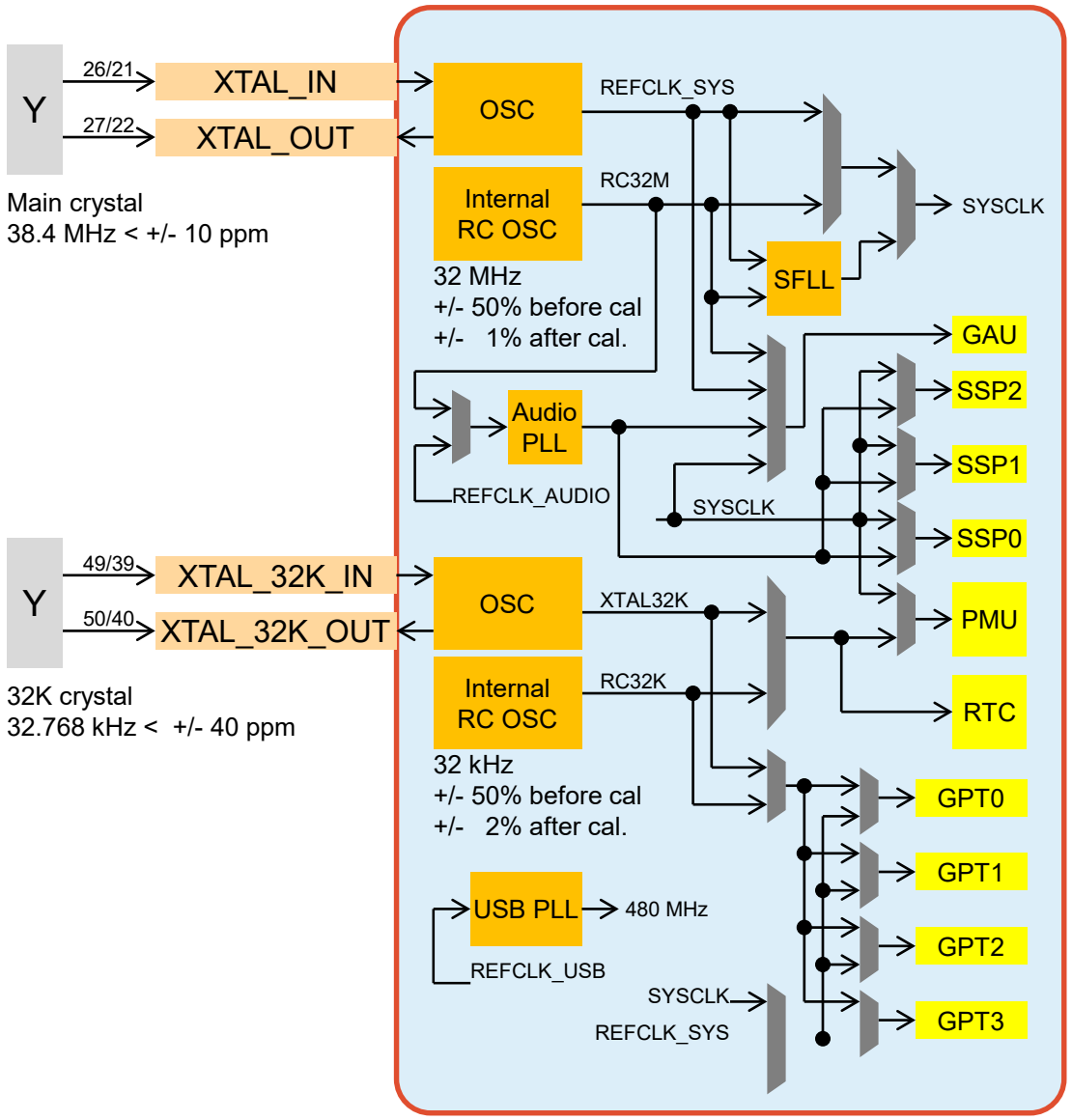
- 88MW32x SoC executes code from internal ROM (also referred as Boot ROM) after valid reset condition is de-asserted
  - ROM is 128KB (permanently programmed in silicon)
    - PBC 0x000000 : 0x007FFF
    - WMSDKA Library 0x008000 : 0x01FFFF
  - Depending on CON[5:4], loads code from Flash/UART/USB
- Reset sources can be
  - Power-On-Reset (POR)
  - RESETn pin
  - Cortex-M4F exit from low-power mode
  - Warm reset
    - Brown-out detection by power management
    - Soft RESET instruction from CPU
    - CM4F exit LOCKUP state (for example NMI)
    - Watchdog timer timeout

Boot configuration	
CON[5:4]	**BOOT FROM**
00	UART
01	RESERVED
10	USB (88MW322 only)
11	Flash (default)

GPIO used by boot code	
GPIO	**Function**
27	CON[4]
16	CON[5], Indication
2	UART0_TXD
3	UART0_RXD
28:33	QSPI bus

The designer should provide access to GPIO_27 and GPIO_16 on the PCBA to support the alternate boot method.

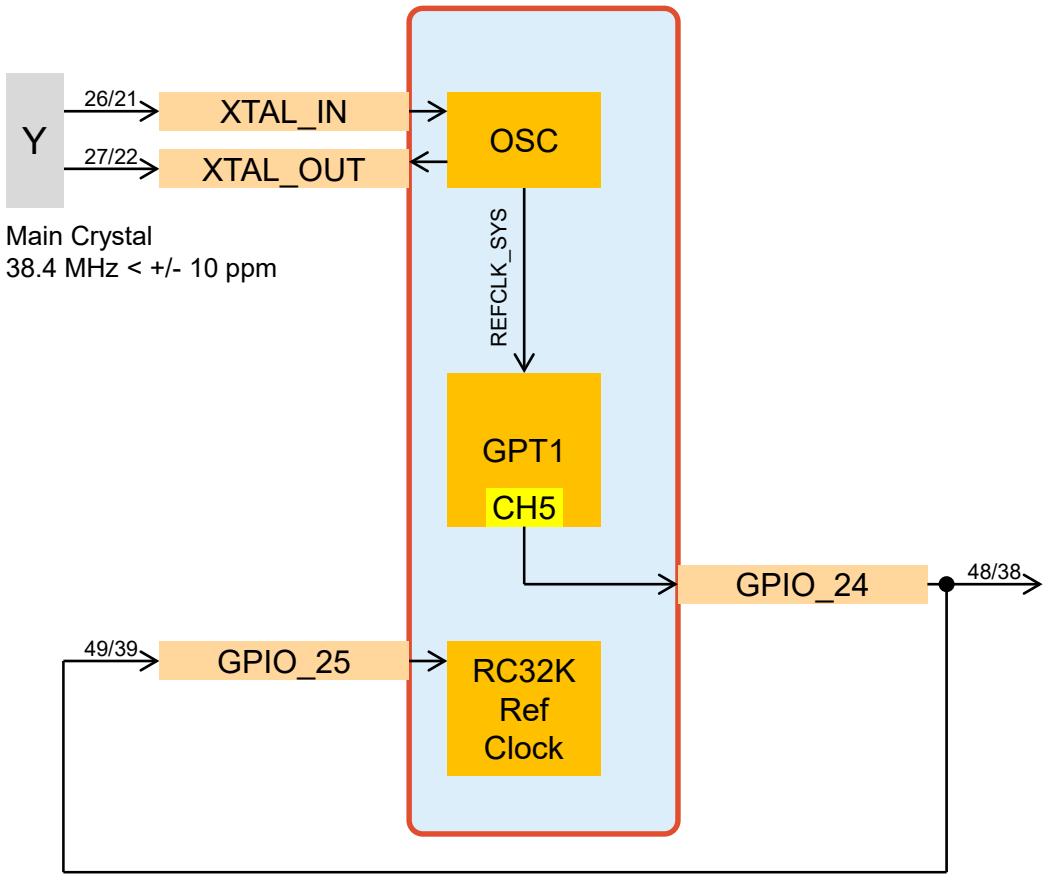
CLOCK SOURCES AND DISTRIBUTION



- External or internal reference clock generation for FAST and SLOW clocks
  - FAST: 38.4 MHz
  - SLOW: 32.768 kHz
- Three PLLs for application specific operation
  - System PLL (SFLL) : 200 MHz max
  - Audio PLL (AUPLL)
  - USB PLL (USBPLL) for HS/FS/LS
- SYSCLK and its derivatives used by all other system blocks
  - Two programmable fractional divider shared between UART[0:3]

DESIGN NOTE: USING RC32K CLOCK REFERENCE

Reduce system cost and board space by not using external 32.768 kHz crystal

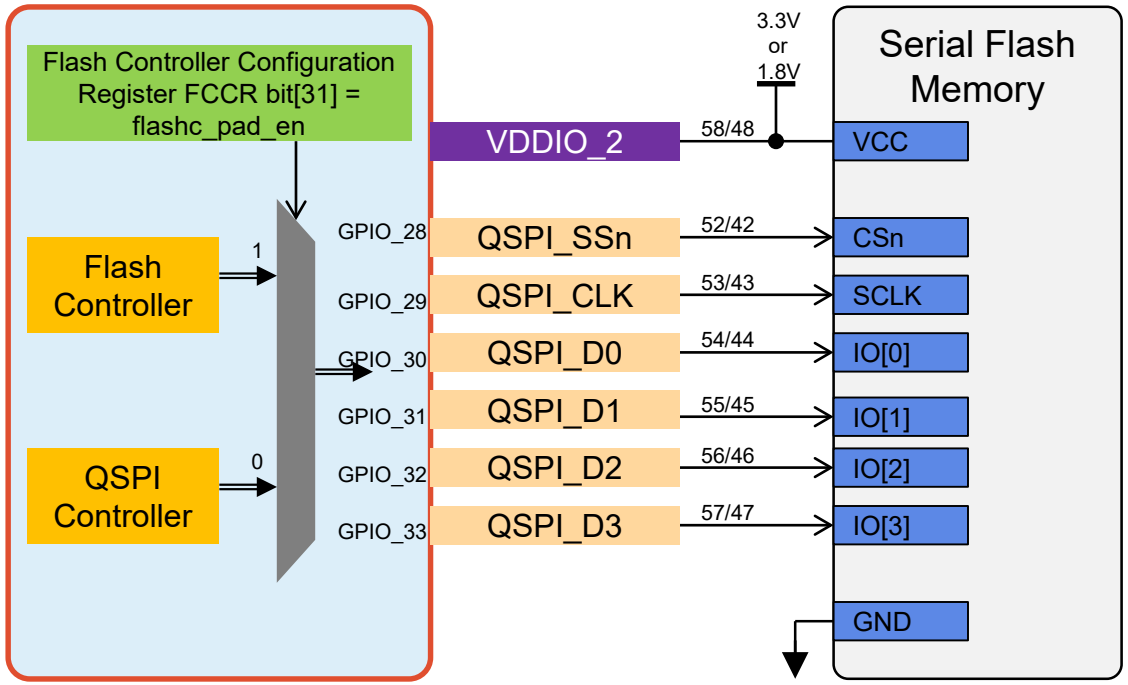


- Using on-chip RC OSC for 32 kHz reference requires in-system calibration to compensate for:
  - Voltage drift
  - Temperature drift
- Accurate REFCLK_SYS 38.4 MHz required
- Divided clock at 32.768 KHz output on GPIO_24 needs to be feed back to GPIO_25 off-chip

GPIO_24 and GPIO_25 are not available for application use

GPT1-CH5 is not available for application use, and GPT1 clock source is fixed, derived from 38.4 MHz

QSPI PHYSICAL INTERFACE TO FLASH MEMORY

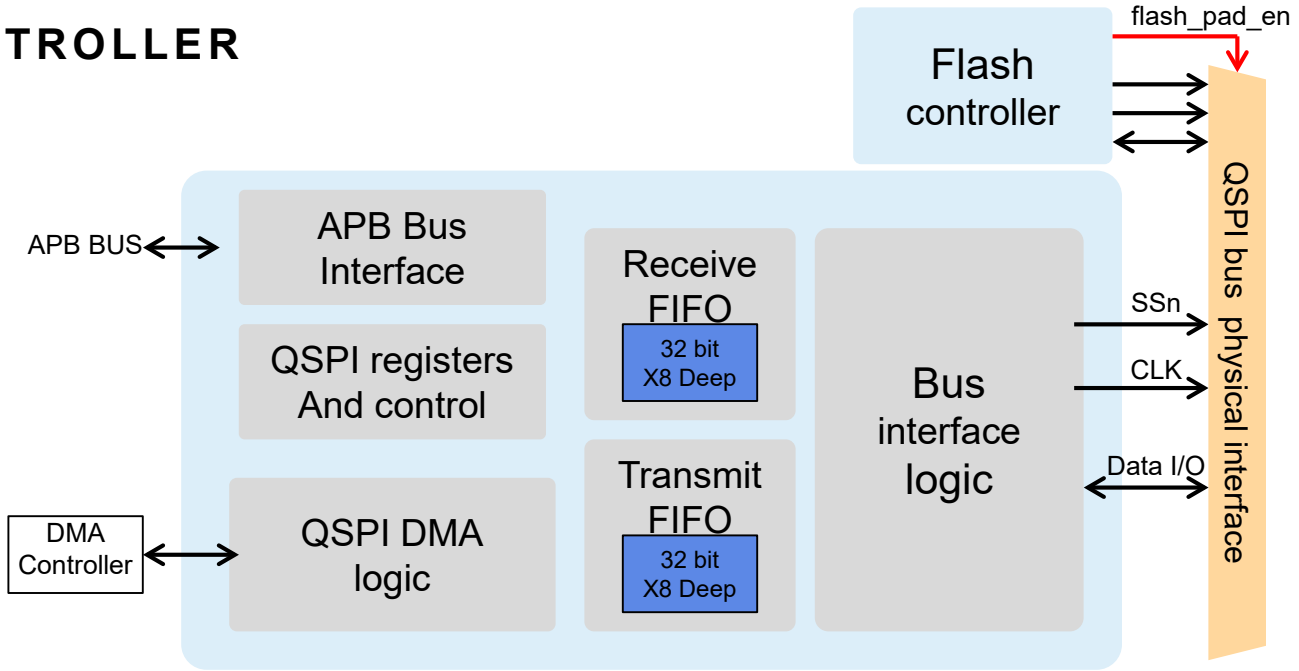


QSPI physical interface to external QSPI Flash Memory Device is multiplexed between two internal functional blocks:

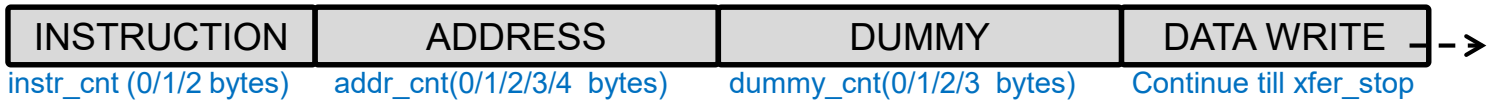
- QSPI controller
- Flash controller

- Support for data transfer on 1-bit (DO + DI) or bi-directional 2-bit or 4-bit data bus
- 50 MHz max clock
- VDDIO_2 exclusive to 6 signals for QSPI
  - 3.3V or 1.8V common
- Flash controller useful for READ operations
  - For Write/Erase use QSPI
- “Basic” and “Additional” features use select set of SPI Flash “commands”

QSPI CONTROLLER

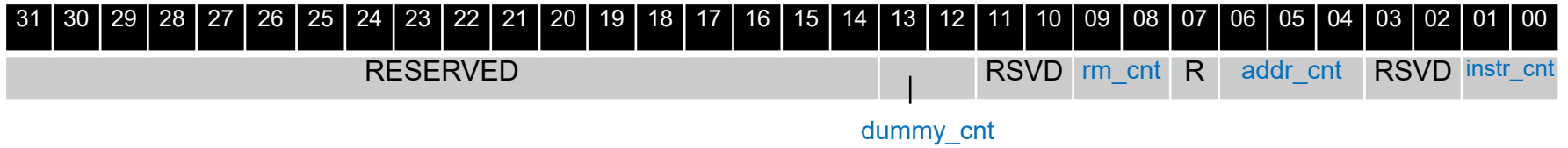


Bus transaction: WRITE

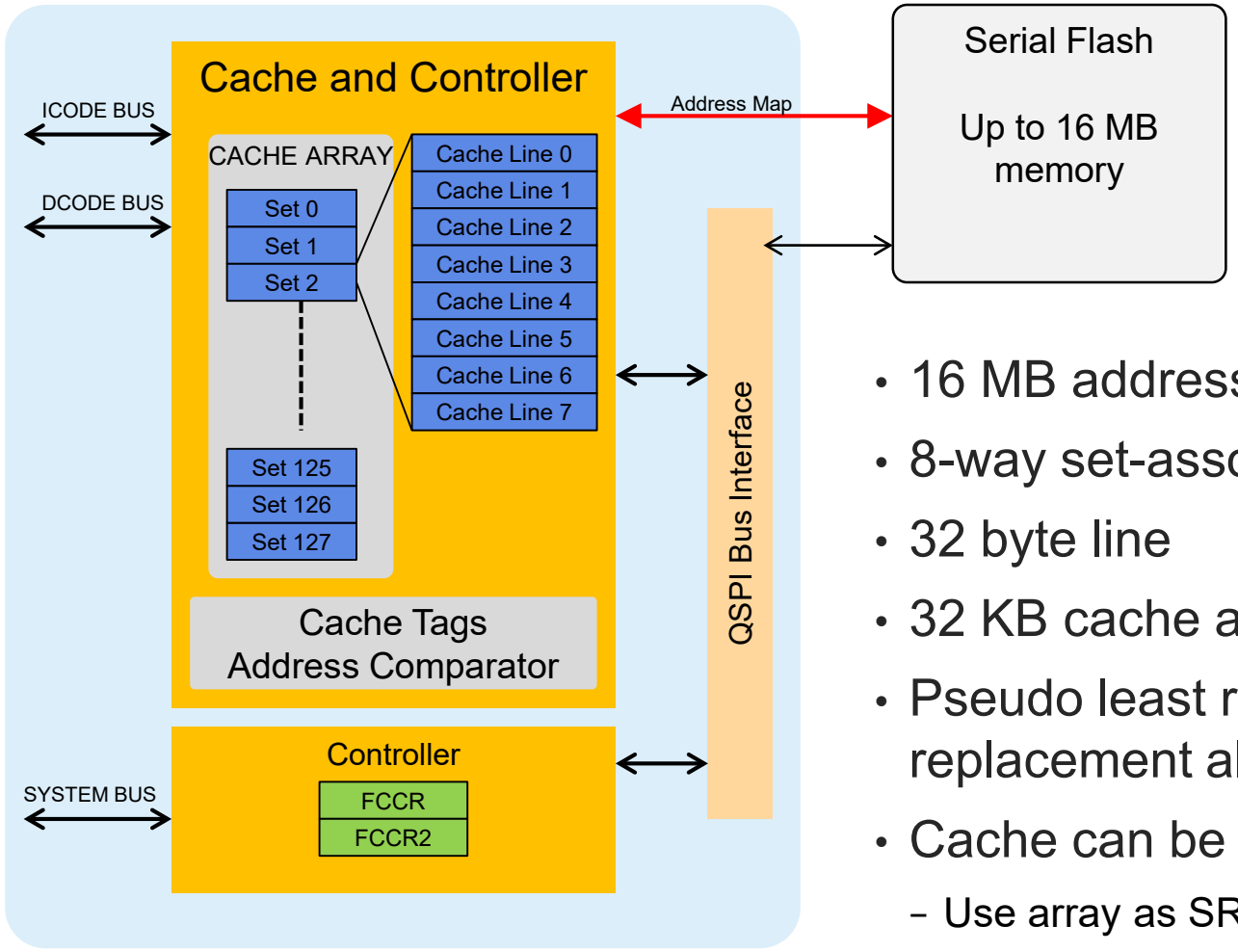


Bus transaction: READ

HdrCnt



FLASH MEMORY CONTROLLER

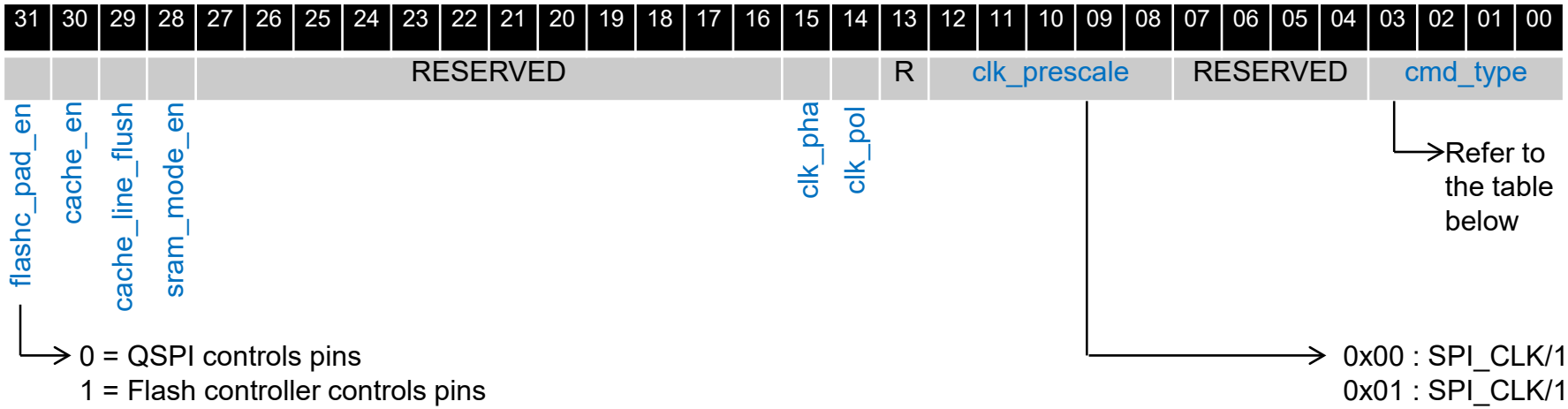


Support for Execute-In-Place (XIP)
by caching I/D Code bus

- 16 MB address space
- 8-way set-associative cache
- 32 byte line
- 32 KB cache array
- Pseudo least recently used line replacement algorithm
- Cache can be bypassed
  - Use array as SRAM

FLASH CONTROL REGISTER

FCCR



cmd_type	Code	Command
0x0	0x03	Read Data
0x1	0x0B	Fast Read
0x2	0x3B	Fast Read Dual Output
0x3	0x6B	Fast Read Quad Output
0x4	0xBB	Fast Read Dual I/O
0x5	**0xBB**	**... w/ Continuous Read Mode**
0x6	0xEB	Fast Read Quad I/O
0x7	0xEB	... w/ Continuous Read Mode

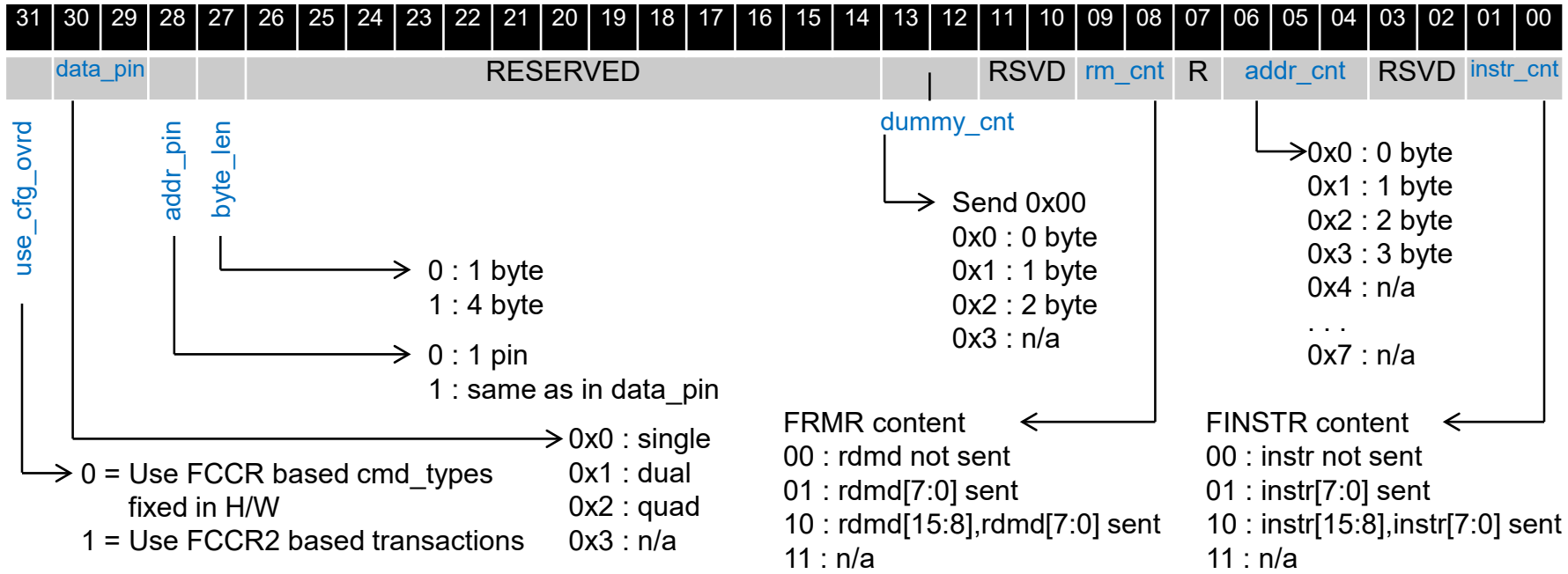
cmd_type	Code	Command
0x8	0xE7	Word Read Quad I/O
0x9	0xE7	… w/Continuous Read Mode
0xA	0xE3	Octal Word Read Quad I/O
0xB	0xE3	… w/Continuous Read Mode
0xC	0xFFFF	Exit from cont. Read Dual
0xD	0xFF	Exit from cont. Read Quad
0xE	-	Not used
0xF	-	Not used

Default command

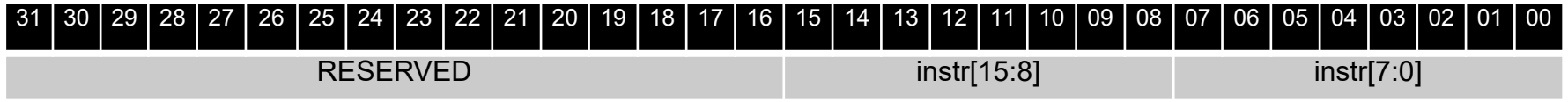
*** Bus cycles follow Winbond W25Q Device Family Requirements**

USING FLASH CONTROL REGISTER 2

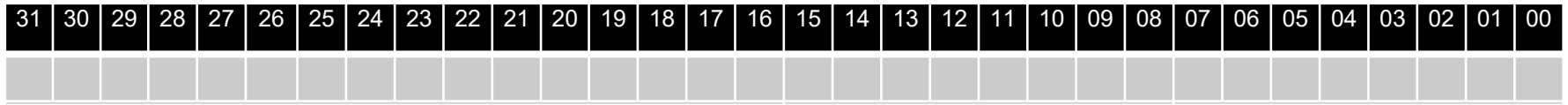
FCCR2



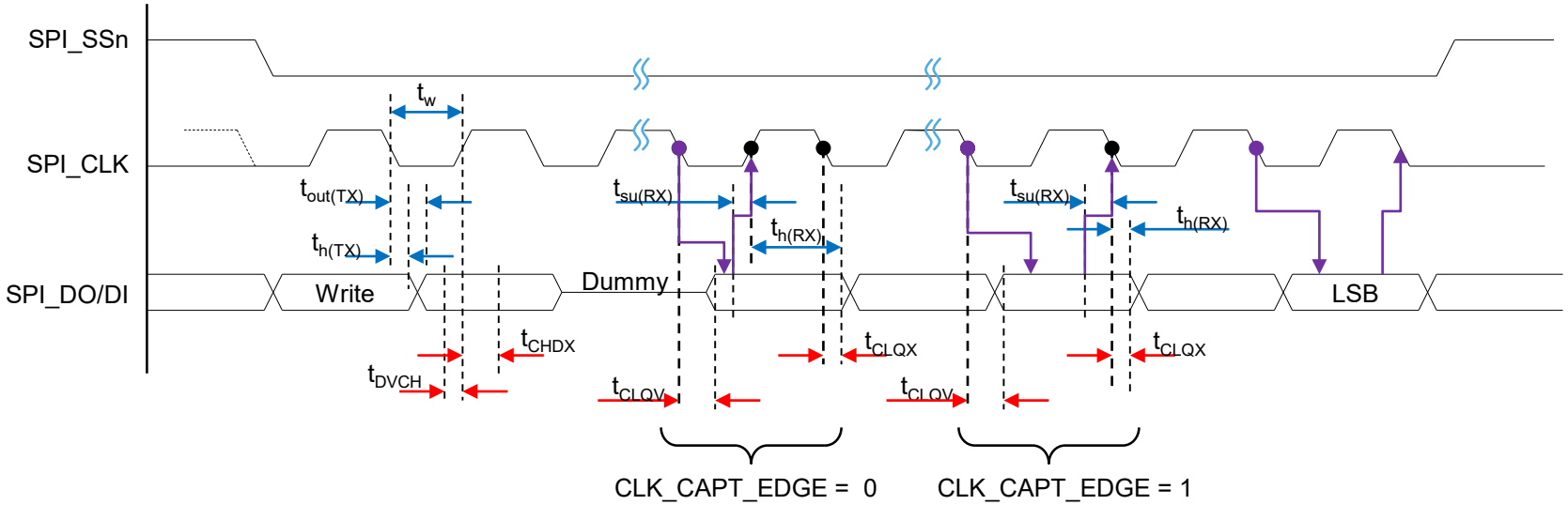
FINSTR



FRMR



DESIGN NOTE: READ TIMING ANALYSIS AT 50 MHZ



Parameter	Value (ns)
$t_{w(min)}$	20/2 – 0.5 = 9.5
$t_{w(max)}$	20 - $T_{w(min)}$ = 10.5
t_{CLQV}	8.5
t_{CLQX}	0
$t_{su(RX)}$	8
$t_{h(RX)}$	0

Flash to MW32x

MW320 side data setup time analysis:
$t_{w(min)} – t_{CLQV}$ = 9.5 – 8.5 = 1.0 ns
$t_{su(RX)}$ = 8 ns
Design margin available = **-7.0 ns**

MW320 side data hold time analysis:
$t_{w(min)} + t_{CLQX(TX)}$ = 9.5 + 0 = 9.5 ns
$t_{h(RX)}$ = 0 ns
Design margin available = **9.5 ns**

Flash to MW32x

MW320 side data setup time analysis:
$t_{cy} – t_{CLQV}$ = 20 – 8.5 = 11.5 ns
$t_{su(RX)}$ = 8 ns
Design margin available = **3.5 ns**

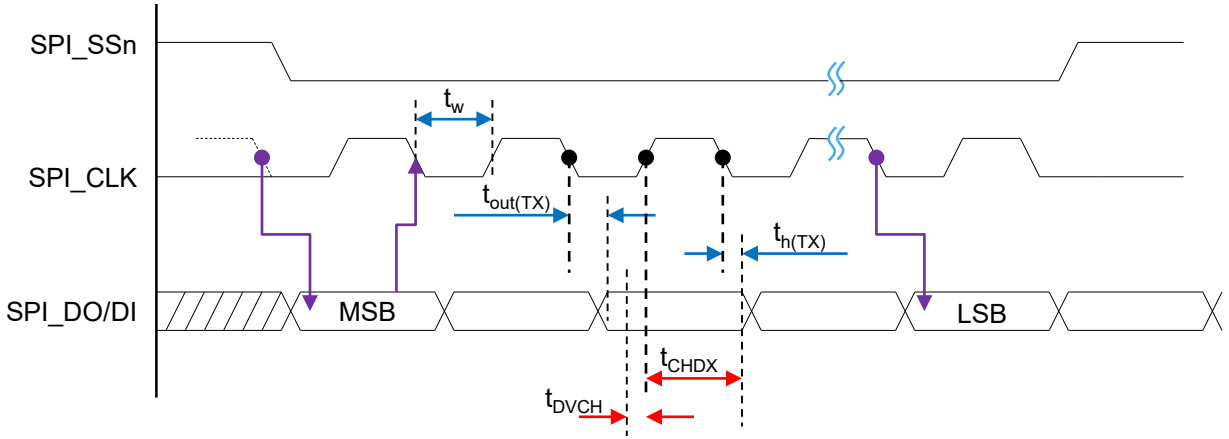
MW320 side data hold time analysis:
$t_{CLQX(TX)}$ = 0 ns
$t_{h(RX)}$ = 0 ns
Design margin available = **0 ns**

USE CLK_CAPT_EDGE = 1

Clock Low to Output Valid 2.5V-3.6V / 3.0V-3.6V	tCLQV1	tV1			7/6	ns
Clock Low to Output Valid (for Read ID instructions) 2.5V-3.6V / 3.0V-3.6V	tCLQV2	tV2			8.5/7.5	ns
Output Hold Time	tCLQX	tHO	0			ns

From: Winbond W25Q80BV Datasheet

DESIGN NOTE: WRITE TIMING ANALYSIS AT 50 MHZ



Parameter	Value (ns)
$t_{w(min)}$	20/2 – 0.5 = 9.5
$t_{w(max)}$	20 - $t_{w(min)}$ = 10.5
$t_{out(TX)}$	7
$t_{h(TX)}$	0
t_{DVCH}	2
t_{CHDX}	5

MW32x to Flash

Flash side data setup time analysis:
$t_{w(min)} - t_{out(TX)}$ = 9.5 – 7 = 2.5 ns
t_{DVCH} = 2 ns
Design margin available = **0.5 ns**

Flash side data hold time analysis:
$t_{w(min)} + t_{h(TX)}$ = 9.5 + 0 = 9.5 ns
t_{CHDX} = 5 ns
Design margin available = **4.5 ns**

Data In Setup Time	tDVCH	tDSU	2			ns
Data In Hold Time	tCHDX	tDH	5			ns

From: Winbond W25Q80BV Datasheet

Summary

Flash device requirement

Parameter	Value required (ns)
t_{DVCH} (min)	2.5 or less
t_{CHDX} (min)	9.5 or less
t_{CLQV} (max)	12.0 or less
t_{CLQX} (min)	0.0 or more

Use CLK_CAPT_EDGE = 1

DESIGN NOTE: FLASHC AND QSPI REGISTER SETTING

- QSPI bus timing needs to be set in two functional blocks
  - QSPI @0x46010000 : 0x4601003B
  - Flash Controller (FLASHC) @0x44003000 : 0x4400302F
- CLK_CAPT_EDGE bit is at different bit-field
  - QSPI → Serial Interface Timing Register (offset 0x24) bit 6
  - FLASHC → Flash Controller Timing Register (offset 0x04) bit 4
- Software component to check
  - Boot ROM
  - Boot2
  - Drivers and Framework
  - Tools

Refer to the Boot ROM section in the Datasheet and MWSDK documents

DESIGN NOTE: FLASH DEVICE SELECTION

- Read and fast read used by Flash controller, once configured
- Boot ROM uses common commands for READ/ERASE/WRITE
  - 0x03 (READ), 0xC7 (ERASE), 0x02 (PROG)
- “Basic” features used by Flash controller and boot ROM UART boot
- “Additional” features include USB boot (for 88MW322 only) and Flash programming

Winbond W25Qxx family validated
Devices from other suppliers support necessary commands for “Basic” features

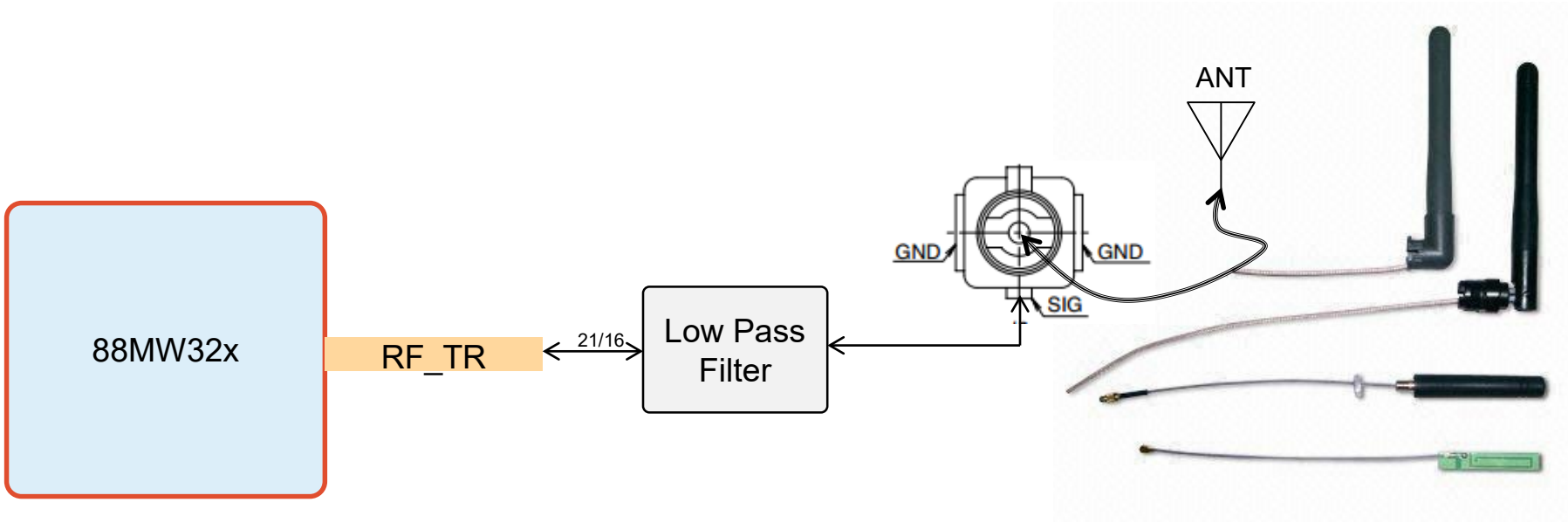
Command	Basic	Additional
Read Electronic ID	0xAB	
Write Enable	0x06	
WE for Volatile Status Register		0x50*
Read Status Register-1	0x05	
Read Status Register-2		0x35
Write Status Register		0x01
Page Program		0x02
Quad Page Program		0x32
Sector Erase (4KB)		0x20
Chip Erase	0xC7	
Continuous Read mode Reset		0xFF
Read Data	0x03	
Fast Read		0x0B
Fast Read Dual Output		0x3B
Fast Read Quad Output		0x6B

* Winbond specific

Table 62: SPI Flash for Basic Flash Boot Function

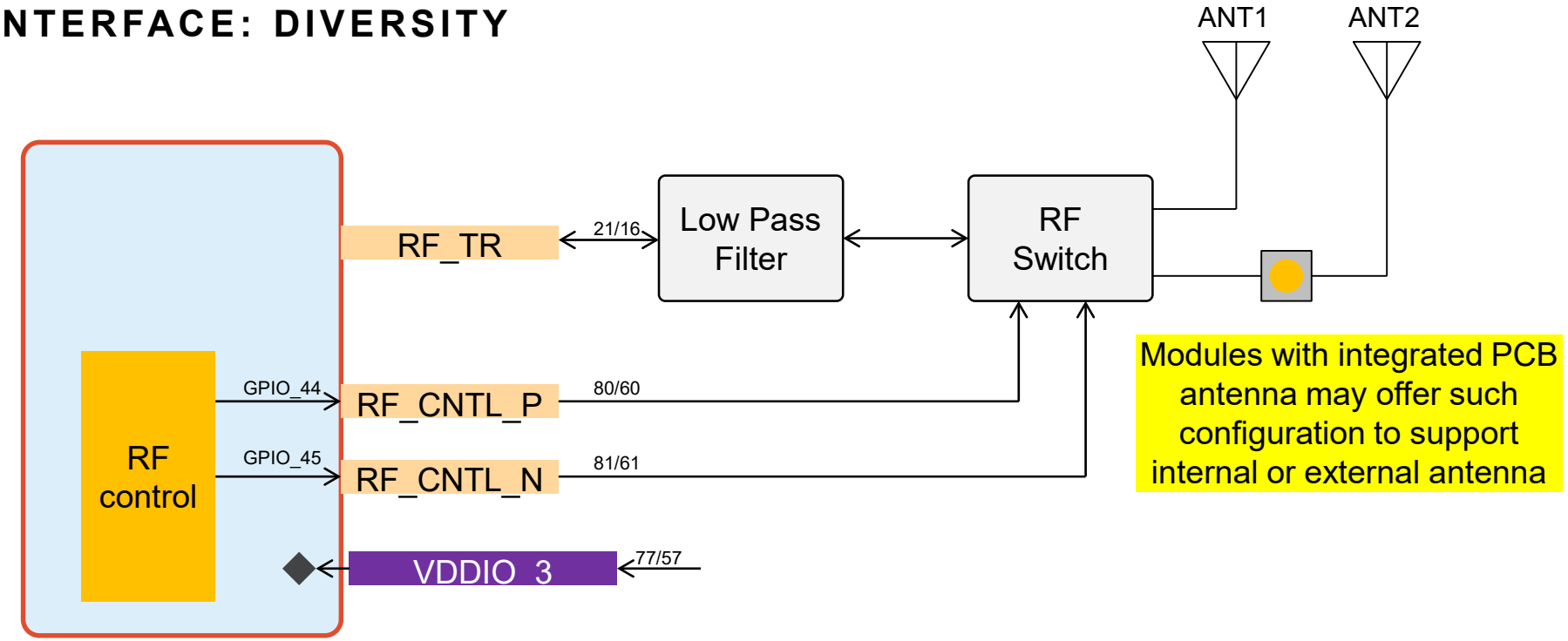
Company	Part Number
WINBOND	W25Q80BV
EON	EN25F80
ATMEL	AT25DF081
MXIC	MX25L8005
SPANSION	S25FL008A
ST	M25P80
AMIC	A25L080
GIGADEVICE	GD25Q80

SINGLE ANTENNA CONNECTOR



- 88MW32x RX_TR (antenna) pin through a low pass filter can be directly connected to a u.FL, w.FL, or other RF connector
- With external antenna or a separate internal PCB antenna, flexibility for RF testing and calibration can be easily carried out by using the same low cost connector

ANTENNA INTERFACE: DIVERSITY



- External RF Switch – SPDT (Single Pole, Double Throw) control support is provided through GPIO_44 and GPIO_45 for Antenna Diversity
  - Differential or direct signal configuration can be used
- Plan VDDIO_3 bias voltage to support the RF Switch requirements (typically 3.3V or 1.8V choice) and other GPIO in the group

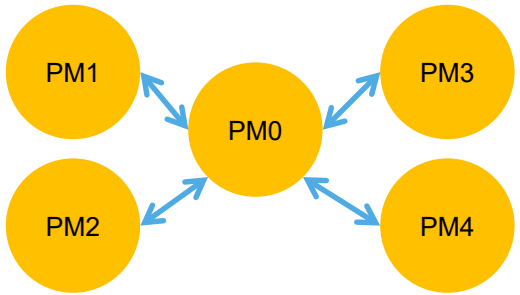
OPERATING MODES: APPLICATION PROCESSOR

Subsystem	PM0 Active	PM1 Idle	PM2 Standby	PM3 Sleep	PM4 Shutoff
Cortex-M4F	C0 (Run)	C1 (Idle)	C2 (Standby)	C3 (Off)	C3 (Off)
SRAM	M0 (Run)	M0 (Run)	M2 (Standby)	M2 (Standby)	M3 (Off)
Flash	Active standby (CSn=H)	Active standby	power-down (reduce leakage)	off	off
RTC	on	on	on	on	on
Peripherals	on: selective clock gating	on: selective clock gating	state retentive	off	off
Main XTAL	on/off	on/off	on/off	off	off
SFLL	on/off	on/off	on/off	off	off
AUPLL	on/off	on/off	on/off	off	off

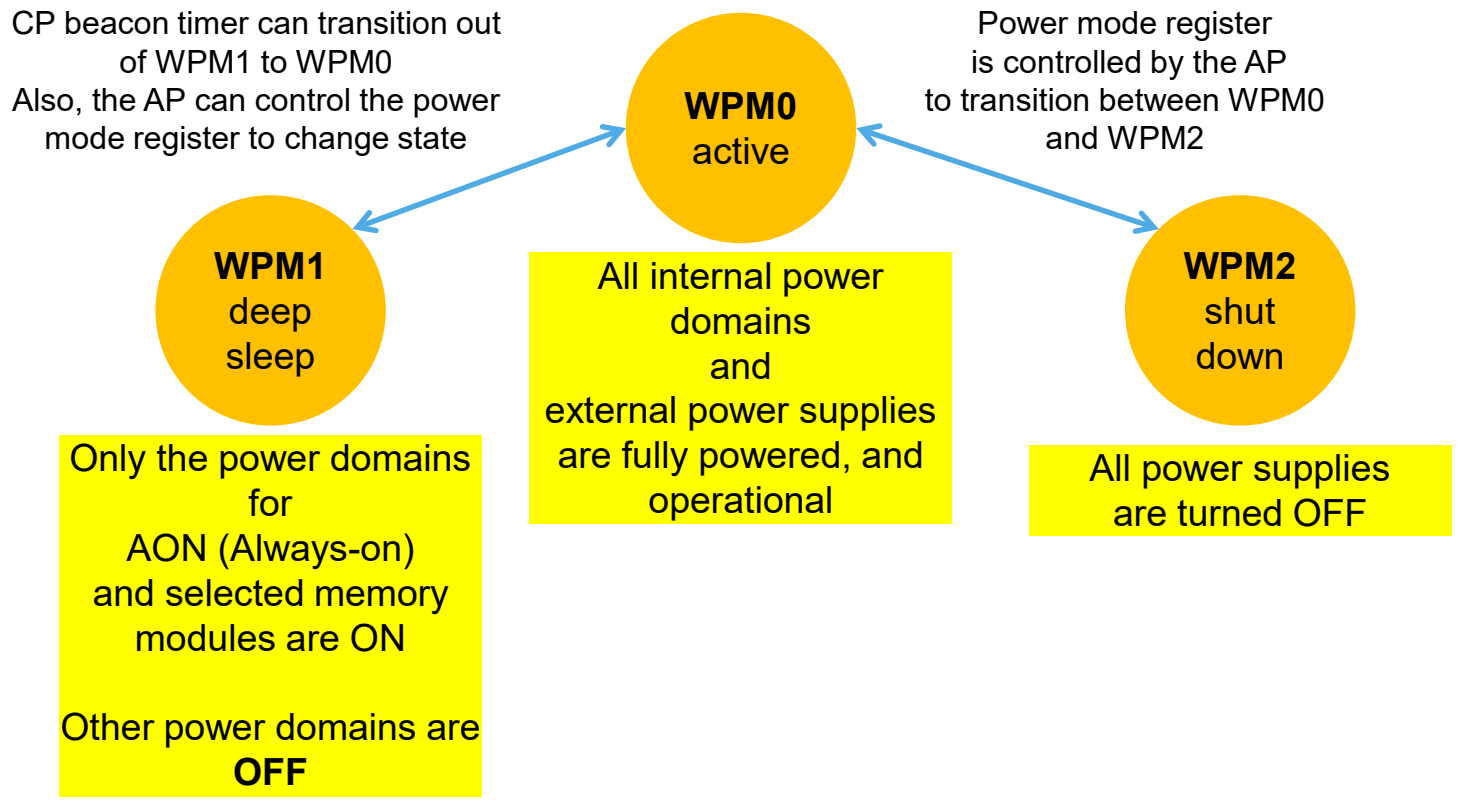
HCLK = AHB-Lite system clock.
- Can be gated off during sleep mode

FCLK = Free running clock (in same phase as HCLK)
- Must be running to generate edge trigger interrupt

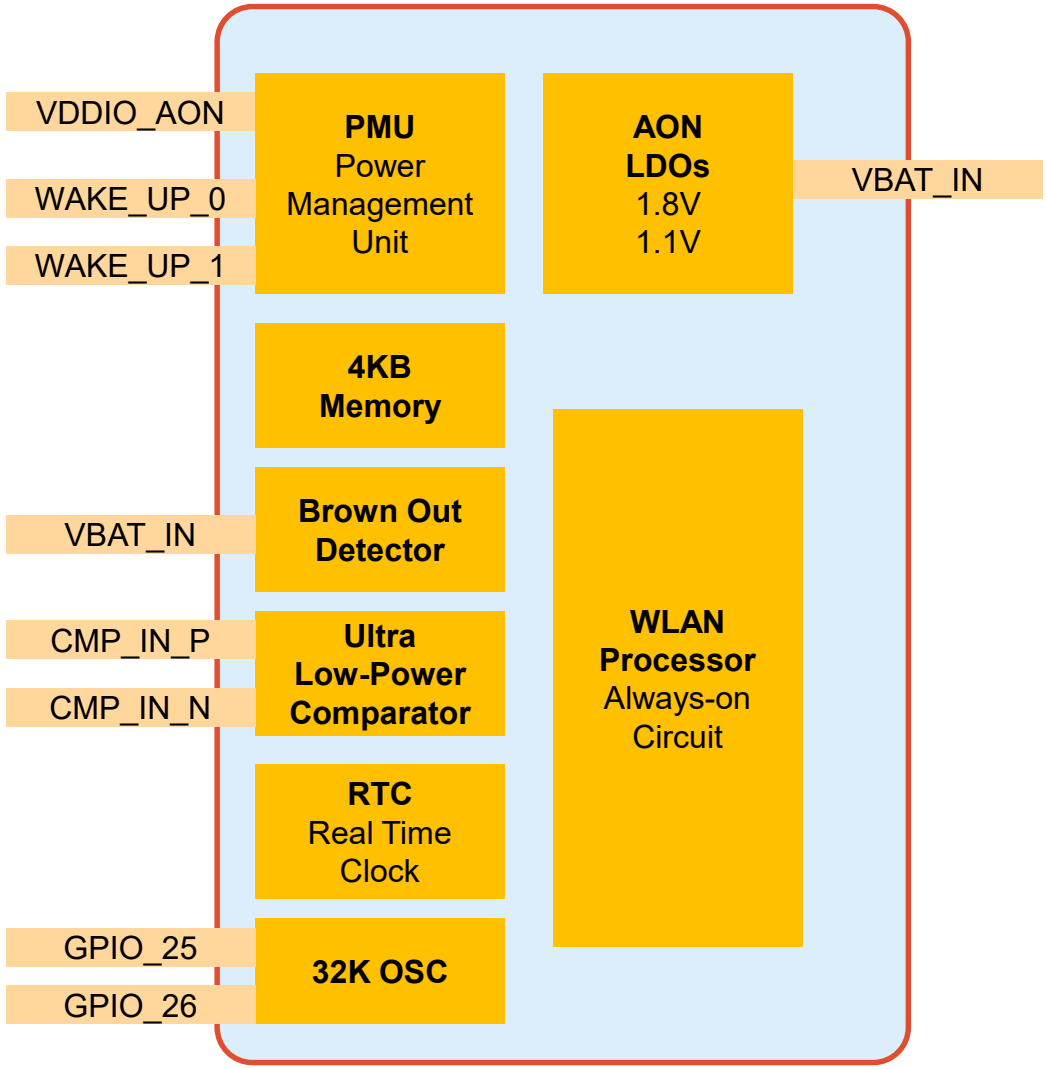
Cortex-M4 State	HCLK/FCLK
Run	on/on
Idle	off/on
Standby	off/off (State retention)
Off	Power Removed



OPERATING MODES: COMMUNICATION PROCESSOR



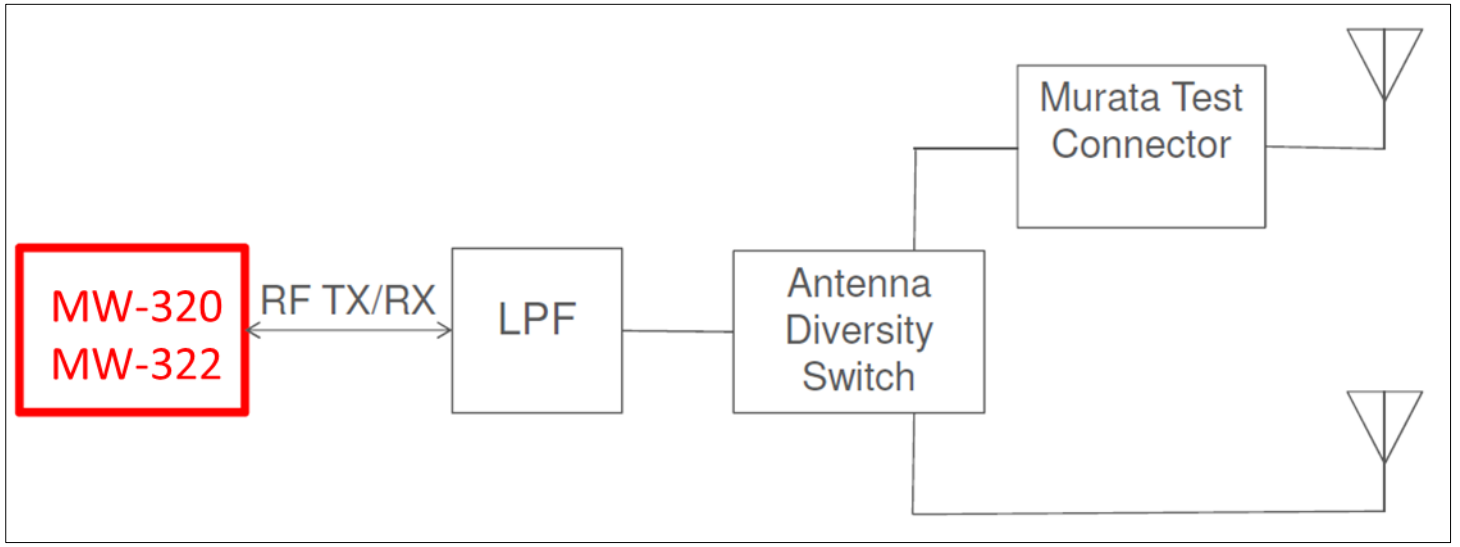
ALWAYS-ON CIRCUIT AND POWER SAVING FEATURES



- Always-on domains for applications processor and communications processor can be independently managed
- Dedicated internal LDOs power the AON circuits
- Wake-up sources
  - WAKE_UP_0/1 input
  - RTC timeout
  - Ultra low power comparator

WI-FI PERFORMANCE TESTING SETUP

- Platform: RD-88MW322-QFN-1B-2A_V1
  - Measurements carried out on this platform
- Test conditions
  - All RF parameters at 88MW320/322 RF_TR pin
  - Typical RF front-end loss (pin to antenna) is 1.5 dB
  - Minimum/maximum values over temperature, voltage and frequency
    - Temperature → -40° to +85°C
    - Voltage → 1.8V +/- 5% to 3.3V +/- 10%
    - Center frequency → 2.412 to 2.472 GHz



Single PCB Design

SECURE CONNECTIONS
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35

SINGLE PCB DESIGN

- Reasons for Chip-on-Board (CoB) design considerations
  - Module-based design not possible
    - Physical shape or size of product
    - Power topology requirement not supported by available modules
  - Cost reduction for high volume with single PCBA
  - Business requirements
    - Barrier to competition
    - CoB design reuse by OEM/ODM for multiple products
- Capabilities (in-house or access to)
  - RF design and testing
  - Regional certification
- Key considerations
  - RF: Low pass filter (LPF), antenna diversity switch
  - Power supply topology

BAND PASS / LOW PASS FILTER

- Reference
  - Vendor: TDK
  - Part number: DEA162450BT-1298A1
- LPF or BPF
  - Low Pass Filter (LPF) sufficient to control 2nd and 3rd harmonic emission where co-existence is not an issue
  - Consider Band Pass Filter (BPF) to attenuate frequency below the Wi-Fi band for co-existence with cellular and other RF communication
- Key parameters to consider
  - Insertion loss
  - Characteristic impedance
  - Pass band ripple
  - Stop band ripple : Especially at 2nd and 3rd harmonic frequencies
  - Roll off rate for band pass filter, particularly at lower end of the pass band

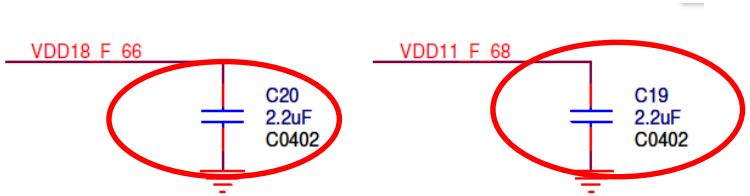
RF SWITCH FOR ANTENNA DIVERSITY

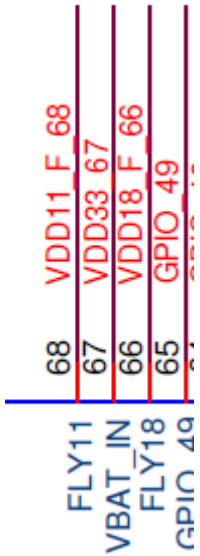
- Reference for RF SPDT switch
  - Vendor: Skyworks
  - Part number: SKY13323-378LF
- Key parameters to consider
  - Input power
  - Insertion loss
  - P1dB compression point
  - Characteristic impedance
  - Need for external DC blocking capacitors
- Control signal voltage (3.3V vs. 1.8V)
  - GPIO_[44:45] differential pair used for switch control with bias on VDDIO_3
    - Ensure other GPIO in the group can operate at selected bias
  - Confirm appropriate RF switch characteristics

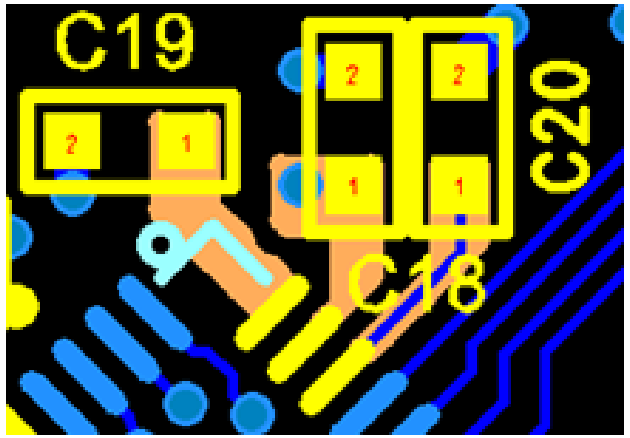
POWER TOPOLOGY CONSIDERATIONS

- Support for different power sources
  - Wi-Fi PA, logic domain 1.8V and 1.1V, analog domain 1.8V
- Support for different VDDIO groups
  - SPI Flash at 1.8V
  - Digital interfaces at 1.8V or 2.5V or 3.3V
  - Analog at 1.8V or 2.5V or 3.3V

LAYOUT GUIDELINE: PMIP VDD18 AND VDD11 FLY CAP

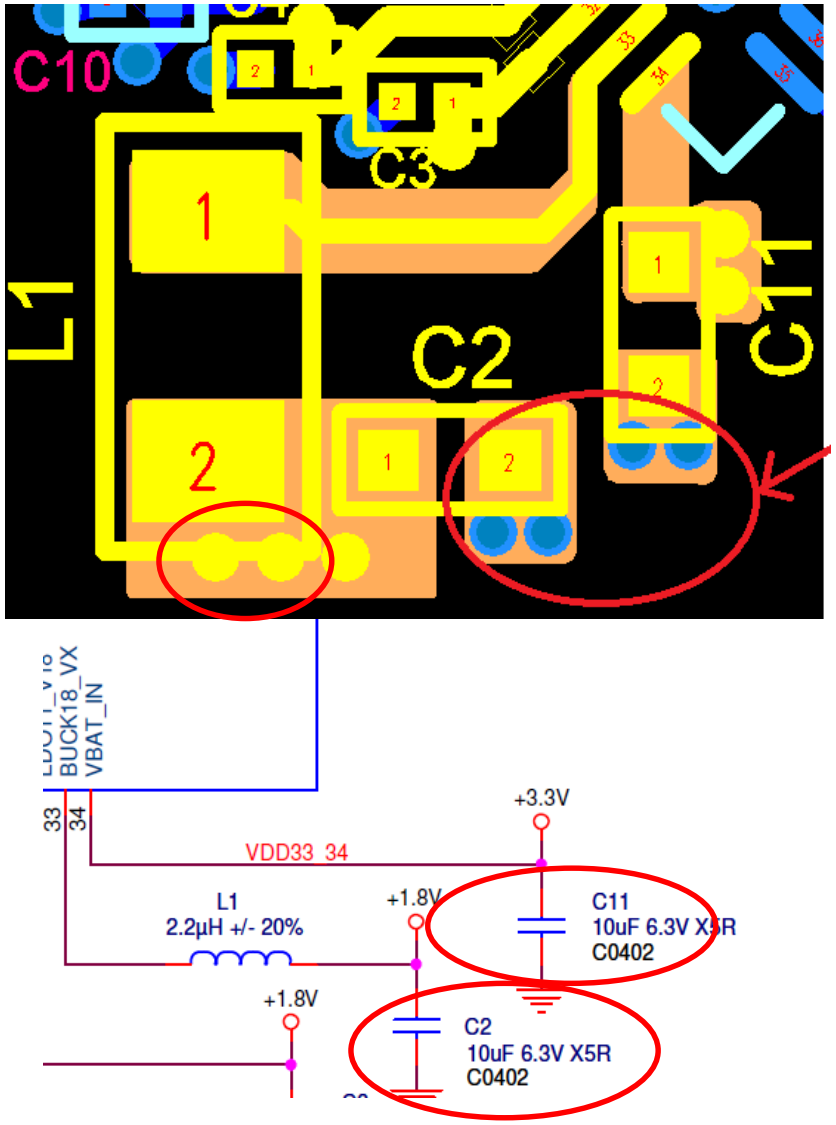






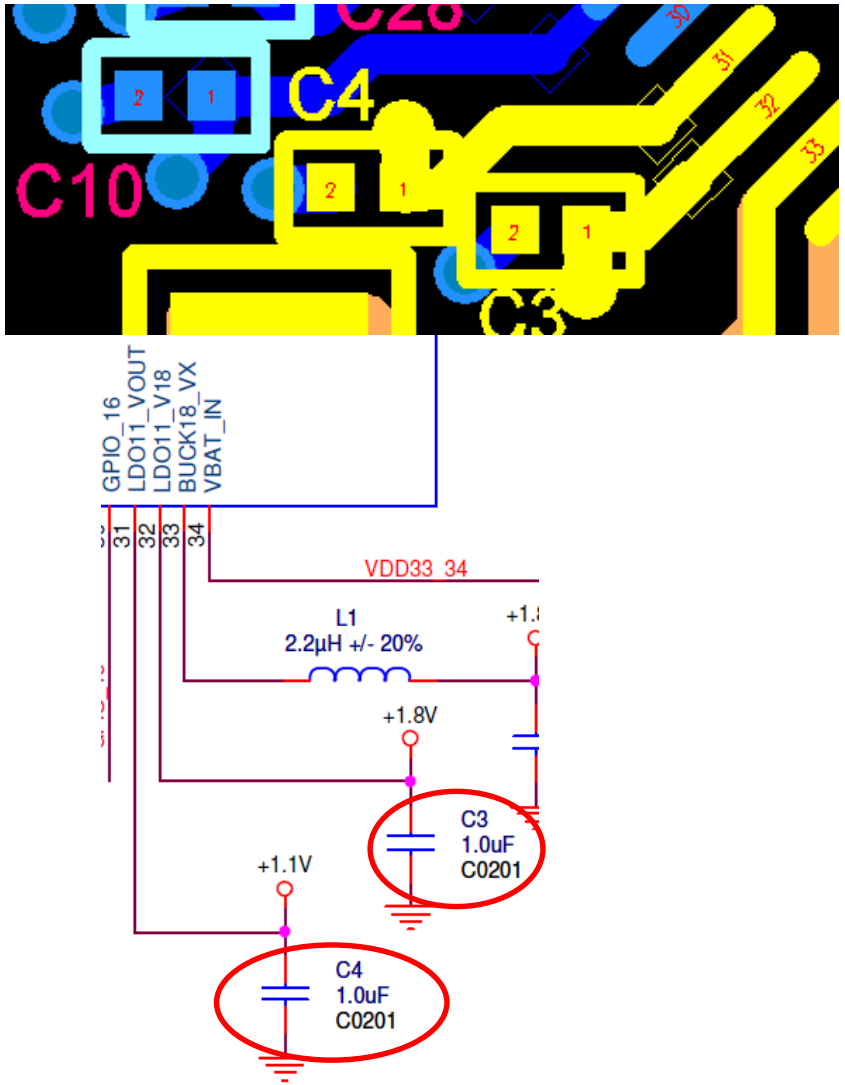
- Decoupling capacitors
  - External CAP for LDO18 (PMIP)
    - C20 value 2.2uF
    - Keep as close as possible to pin 66
  - External CAP for LDO11 (PMIP)
    - C19 value 2.2uF
    - Keep as close as possible to pin 68

LAYOUT GUIDELINE: PSU BUCK18



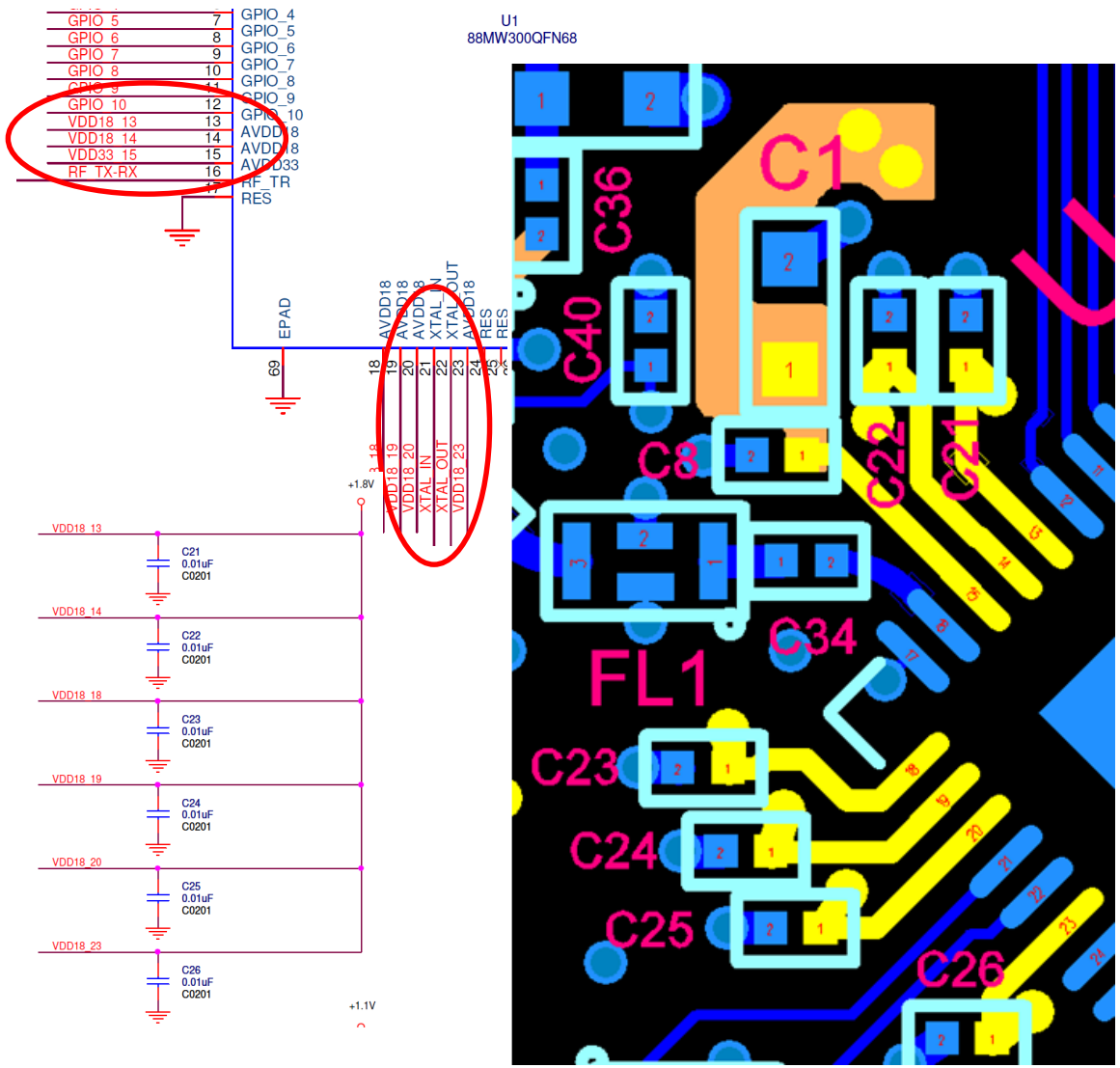
- Decoupling capacitors for PSU
  - Input CAP
    - C11 value 10uF X5R
    - Input power rail → CAP → pin 34
    - Two via from input power plane
    - Two via to GND
  - Output CAP
    - C2 value 10uF X5R
    - Two via to GND
  - Keep GND via for input and output CAPs as close as possible
- Power inductor
  - Two via to 1.8V power plane

LAYOUT GUIDELINE: PSU LDO11



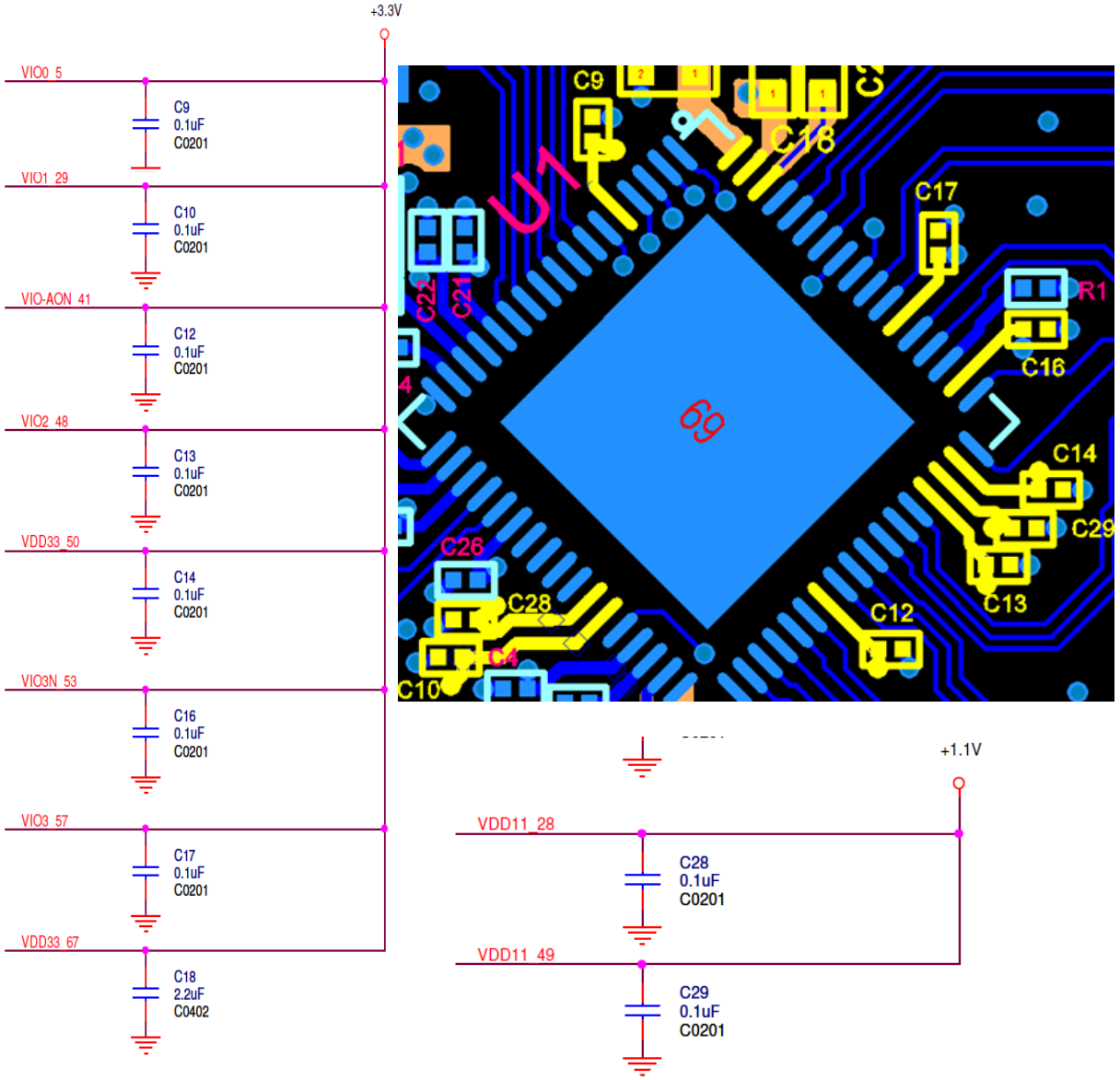
- Decoupling capacitors for PSU
  - Input CAP
    - C3 value 1.0uF
    - 1.8V power plane → CAP → pin 31
  - Output CAP
    - C4 value 1.0uF
    - Pin 32 → CAP → 1.1V power plane
    - 1.1V power plane → VDD11 pins

LAYOUT GUIDELINE: AVDD18, AVDD33 D-CAPS



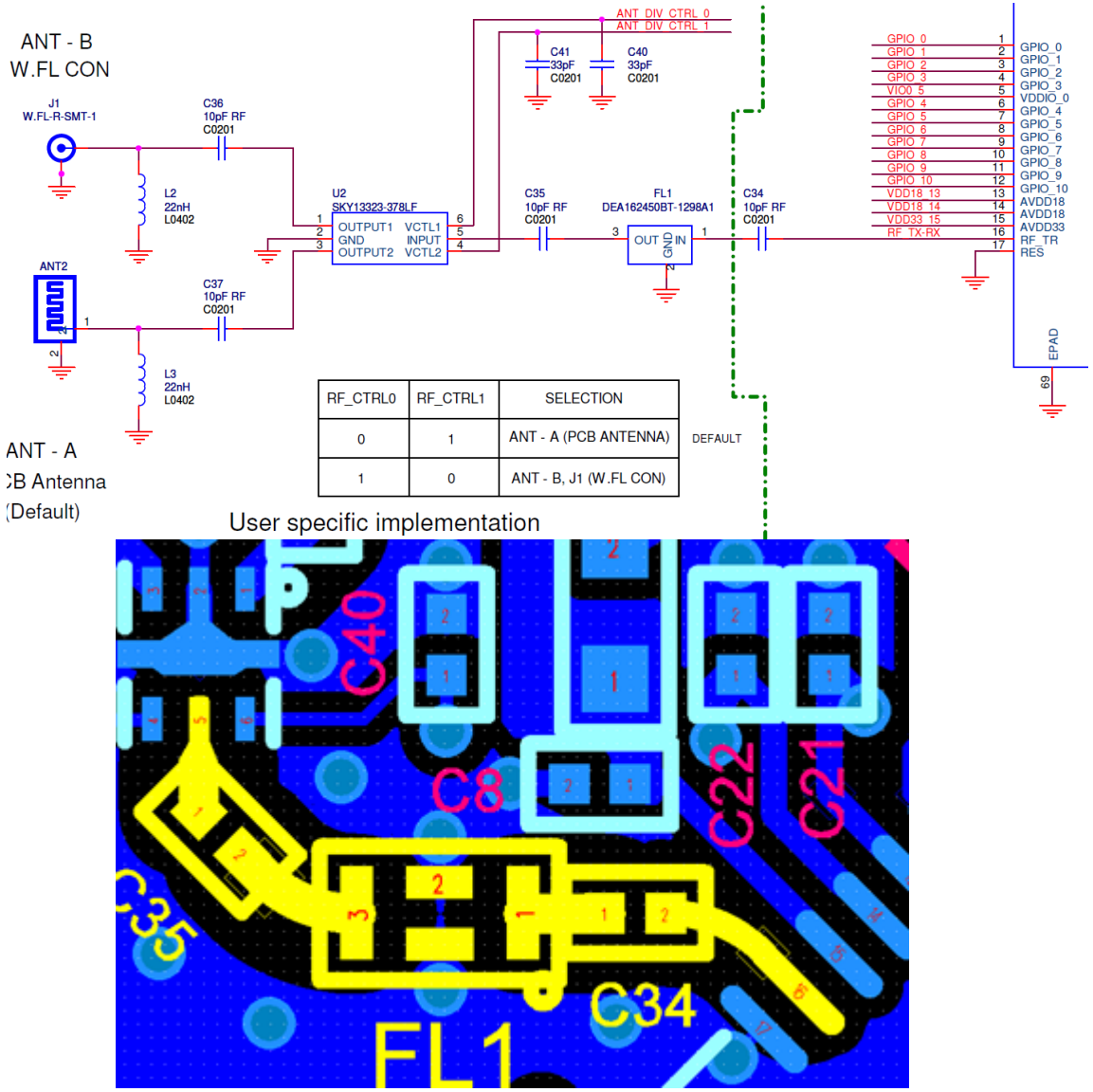
- Decoupling capacitors
  - AVDD18 for RF Unit (RFU) and Common Analog Unit (CAU)
    - C21 to C26 value 0.01uF
    - Shortest path from power plane to Capacitor through via, and then to the MW32x AVDD18 pins
  - AVDD33 for PA
    - C1 value 10uF
    - Minimum 2 via from power plane
    - Shortest path to pin from CAP

LAYOUT GUIDELINE: VDDIO AND VDDD11 D-CAPS



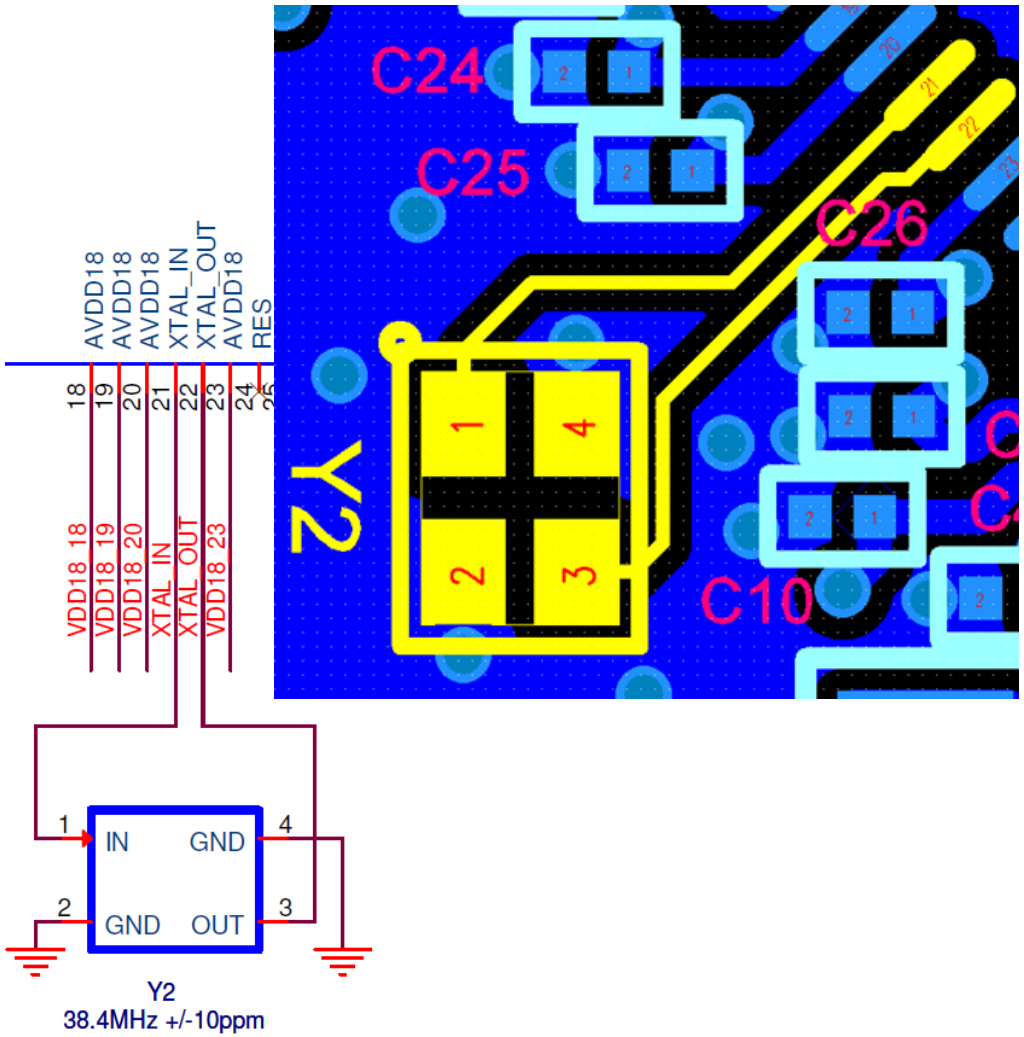
- Decoupling capacitors C[9,10,12,13,14,16,17,18] for each VDDIO_x should be connected to the pins [5,29,41,48,50,53,57,67] as close as possible
- VDD11 power on pins 28 and 49 should have decoupling capacitors C28 and C29 as close as possible
- The via from the power plane should first connects to the CAP and then the trace to the pin

LAYOUT GUIDELINE: RF



- Pay attention to:
  - Impedance control : 50 Ω
  - Noise coupling
  - Emission
  - Ground plane
  - Trace bend
- Solid GND plane under RF
  - GND on top layer around RF trace with sufficient stitching vias
- Place C34 as close as possible to RF_TR pin
- Isolate RF trace from high frequency digital signals and power lines to avoid coupling with them
- Avoid routing RF trace with sharp corners, a smooth arch is suggested

LAYOUT GUIDELINE: USB



- Crystal should be placed as close to chip as possible
- Crystal lines should be as short as possible
- Crystal should be placed as far away as possible from RF section and antenna
- Avoid noise coupling
  - GND plane under crystal and its in/out signal traces
  - No power or signal on any layer underneath crystal or its in/out lines

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