AN13594

PCA9460 application note

Rev. 1 — 6 April 2022 **Application note**

Document information

Information	Content
Keywords	PCA9460, I.MX 8ULP, PMIC
Abstract	This application note discusses the critical items needed in designing the PMIC PCA9460 in portable devices with an i.MX 8ULP application processor. It gives a guideline for component selection, placement, and routing the trace.

Revision history

Rev	Date	Description
1	20220406	Initial version

1 Introduction

The PCA9460 is a single chip Power Management IC (PMIC) specifically designed for 8ULP processor. It provides power supply solutions for low power wearable application where size and efficiency are critical.

The device provides four high efficiency step-down regulators, four LDOs, one 10 mA SNVS LDO, and four load switches.

Each buck regulator has ultra low Iq current to reduce standby current. Two buck regulators support smart Dynamic Voltage Scaling (DVS). Five LDOs have 300 nA low quiescent current. One LDOs is for SNVS core power supply, one 250 mA NMOS LDO is to regulate to low output voltage from buck regulator output. Three 250 mA PMOS LDOs are purposed to supply power to process and peripheral devices. Four 150 mΩ load switches are to switch power for peripheral device and also they can be configured to LED driver with two different blink modes.

This device is characterized across -40°C to 85°C ambient temperature range.

PCA9460 has three OTP versions:

- PCA9460A is companion PMIC for i.MX 8ULP + LPDDR4
- PCA9460B is companion PMIC for i.MX 8ULP + LPDDR4X
- PCA9450C is companion PMIC for i.MX 8ULP + LPDDR3

The PCA9460 is offered in 42-bumps Wafer level CSP package, 2.86 mm x 2.46 mm, 0.4 mm pitch.

1.1 Features and benefits

- Four Buck regulators
  - Two 1 A buck regulators
  - Two 1 A buck regulator with DVS
  - Low Iq (1.5 µA at low power mode, 5.5 µA at normal mode)
- Five linear regulators
  - One 250 mA NMOS LDO
  - Three 250 mA PMOS LDO
  - One 10 mA SNVS LDO
  - Built-in active discharge resistor
- Four Load Switches with active discharge resistor
  - 150 mΩ Rdson
  - ON/OFF control in different modes
  - Configurable to LED driver with two blink patterns
- Power control IO
  - Power ON/OFF control
  - Standby/Run mode control
  - Smart DVS control
- Flexible power ON/OFF sequence
- Fm+ 1 MHz I2C Interface
- ESD protection
  - Human Body Model (HBM) : ± 2000 V
  - Charged Device Model (CDM) : ± 500 V
- 7 x 6 bump array, 0.4 mm pitch, WL-CSP, 2.86 mm x 2.46 mm

2 Block diagram

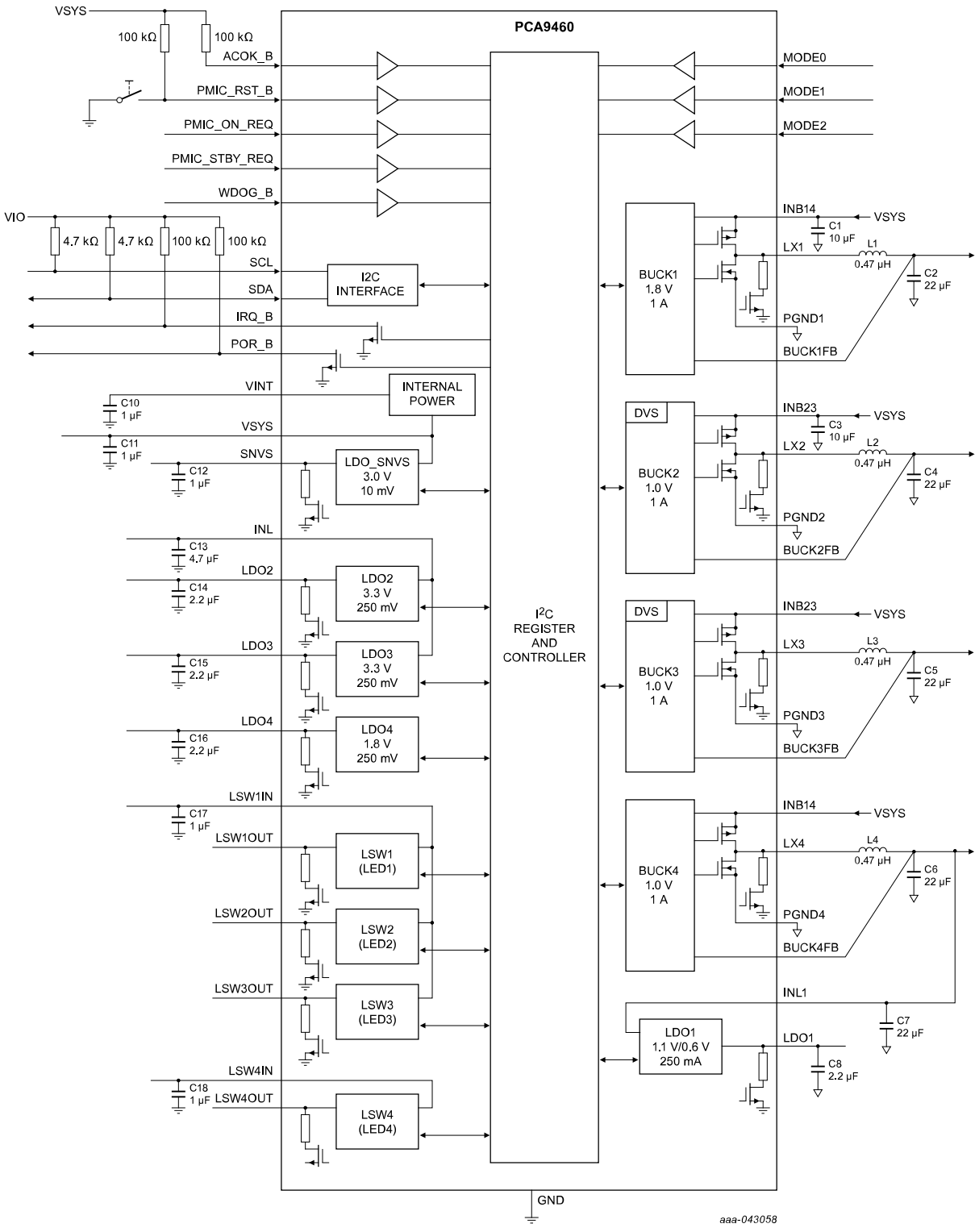


Figure 1. Block diagram

3 PCA9460 Selection guide

Table 1. PCA9460 Selection guide

Partnumber	AP + Memory Platform	Buck4	LDO1
PCA9460A	i.MX 8ULP + LPDDR4	1.1V	1.1V
PCA9460B	i.MX 8ULP + LPDDR4X	1.1V	0.6V
PCA9460C	i.MX 8ULP + LPDDR3	1.2V	1.2V

4 Application design-in information

4.1 Reference schematic

PCA9460 reference schematic with i.MX 8ULP is illustrated in Figure 2.

This serves a guide on how the output voltage rails on PCA9460 would be typically connected to the corresponding voltage domains on i.Mx8ULP and external components such as the memories (DDR and or EMMC/SDHC). This is not a mandatory configuration and the customer has flexibility to make adjustments as long as the voltage and sequencing requirements for the processor are respected and are supported by the PCA9460 variant.

Refer to the corresponding i.Mx 8ULP EVK for detailed design information and schematic/layout source files.

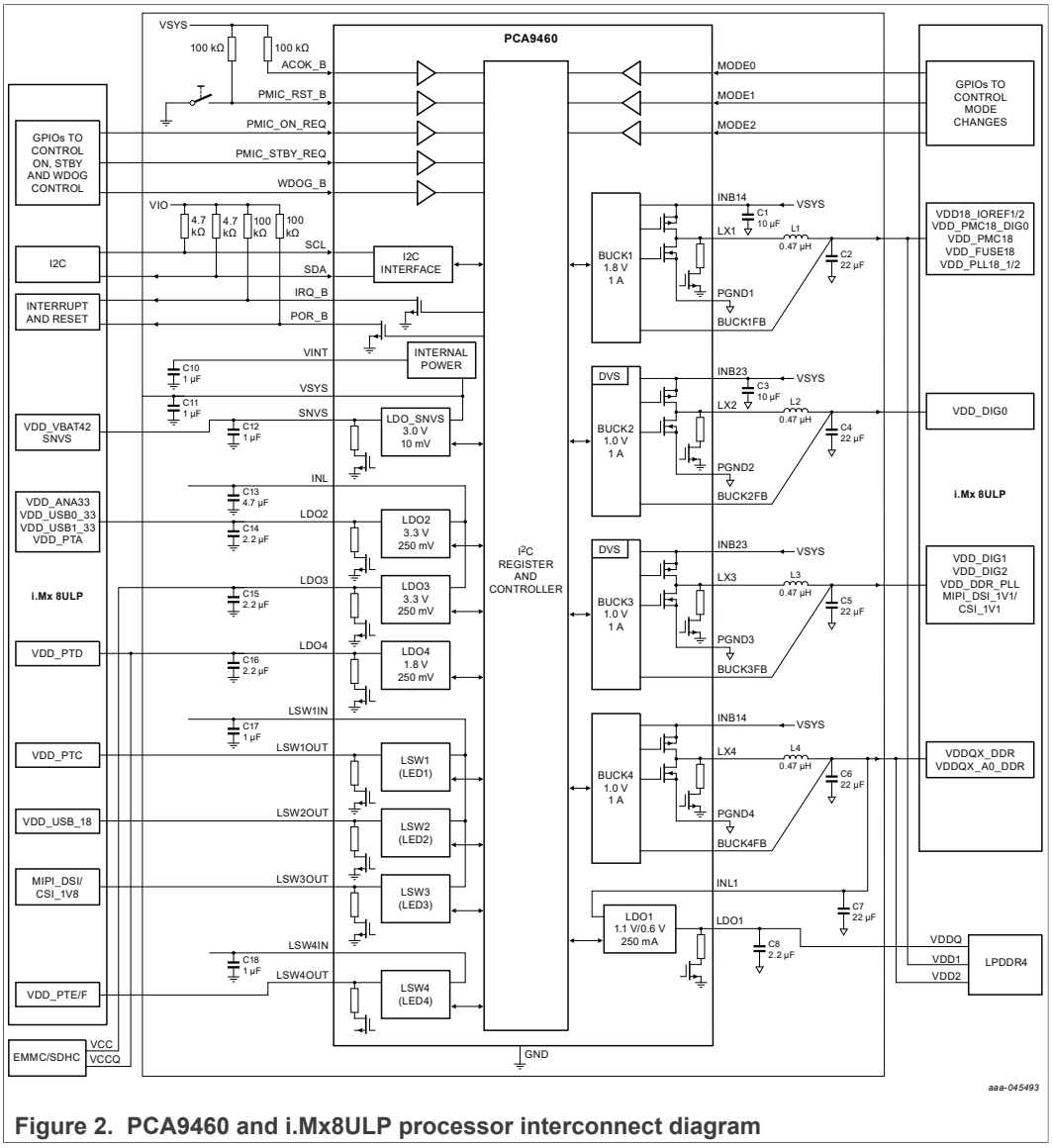


Figure 2. PCA9460 and i.Mx8ULP processor interconnect diagram

4.2 Typical application

The PCA9460 devices have only a few design requirements. Use the following parameters for the design

- 1 µF bypass capacitor on VINT and VSYS, located as close as possible to those pins to ground
- Input capacitors must be present on the INB and INL supplies if used
- Output inductors and capacitors must be used on the outputs of the BUCK converters if used
- Output capacitors must be used on the outputs of the LDOs

4.2.1 Inductor selection for buck converters

Each of the converters in the PCA9460 typically use a 0.47 µH output inductor which has to be rated for its DC resistance and saturation current. The DC resistance of the

inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest DC resistance must be selected for highest efficiency.

Equation 1 calculates the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current as calculated with Equation 2. This is needed because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin.max}}{L \times f} \quad (1)$$

$$I_{L.max} = I_{out.max} + \frac{\Delta I_L}{2} \quad (2)$$

Where:

- f = switching frequency (2 MHz)
- L = Inductance
- ΔI_L = Peak to peak inductor ripple current
- $I_{L.max}$ = Maximum inductor current

A conservative approach is to select the inductor current rating just for the maximum switch current of the PCA9460.

Table 2 shows the recommended inductors.

Table 2. Recommended inductors

Buck	Vendor	Part number	Inductance [uH]	Size [mm]	DCR [mΩ]	Isat [A]	Irat [A]
BUCK1, BUCK2, BUCK3, BUCK4	Murata	DFE201210S-R47M	0.47	2012	32	4.8	3.4
	Littelfuse	LPWI201210HR47T	0.47	2012	28	4.9	4.3

4.2.2 Output capacitor selection for buck converters

The fast response adaptive constant ON time control scheme of the buck converters implemented in the PCA9460 allows the use of small ceramic capacitors with a typical value of 22 µF for each converter without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. See Table 3 for recommended the capacitor.

Table 3. Recommended capacitor

BUCK	Vendor	Part number	Capacitance [uF]	Size [mm]	Voltage [V]
BUCK1, BUCK2, BUCK3, BUCK4	Murata	GRM158C80G226ME	22	1005	4
	Kyocera AVX	04024W226MAT2A	22	1005	4

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. Just for completeness, the RMS ripple current is calculated in Equation 3.

$$I_{RMS.COUT} = \text{Vout} \times \frac{1 - \frac{\text{Vout}}{\text{Vin}}}{\text{L} \times \text{f}} \times \frac{1}{2\sqrt{3}} \quad (3)$$

At nominal load current, the inductive converters operate in PWM mode. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta \text{Vout} = \text{Vout} \times \frac{1-\frac{Vout}{Vin}}{\text{L} \times \text{f}} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (4)$$

Where:

- The highest output voltage ripple occurs at the highest input voltage Vin.

When load currents are light, the converters operate in PFM mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1 % of the nominal output voltage.

4.2.3 Input capacitor selection for buck converters

Low ESR input capacitor is highly recommended for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes because of the nature of buck converter. Each DC-DC converter requires a 10 µF ceramic input capacitor on its input pins. The input capacitor could be increased without any limit for better input voltage filtering. See Table 4 for recommended capacitor.

Table 4. Recommended capacitor

BUCK	Vendor	Part number	Capacitance [uF]	Size [mm]	Voltage [V]
BUCK1, BUCK2, BUCK3, BUCK4	Murata	GRM188R60J106ME	10	1608	6.3
	Samsung	CL10A106MQ8NN	10	1608	6.3

4.2.4 VSYS, VINT, LDO_SNVS and LSWxIN capacitor selection

Internal power input, internal power supply output, secure non-volatile storage LDO and load switch input pins are all required to be bypassed by a low ESR 1 uF ceramic capacitor. Table 5 shows the recommended capacitor.

Table 5. Recommended capacitor

PIN	Vendor	Part number	Capacitance [uF]	Size [mm]	Voltage [V]
VINT, VSYS, LDOSNVS, LSWxIN	Murata	GRM188R60J106ME	1	1005	16
	Samsung	CL10A106MQ8NN	1	1005	16

5 Design guidelines

5.1 Package

The PCA9460 device is intended for use in commercial and industrial applications and is offered in a small package 42-bump WLCSP. Refer to Application Note AN10439 (https://www.nxp.com/webapp/Download?colCode=AN10439&location=null) for guidelines on the handling and assembly of NXP WLCSP packages during PCB assembly, guidelines for PCB design and rework, and package performance information (such as Moisture

Sensitivity Level (MSL) rating, board level reliability, mechanical, and thermal resistance data).

Package dimensions are provided in package drawings. To find the most current package outline drawing, you should look directly into the package link: https://www.nxp.com/packages/SOT1459-7.

5.2 Placement

It is desirable to keep all component related to the power stage as close to the PMIC as possible, specially decoupling input and output capacitors.

Place these components as close as possible to the IC in order of priority:

- Input capacitor of the buck regulators
- LDO capacitors
- VSYS and VINT capacitors
- Buck regulator inductors
- Buck regulator output capacitors

The layout guide is shown in Figure 3.

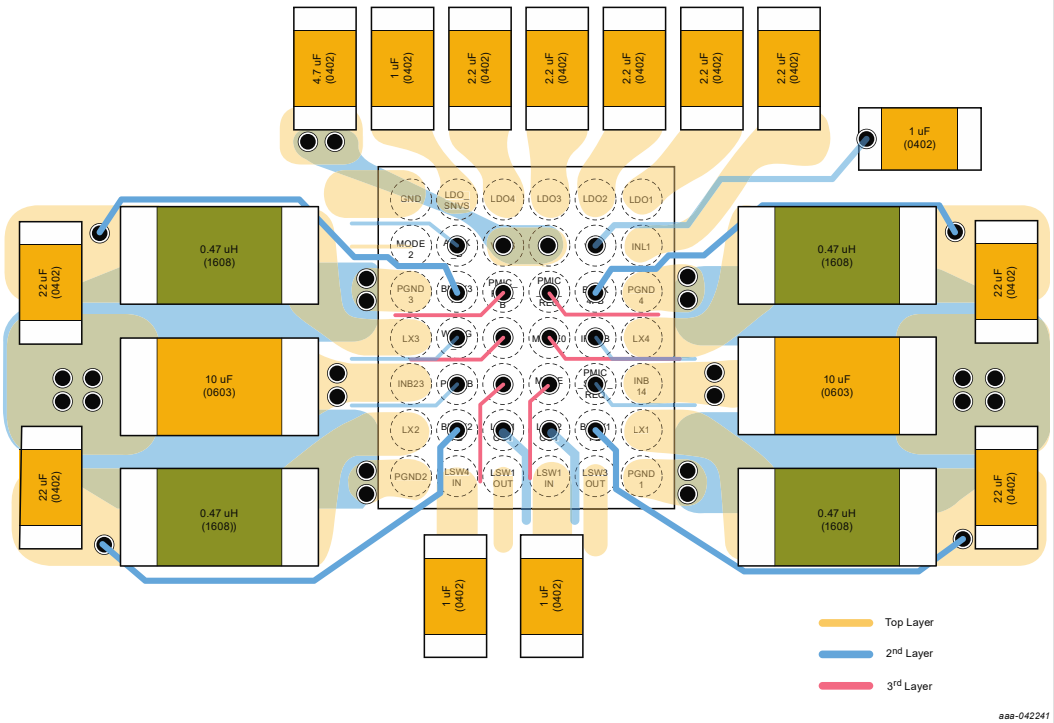


Figure 3. PCA9460 Layout

5.3 Switching regulator schematic recommendations

Figure 4 shows the critical path in buck converter which has high di/dt.

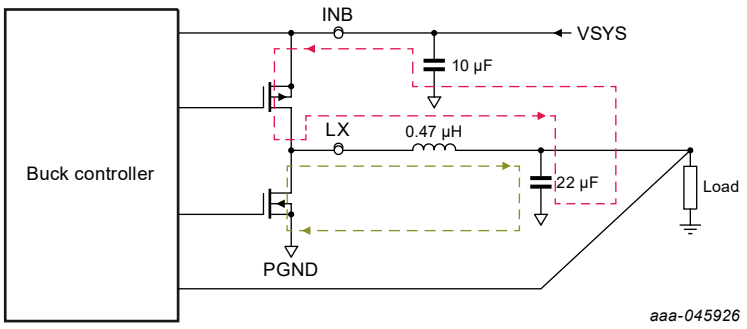


Figure 4. Buck schematic

The biggest challenge in buck layout is EMI. To minimize the EMI requires the minimum loop area of two high di/dt path as shown in Figure 4. The area in red is input power charging the inductor when high side FET is on; the area in green is inductor discharge energy to output capacitor (load) when low side FET is on.

5.4 Layout guidelines

5.4.1 General routing requirements

- Some recommended things to keep in mind for manufacturability:
  - Via in pads require a 4.5 mil minimum annular ring. Pad must be 9.0 mils larger than the hole
  - Maximum copper thickness for lines less than 5.0 mils wide is 0.6 oz copper
  - Minimum allowed spacing between line and hole pad is 3.5 mils
  - Minimum allowed spacing between line and line is 3.0 mils
- Care must be taken with BUCKxFB pins traces. These signals are susceptible to noise and must be routed far away from power, clock, or high power signals, like the ones on the INBxx, and LXx pins. They could be also shielded.
- Shield feedback traces of the regulators and keep them as short as possible (trace them on the bottom so the ground and power planes shield these traces).
- Make sure all components related to a specific block are referenced to the corresponding ground.

5.4.2 Parallel routing requirements

I2C signal routing

- SCL is one of the fastest signal of the system, so it must be given special care.
- To avoid contamination of these delicate signals by nearby high power or high frequency signals, it is a good practice to shield them with ground planes placed on adjacent layers. Make sure the ground plane is uniform throughout the whole signal trace length.

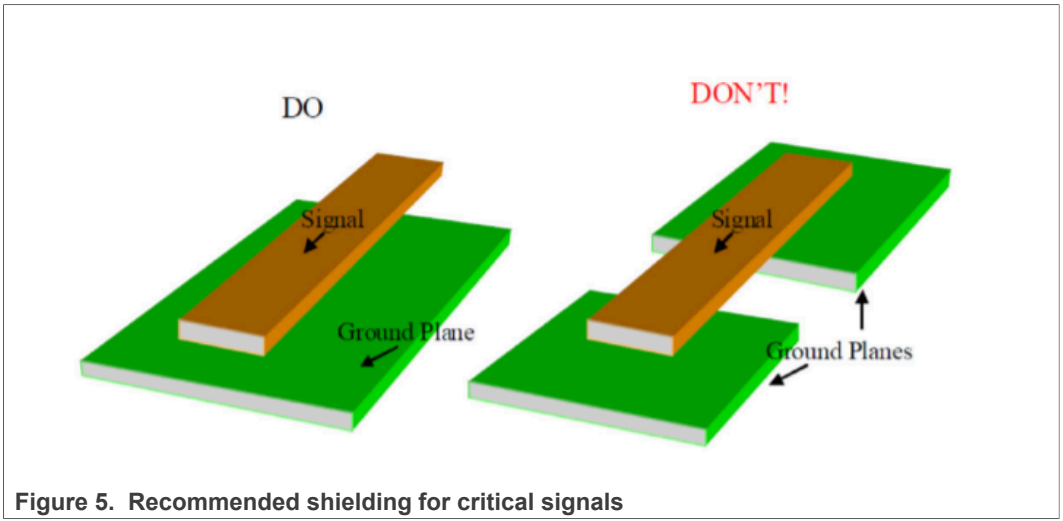


Figure 5. Recommended shielding for critical signals

- These signals can be placed on an outer layer of the board to reduce their capacitance with respect to the ground plane.
- Care must be taken with these signals not to contaminate analog signals, as they are high frequency signals. Another good practice is to trace them perpendicularly on different layers, so there is a minimum area of proximity between signals.

5.4.3 Switching regulator layout recommendations

1. Put the input/output capacitor and inductor as close to chip as possible to minimize the loop area. If using the high frequency bypass capacitor to filter the EMI, make sure this high frequency capacitor is close to the chip.

2. Make high-current ripple traces low-inductance (short, high W/L ratio).

3. Make high-current traces wide or copper islands.

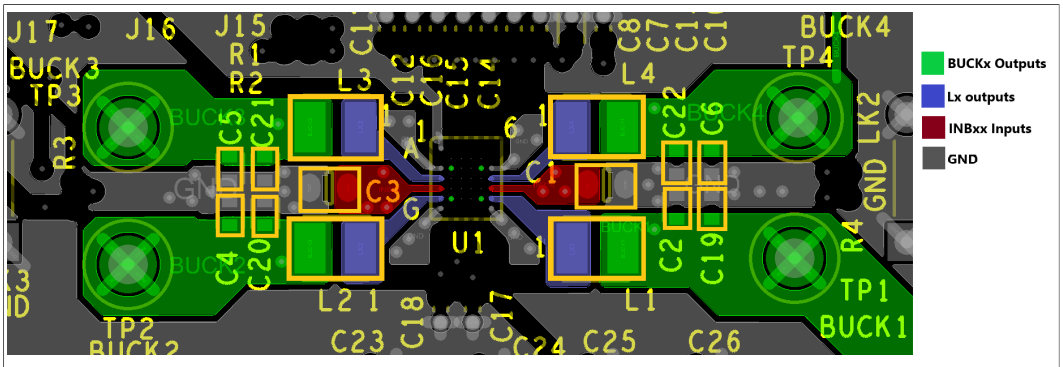


Figure 6. Layout example for buck regulators

6 EMC results for Evaluation board

Provided as a reference only, the FCC EMC results for our evaluation board (part number: KIT-PCA9460-EVB) demonstrate the appropriate EMC performance for this device for three main categories: conducted emissions, radiated emissions and radiated immunity. The table below shows a summary of those results. More detailed information can be provided on demand through our customer support channels.

Table 6. FCC EMC results

Description of test item	Standard	Limits	Results
Emissions			
Conducted disturbance at the main supply terminals	EN 55032:2015+A11:2020	Class A	Pass Class A
Radiated disturbance		Class A	Pass Class A
Powerline conducted emissions	47 CFR FCC Part 15 Subpart B ANSI C63.4-2014	15.107(b) Class A	Pass Class A
Radiated Emissions (30-1000 MHz)		15.109(b) Class A	Pass Class A
Immunity (EN 55035:2017+A11:2020)			
Radio-frequency, Radiated Immunity	IEC 61000-4-3:2006+A1:2007+A2: 2010	A	Pass

7 Thermal analysis calculation

7.1 Rating data

Junction-to-Ambient Thermal Resistance Nomenclature: the JEDEC specification reserves the symbol RθJA or θJA (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in a natural-convection environment. RθJMA or θJMA (ThetaJMA) is used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated that the generic name, Theta-JA, continues to be commonly used. The JEDEC standards can be consulted at http://www.jedec.org.

7.2 Estimation of junction temperature

An estimation of the chip junction temperature TJ can be obtained from the equation:

$$TJ = TA + (R\theta JA \times PD) \quad (5)$$

with:

TA = Ambient temperature for the package in °C

RθJA = Junction-to-ambient thermal resistance in °C/W

PD = Power dissipation in the package in W

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board RθJA and the value obtained on a four-layer board RθJMA. Actual application PCBs show a performance close to the simulated four-layer board value. Although, this performance might be somewhat degraded in the case of significant power dissipated by other components placed close to the device.

8 Practical Efficiency results for PCA9460

Figure 7 shows practical results for the buck regulator´s efficiency under various conditions. A key aspect to consider is that the efficiency is kept at a very good level

throughout the different loading conditions. This capability is thanks to the automatic switching between pulsed frequency modulation (PFM) and pulsed width modulation (PWM), depending on the loading conditions. With very good efficiency levels (higher than 80 %) even at very light loads such as 1 mA.

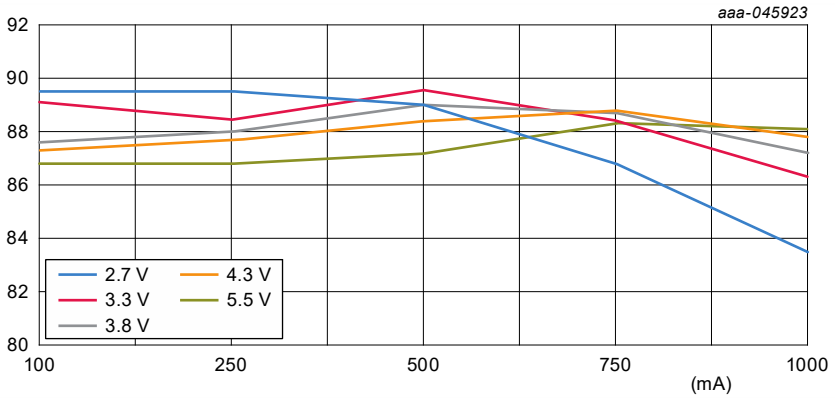


Figure 7. Efficiency curves for Vout = 1.8 V for different Vsys inputs

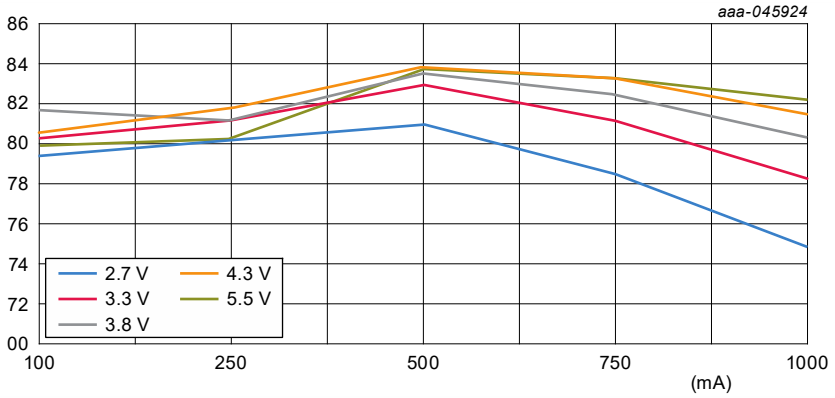


Figure 8. Efficiency curves for Vout = 0.9 V for different Vsys inputs

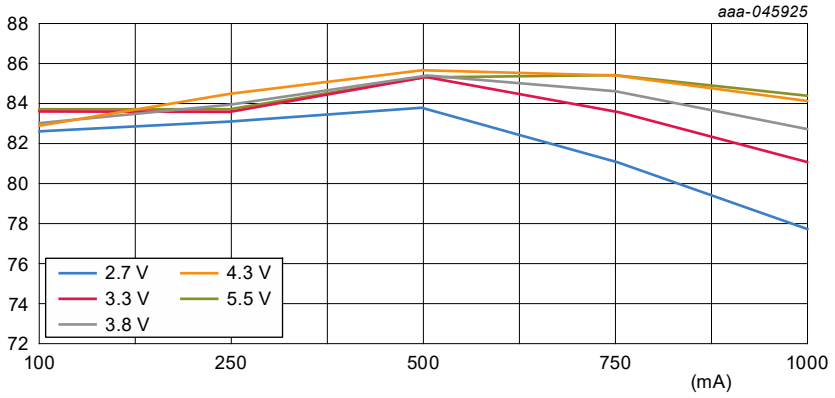


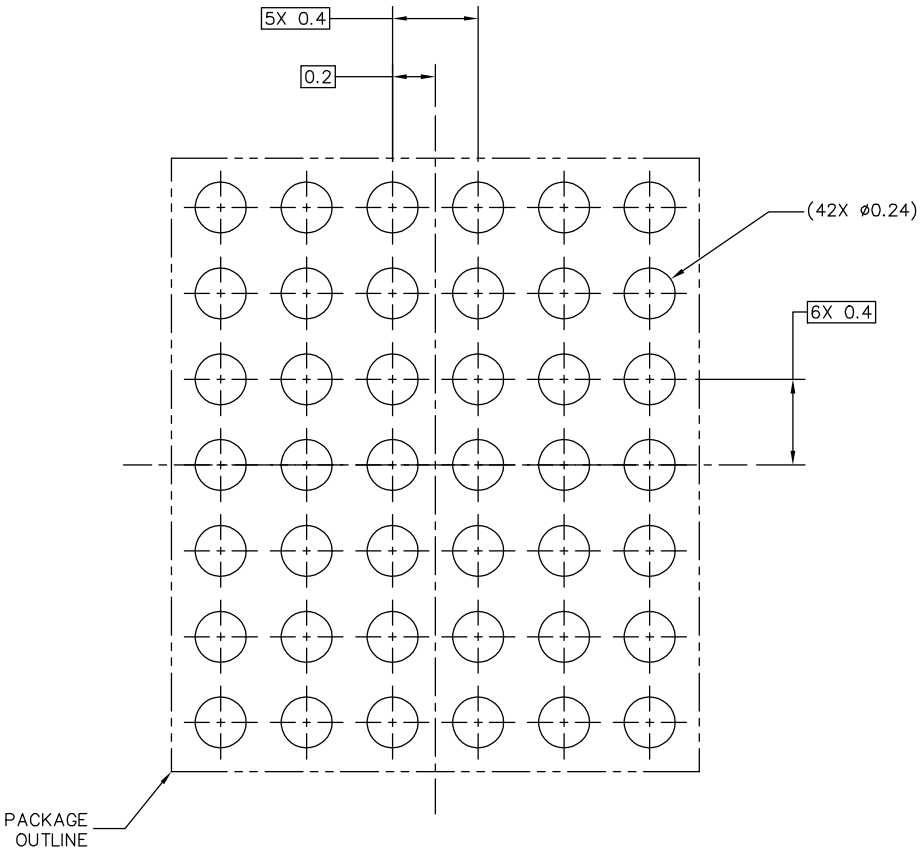
Figure 9. Efficiency curves for Vout = 1.1 V for different Vsys inputs

9 PCB design guidelines

Package dimensions are provided in package drawings. To find the most current package outline drawing, click on https://www.nxp.com/packages/SOT1459-7.

WLCSP−42 I/O
2.86 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1459−7



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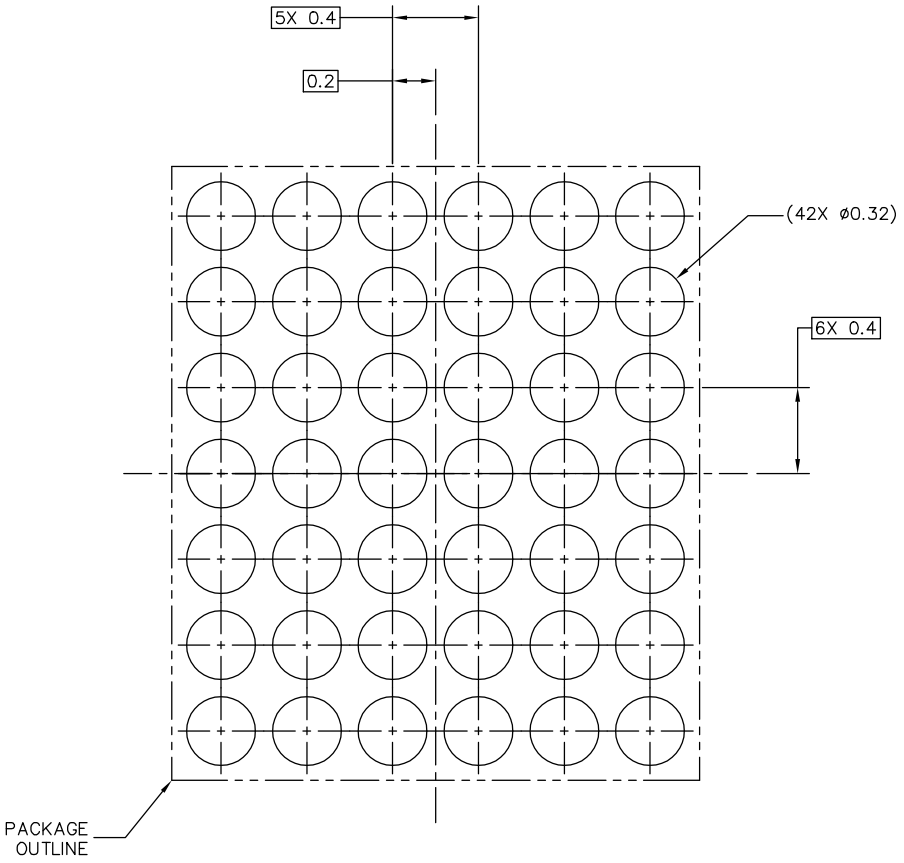
SOT1459−7



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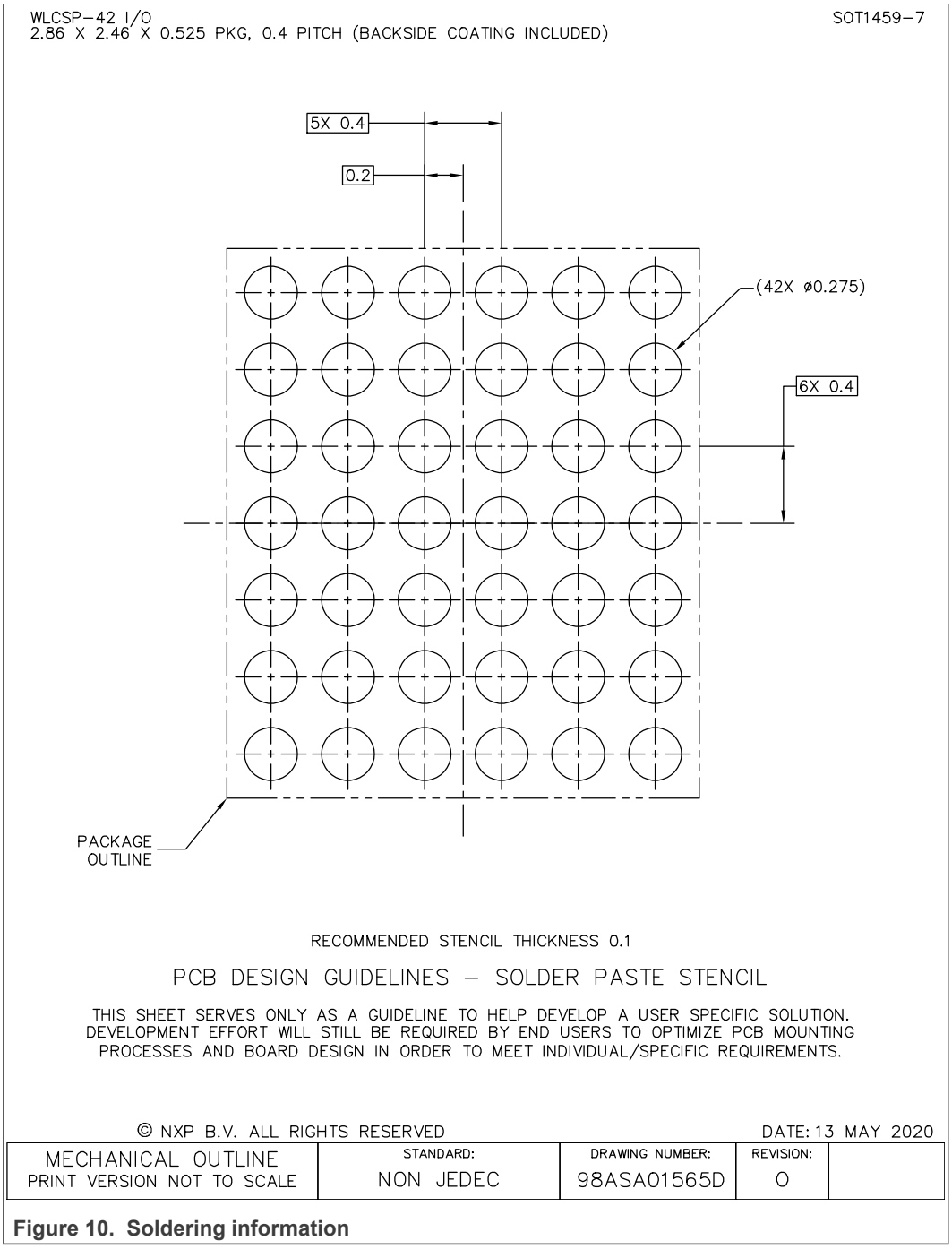

Figure 10. Soldering information

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