AN13656

Assembly guidelines for Flip Chip plastic ball grid array and chip scale package

Rev. 1 — 1 September 2022 Application note

Document information

Information	Content
Keywords	FCBGA, FCCSP, FCPBGA, Flip Chip, PCB, thermal guidelines, assembly, soldering, printed circuit board
Abstract	This document provides guidelines for the handling and board mounting of FCBGA and FCCSP packages, including recommendations for printed-circuit board (PCB) design, soldering, and rework. It also includes recommendations for thermal solutions.

Revision history

Rev	Date	Description
1	20220901	Initial release combines AN4871 and AN1850 into this single document. AN4871 and AN1850 will be archived.

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1 Introduction

This application note provides guidelines for the board assembly, handling and application of thermal management solutions for Flip Chip plastic ball grid array (FCPBGA) and Flip Chip chip-scale package (FCCSP) components.Semiconductor components are electrical (ESD) and mechanical sensitive devices.

These guidelines include proper precautions for handling, packing and processing FCPBGA and FCCSP components.

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2 Scope

This document contains generic information that encompasses various NXP FCPBGA and FCCSP packages assembled internally or at external subcontractors. Specific information about each device is not provided. To develop a specific solution, actual experience and development efforts are required to optimize the assembly process and application design per individual device requirements, industry standards (such as IPC and JEDEC), and prevalent practices in the assembly environment. For more details about the specific devices contained in this note, visit https://www.nxp.com/ or contact the appropriate product application team.

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3 FCPBGA and FCCSP packages

3.1 FCPBGA package description

Flip Chip Plastic ball grid array (FCPBGA) packages feature a semiconductor die or chip, which is flipped so that the active side of the device faces the package substrate. A device may have one of three FCPBGA configurations, which are listed in the table below.

In the lidless configuration, exposure of the chip's backside allows for direct contact between the chip and heat sink, which improves the overall thermal performance of the chip. Note that, because the chip's backside is exposed, the engineer must exercise caution when placing the component on the printed circuit board, in testing operations, and applying a heat-sink solution. See relevant sections of this document for guidelines relevant to handling, assembly and thermal solutions for lidless flip chip packages.

While lidless packages achieve better thermal performance, flat- and full-lidded packages ease handling by providing a lid that both protects the die and distributes heat.

Table 1. FCPBGA configuration options

Configuration Name	Characterized by...	Handling	Example
Lidless	No lid present	Exercise caution when placing the component on the printed circuit board and when applying a heat-sink solution.	Underfill Flip chip solder bump Capacitor Package substrate BGA solder ball FBGA621 aaa-046744
Flat-lidded	Lid covers die	Avoid impact to lid. Applying uneven force, or bonding heat-sink to lid, can damage the lid-to-chip bond. For more information, see Section 8.3	Lid/heat spreader Thermal interface material Flip chip solder bump Underfill Capacitor Package substrate BGA solder ball aaa-046745

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Table 1. FCPBGA configuration options*...continued*

Configuration Name	Characterized by...	Handling	Example
Full-lidded	Lid covers device	Lid protects the die. Bonded adhesive, capable of withstanding the force of the heatsink, couples the protective lid to the package substrate.	

3.2 FCCSP Package description

FCCSP packages, similar to FCPBGA, feature a semiconductor die or chip, which is flipped so that the active side of the device faces the package substrate. The semiconductor die is over-molded with epoxy mold compound. Therefore, the backside of the die is not exposed. Because of the mold compound on top of the die, FCCSP packages have higher junction-to-case temperatures than FCPBGA configurations.

Table 2. FCPBGA configuration options

Configuration Name	Characterized by...	Handling	Example
FCCSP	Overmolded Die	Generally, no special handling required. Since package is typically much thinner than FCPBGA, avoid excessive force during pick and place.	

3.3 Flip Chip package solder bump construction

NXP Flip Chip packages feature either a high-lead solder bump soldered to the package substrate with a eutectic tin-lead solder, a lead-free solder bump or a copper pillar with lead-free solder. The solder bump or copper pillar details are not specified in the device data sheet. However, any component containing lead will be indicated as such in the material content declaration.

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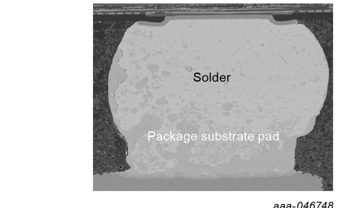

Figure 1. High-Lead Solder Bump

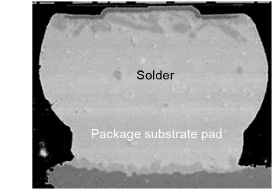

Figure 2. Pb-Free Solder Bump

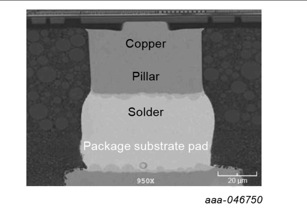

Figure 3. Copper Pillar

3.4 FCPBGA and FCCSP body sizes

The exact product package outline can be found under the “Package Quality” tab on the NXP.com product page.

3.5 Flip Chip package Pin A1 location

The pin A1 location on NXP devices may be indicated by a top-side marker and/or depopulated corner sphere or marker on the bottom-side. Examples of pin A1 markers are shown in Figure 4.

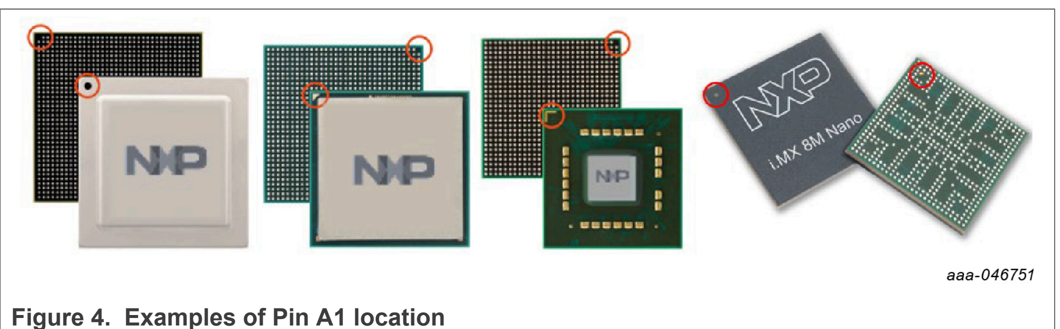

Figure 4. Examples of Pin A1 location

3.6 FCPBGA substrate construction

Most FCPBGA substrates feature high density interconnect (HDI) construction with build-up (BU) layers on both sides of a glass/epoxy core. Construction is typically designated by the number of build-up and core copper layers (BU-C-BU). For example, (3-2-3) construction is three build-up layers on both sides of a two-layer glass/epoxy core. See NXP package outline drawings for substrate thickness specifications.

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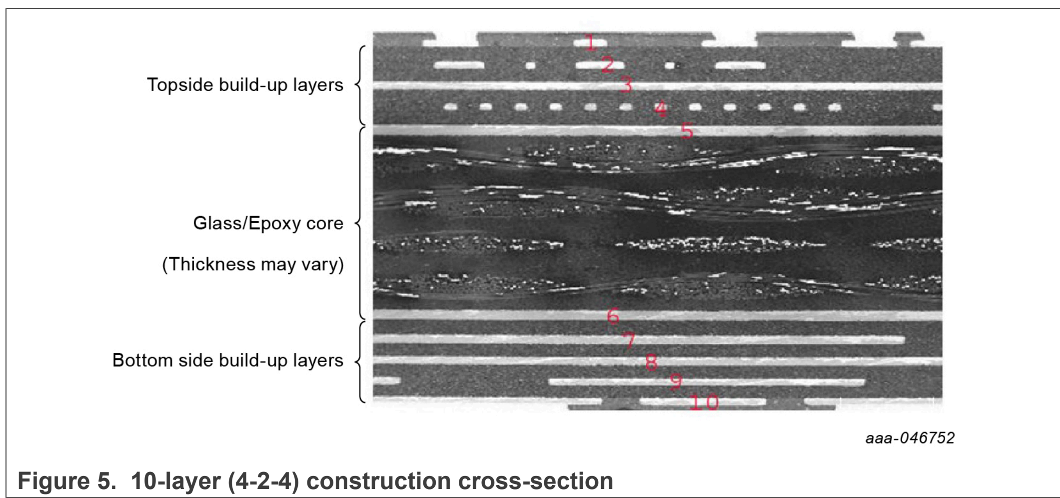

Figure 5. 10-layer (4-2-4) construction cross-section

3.7 FCCSP substrate construction

FCCSP substrates can be of the build-up variety similar to FCPBGA, or they can be of coreless construction, which is typically designated by the total number of layers. For example, 3L construction is three metal layers. See NXP package outline drawings for substrate thickness specifications.

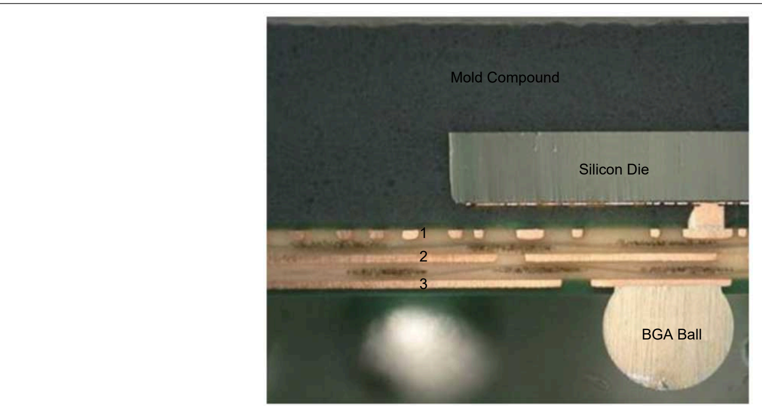

Figure 6. 3-layer coreless FCCSP cross section

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3.8 Example: BGA1313 lidded FCPBGA package drawing

SOT1899-1

BGA1313, ball grid array package, 1313 terminals, 0.75 mm pitch, 29 mm x 29 mm x 2.37 mm body

28 June 2019 Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	BGA1313
Package style descriptive code	BGA (ball grid array)
Package body material type	P (plastic)
Mounting method type	S (surface mount)
Issue date	04-06-2019
Manufacturer package code	98ASA00969D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	29	-	mm
package width	-	29	-	mm
package height	-	2.37	-	mm
nominal pitch	-	0.75	-	mm
actual quantity of termination	-	1313	-	

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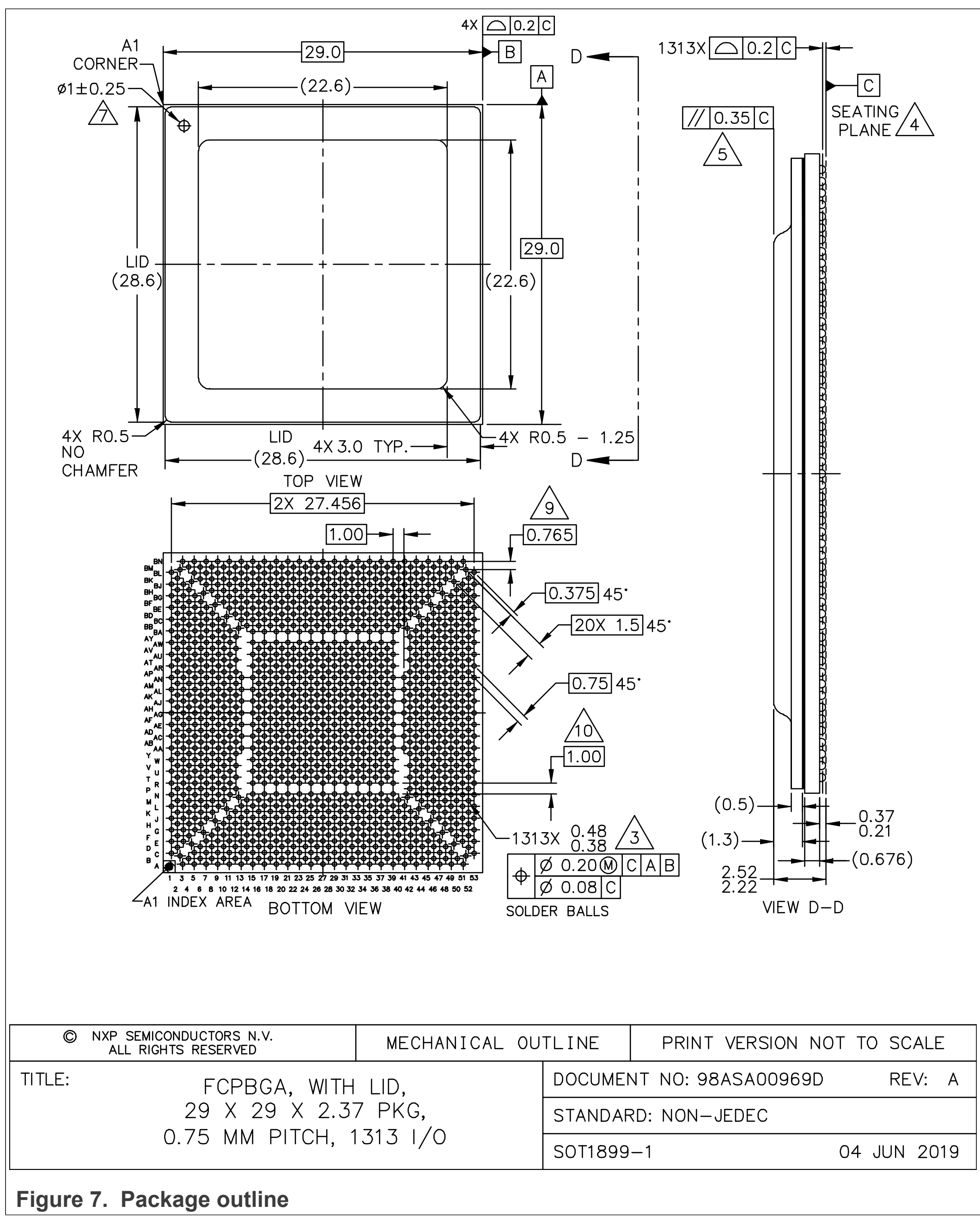

Figure 7. Package outline

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
4. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.
7. PIN 1 THRU HOLE SHALL BE CENTERED WITHIN FOOT AREA.
8. LID OVERHANG ON SUBSTRATE NOT ALLOWED.
9. EACH OF THE SIX BALLS IN THE FOUR DIAGONAL LANES BETWEEN DIE CORNER AND PACKAGE CORNER (24 TOTAL BALLS) ARE EQUAL DISTANCE TO THE FOUR CLOSEST SURROUNDING BALLS.
10. 1MM BALL CENTER TO BALL CENTER BETWEEN INNER ARRAY AND OUTER ARRAY FOR ALL FOUR SIDES.

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TITLE: FCPBGA, WITH LID, 29 X 29 X 2.37 PKG, 0.75 MM PITCH, 1313 I/O	DOCUMENT NO: 98ASA00969D	REV: A
	STANDARD: NON–JEDEC	
	SOT1899–1	04 JUN 2019

Figure 8. Package outline note

3.9 Component level qualification

Flip-Chip packages are typically qualified to industrial tier levels based on JEDEC specifications. In some cases, the package may be qualified to an AEC automotive grade. Refer to the product technical data sheet for specific qualification tier information. Most Flip-Chip packages are qualified to MSL3 at peak reflow of either 245 ºC or 260 ºC.

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4 Printed-circuit board (PCB) guidelines

See NXP application note AN10365 “Surface Mount Reflow Soldering” for guidelines for the board mounting and handling of NXP semiconductor surface mount packages.

4.1 Printed circuit board pad design guidelines and requirements for FCPBGA

In some cases, the package information document on nxp.com will include printed circuit board and solder stencil design guidelines. In the cases where these guidelines are included in the package information document, the package information document guidelines should take precedence over the guidelines in this document. NXP follows the generic requirements for Surface Mount Design and Land Pattern standards from the Institute for Printed Circuits (IPC), IPC-7351B[1].

4.1.1 PCB pad dimensions

In general, the printed circuit board (PCB) pad solderable diameter should match the package pad diameter. When required for routing, the motherboard pad diameter may be decreased by up to 10% versus the package pad.

4.1.2 PCB solder mask layer design

Non-soldermask defined (NSMD) pads

- Most common type of motherboard pad in the industry
- Typically results in the most consistent solderability, especially with hot air solder leveled (HASL) surface finish

Soldermask defined (SMD) pads

- Added strength provided by the solder mask overlap

NSMD motherboard pads are recommended for most applications. It is not recommended to mix NSMD and SMD pads, as this could lead to solder bridging.

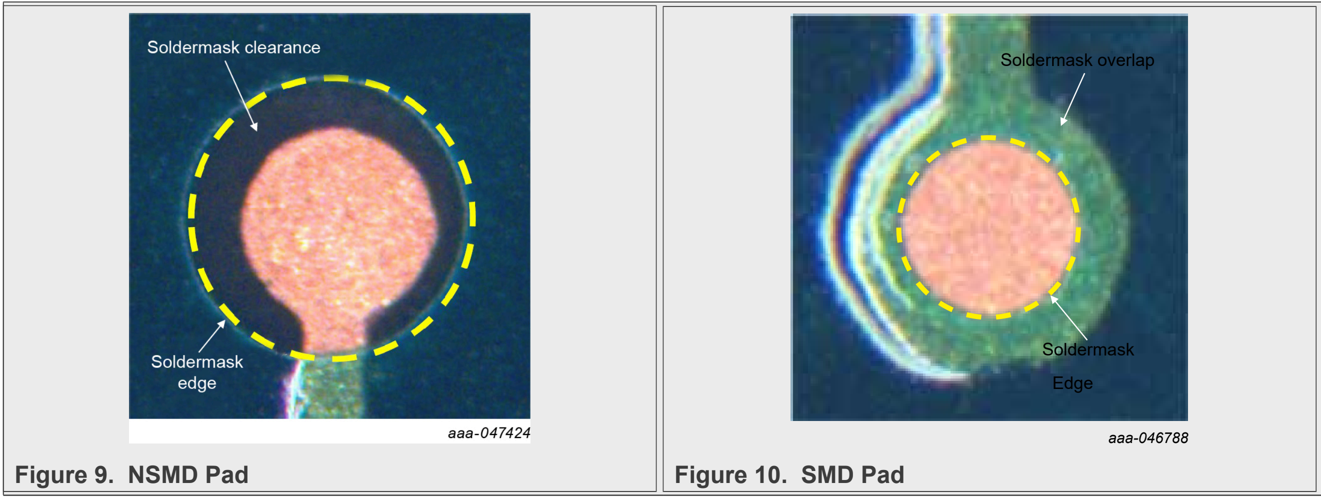

Figure 9. NSMD Pad

Figure 10. SMD Pad

There are many factors influencing whether the PCB designer uses SMD or NSMD pads. NSMD pads are most commonly used for thermo-mechanical fatigue performance and

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SMD pads are used for improved drop test performance. Fillets are recommended where the trace connects to the Cu pad, especially with NSMD pads.

4.1.3 PCB pad surface finish for FCPBGA

Surface finishes compatible with FCPBGA include organic solderability protectant (OSP), hot air solder leveled (HASL), electroless or electrolytic nickel/gold (NiAu) and immersion silver (Ag). A HASL finish might have an uneven surface. Extra caution is required. The PCB surface finish shelf life should be monitored to ensure that it has not expired. Surfaces should always be free of contaminants before PCB assembly.

4.1.4 PCB routing vias for FCPBGA

For coarser BGA pitches, NXP recommends using thru-hole vias that are offset from the BGA PCB pad and placed interstitially between BGA pads. Preferably, the vias are to be tented with soldermask on both sides of the PCB, with soldermask covering the trace connecting the via and BGA pad. Finer pitches may require the use of via-in-pad structures. The need for via-in-pad structures is generally determined by the PCB design. Via-in- pad designs with fully or partially open vias typically result in voids and inconsistent solder joints after reflow, which can lead to early failures. For via-in-pad structures, NXP recommends using filled vias that can be plated over with copper, so the resulting pad is planar. As with any PCB, the quality and experience of the vendor is very important with via-in-pad designs

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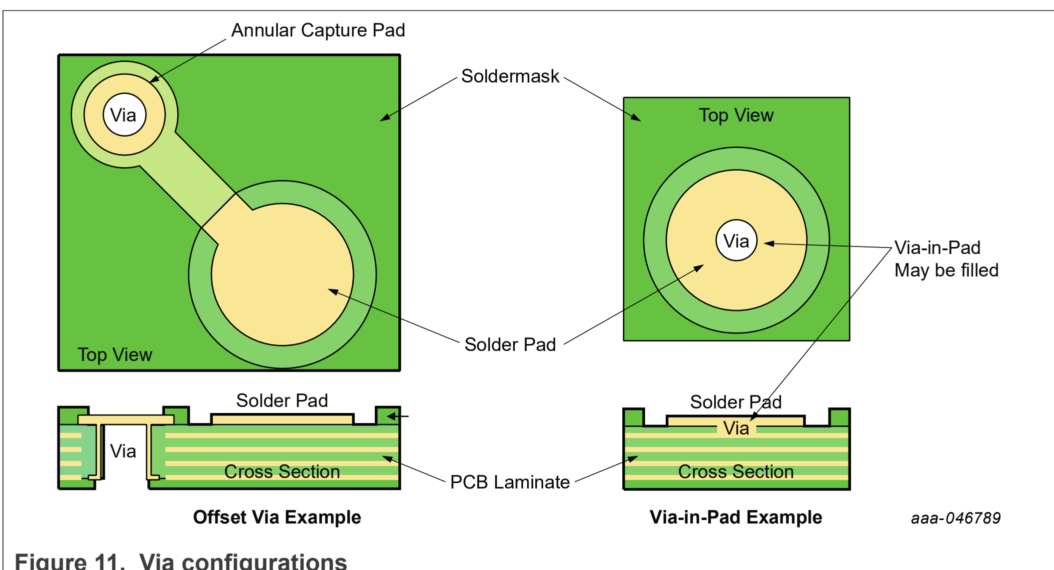

Figure 11. Via configurations

4.1.5 Clearance to vias and adjacent components

Clearance around the component should account for the pick-and-place equipment size, placement accuracy and dimensions of the surrounding components. When underfill is applied, room should be available for dispensing nozzles. Placing a component near features such as PCB mounting holes, connectors or clamps is not recommended. This distance restriction is due to the increased amount of bending stress on the bumps and to avoid hitting those components during product placement for board assembly.

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Placement of components near separation lanes of PCB panels should be avoided to minimize mechanical stress during the panel singulation process.

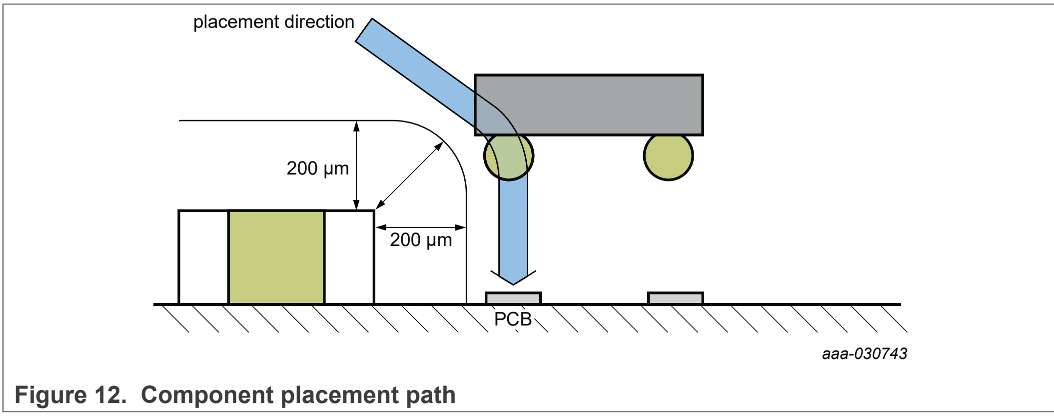

Figure 12. Component placement path

4.2 PCB pad design guidelines and requirements for thin FCCSP packages

For thin FCCSP packages, complete the checklist and then perform a trial assembly run with a minimum of 30 parts to verify good BGA joining yield:

1. Component pick-up and place height adjusted to compensate for the thin package.
2. Check placement force. Excessive placement force may contribute to solder bridging.
3. Board reflow profile verified with temperature sensors located at package top and BGA solder joint. See temperature sensor locations.
4. Component top and BGA solder joint temperatures less than 245 ℃ during reflow. See temperature sensor locations.
5. Non-soldermask defined PC board pad design. See Printed circuit board pad design.
6. Solder stencil aperture diameter matching PC board pad diameter or slightly reduced. See Solder stencil design.
7. Stencil apertures in corner keep-out regions reduced by 10% to 15%. See Solder stencil design.
8. Perform 100 % X-ray and sample cross-section: Check for head-in-pillow (HIP) and bridging solder joints.

4.2.1 Printed circuit board pad design

NXP strongly recommends non-soldermask Defined (NSMD) pads for 100% of the pads on the PC Board. It includes pads formed over ground planes. Thinner packages may have a different characteristic shape at solder reflow temperatures. The corners of thinner packages tend to bend down toward the PC board when the package is above the melting temperature of typical SnAg or SAC solders, as illustrated in Figure 13.

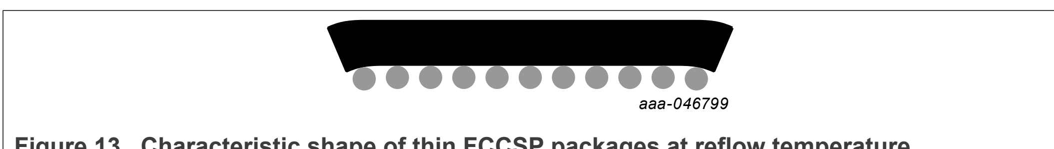

Figure 13. Characteristic shape of thin FCCSP packages at reflow temperature

Soldermask defined (SMD) or a mixture of NSMD and SMD PC board pads are not recommended because the SMD design can cause solder to flow on top of the

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soldermask surrounding the pad, potentially resulting in solder bridging, as illustrated in Figure 14.

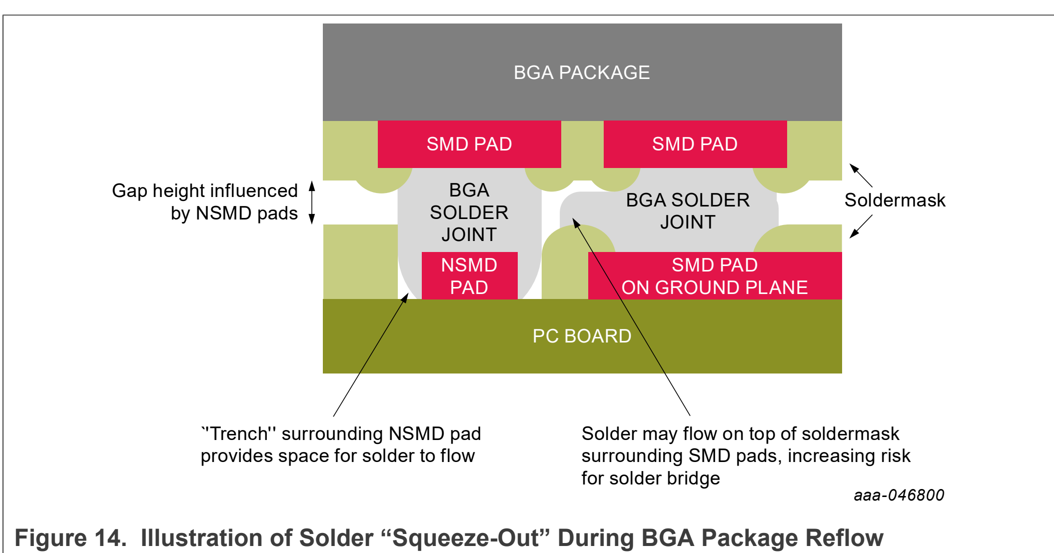

Figure 14. Illustration of Solder “Squeeze-Out” During BGA Package Reflow

Understandably, the preference is often to create an SMD pad over ground planes for electrical and design simplicity motivations. As illustrated above, this may increase the risk of solder bridging. NXP recommends using a ground plane relief design where an opening is created in the plane for placement of an NSMD pad, as shown in Figure 15. The pad is connected to the plane by multiple metal lines. This design maintains the trench around the pad to capture molten solder that may be pushed out during the dynamic package bending during reflow. NXP recommends having the solder resist opening 0.080 mm larger than the NSMD pad diameter.

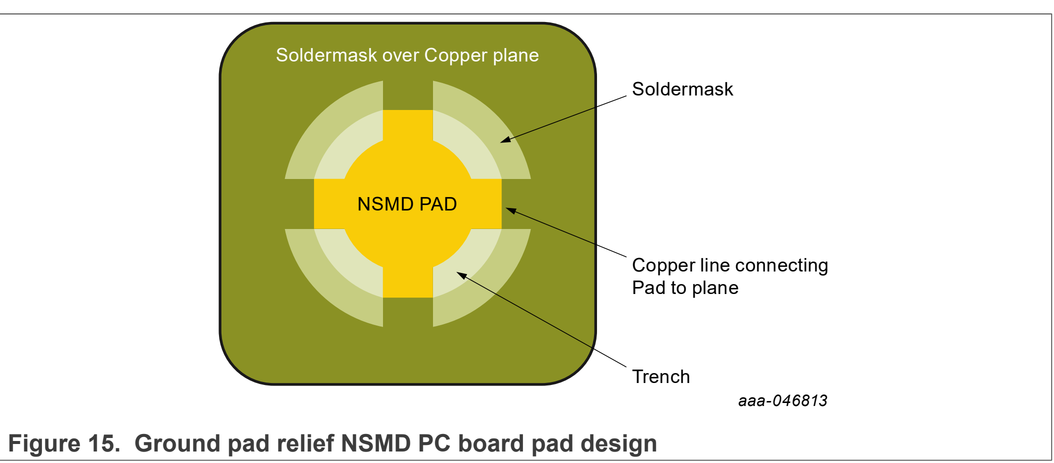

Figure 15. Ground pad relief NSMD PC board pad design

If manufacturing or electrical constraints prohibit the use of NSMD pad design over ground planes, while not recommended, a mixed SMD and NSMD design may be used outside of corner regions which are defined by a 3 × 3 BGA array at each of the four package corners. See Figure 16.

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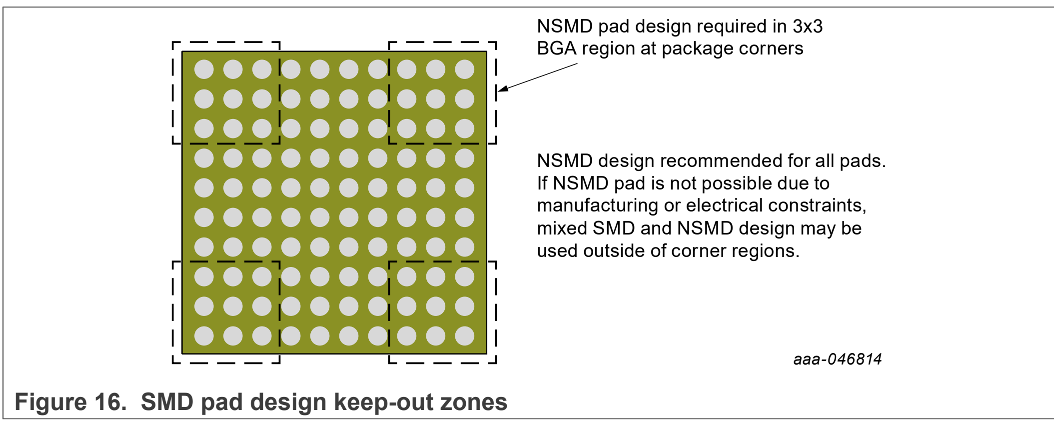

Figure 16. SMD pad design keep-out zones

NXP strongly recommends that design for manufacturability (DFM) checks and electrical simulations are done to realize a design with 100% NSMD pads. If SMD pads are used, it is recommended that the SMD solder resist opening is 0.050mm larger than the NSMD pad diameter used elsewhere.

4.2.2 Solder stencil design

For BGA, the typical stencil aperture diameter should be the same size as the PCB solder pad or solder mask opening for SMD designs. Slight reductions (0.02 - 0.05 mm) of the stencil diameter to the PCB pad diameter may improve gasket between the stencil and PCB. It helps with solder paste release. Thin Flip Chip – Chip Scale Packages (FCCSPs) may bend down toward the PC board at the corners during reflow. To reduce the risk of solder bridging at package corners, a slightly reduced (10 -15 %) stencil aperture at the corner BGA locations may be beneficial.

4.2.3 Reflow profile

The infrared or convection reflow requires a solder joint temperature (SJT) of 235 - 245 °C, not exceeding 245 °C, and should follow the recommendation of the solder paste manufacturer, including the solder alloy being used. NXP recommends that Package Peak Temperature (PPT) should not exceed 245 °C, as higher temperatures may contribute to soldering defects. For details, see General Soldering Temperature Process Guidelines (document AN3300). NXP suggests confirming SJT and PPT by populating a few target PCBs with the new package and verifying that the temperatures meet target specifications.

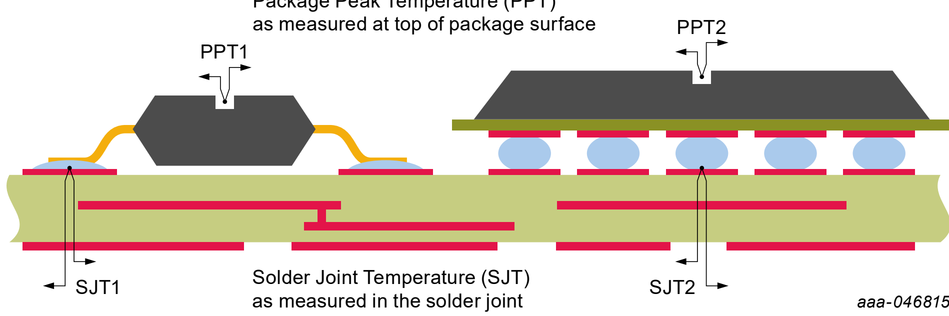

Figure 15. SJT and PPT temperature sensor locations

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5 Board assembly

5.1 Assembly process flow

Figure 17 shows a typical surface mount technology (SMT) process flow.

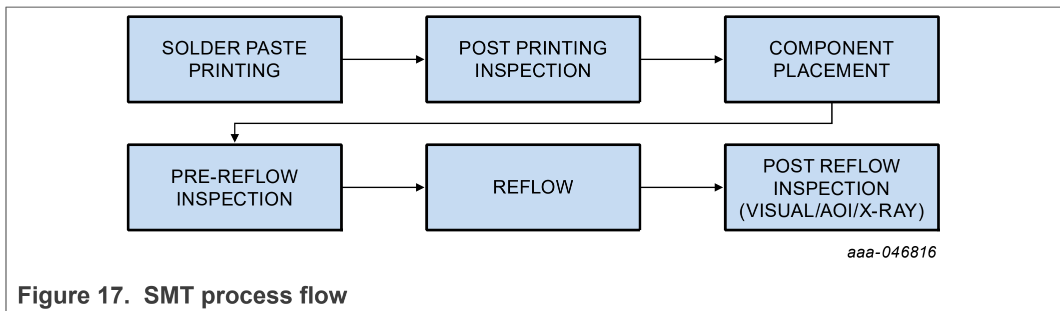

Figure 17. SMT process flow

5.2 Solder stencils

The thickness and apertures of a stencil determine the amount of solder paste deposited on the PCB land. For BGA, the typical stencil aperture diameter should be the same size as the PCB solder pad. Slight reductions (0.02 - 0.05 mm) of the stencil diameter to the PCB pad diameter may improve gasketing between the stencil and the PCB and help with solder paste release. Inspect stencil openings for dimensional accuracy, burrs and other quality issues prior to use. 125 to 150 mm thick stencils have been found to give good results. NXP recommends following IPC-7525 *Stencil Design Guidelines.* When these stencil design requirements conflict with other required surface mount technology (SMT) components in a mixed technology PCB assembly, a step-down stencil process may be utilized in compliance with IPC-7525 [2]design standards.

5.3 Solder paste

Solder paste is a homogenous mixture of fine metal alloy particles, flux, and viscosity modifiers to adjust printing and reflow properties. The main ingredients of solder paste include solder alloy. NXP's preference is to use lead-free solder paste, in line with environmental legislation (RoHS, ELV). A variety of lead-free alloys are available for PCB assembly, with different physical properties and melting temperatures. Typical melting range is between 217 – 220 °C. The peak reflow temperature for these alloys is > 235 °C.

A main component of the paste is the spherical powder made from the solder alloy. The solder pastes are classified by sphere size according to IPC standard J-STD-005 [3]. Smaller spheres allow higher printing resolution and smaller pitches. Solder paste suppliers can recommend a suitable flux for the selected solder paste. For 0.65 mm BGA solder ball pitch and higher, it is recommended to use a paste formulated with type 3 powder. For BGA pitches below 0.65 mm, type 4 powder is recommended. Flux is needed to remove surface oxidation, prevent oxidation during reflow, and improve the wetting of the solder alloy. IPC standard J-STD-004 [4] classifies fluxes into three types:

- Rosin-based flux
- Water-soluble flux
- No-clean flux

Rosin based and water-soluble fluxes require cleaning of the PCB after the reflow process. Standard rosin chemistries are normally cleaned with solvents, semi-aqueous

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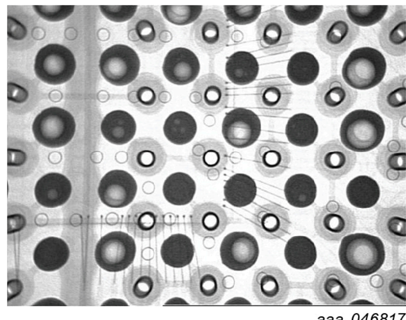
solutions or aqueous/saponifier solutions, while the water-soluble chemistries are cleaned with pure water.

In general, NXP recommends using a no-clean solder paste, as it does not require cleaning.

5.4 Flip Chip BGA solder joint voids

BGA solder joint voids, commonly known as “Macro” or “Process” voids, are the result of solder paste flux volatiles trapped during the solidification of the molten solder during the PCB reflow assembly process. PCB assembly process parameters, as well as the type of solder paste used, can have a significant impact on the quantity and size of the voids. Water washable solder paste typically produces larger voids than rosin-based paste. IPC-610 calls out a void criterion of a maximum of 25% of the joint area.



aaa-046817

Figure 18. X-ray showing voids in BGA solder joints

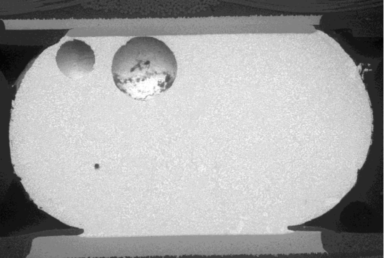


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Figure 19. Cross-section of BGA solder joint showing macro voids

5.5 FCPBGA placement

NXP recommends an automated fine-pitch pick-and-place tool with an optical recognition system for precisely placing FCPBGAs on a PCB. Local fiducial markers are required on the board to support the vision systems.

Flip Chip BGAs have excellent self-centering properties which are attributed to surface tension between the applied solder on the PCB solder pad and the FCPBGA solder sphere. Surface tension during solder reflow will center the BGA spheres to the PCB pads. The solder spheres of the FCPBGA should be pushed into the printed solder paste until they are contacting the PCB solder pad, to reduce the risk of head in pillow (HIP) open solder joints.

5.6 Flip Chip package placement – bare die packages

Lidless and non-overmolded Flip Chip packages feature an exposed backside, or top surface, of the semiconductor chip, which is often the surface that the designer uses for vacuum-picking and placing the component onto the printed circuit board. To prevent chipping or fracturing the exposed silicon die backside and edges, exercise caution when handling and placing lidless packages. Do not use a metal pickup tip, as this may damage the exposed die.

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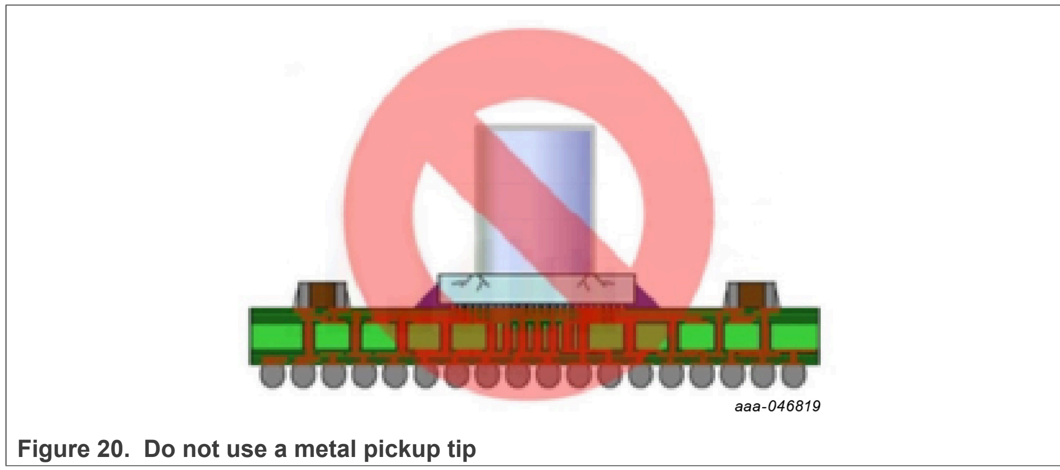

Figure 20. Do not use a metal pickup tip

When picking and placing exposed silicon devices, use a compliant-tip nozzle with a rubber tip and a closed loop head to control force, as shown in Figure 21.

Use only a vacuum pencil with a compliant tip material whenever manual handling is required. Do not handle parts using tweezers.

Note: *Consult your pick-and-place equipment provider for pick-up tip size and material recommendations.*

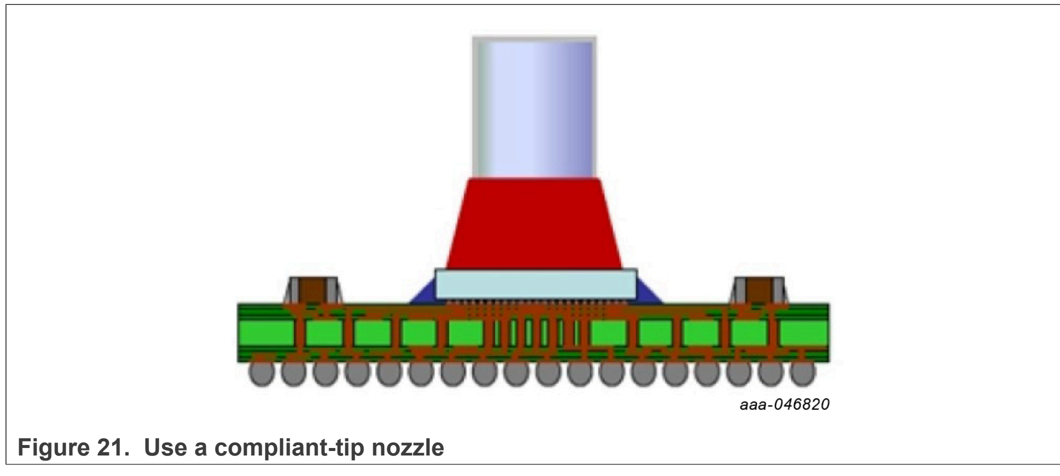

Figure 21. Use a compliant-tip nozzle

When the lidless or non-overmolded Flip Chip component is the tallest component on the printed circuit board, the risk of impact is high. After soldering the package to the printed circuit board, be sure subsequent tooling and handling is designed such that the exposed die is not impacted.

5.7 Flip Chip PBGA reflow soldering guidelines

See AN3300 “General Soldering Temperature Process Guidelines, Solder Joint and Package Temperature for Pb-free BGA in SnPb and Pb-free Solders in IR or Convection Reflow Ovens” for guidelines for reflow soldering of Flip Chip BGA Packages. While profiling, the temperature of the package top surface shall be monitored, to validate that the peak package body temperature (TP) does not exceed the MSL classification of individual devices. See IPC/ JEDEC J-STD020[5].

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5.8 Post reflow washing

Post-reflow washing with water or solvents is typically discouraged, as moisture or chemicals could corrode or attack package materials. If a water or solvent wash process is used, care must be taken to completely dry the water from the PCB and components following the wash process. The component should be cooler than the wash fluid when entering the wash process. This is especially true with the full lid FCPBGA configuration. This configuration typically features venting that allows pressure equalization between the inside and outside surfaces of the lid. During the water or solvent wash process, moisture or chemicals may seep under the lid through the vents. To remove this moisture, NXP strongly recommends a post-wash bake.

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6 Repair and rework procedure

The entire board to be reworked should be baked for at least 12 hours at 125 °C, or at the highest temperature the assembly can withstand, to remove moisture which can result in Flip Chip package delamination. BGA spheres completely melt and will solder without additional solder if flux only is applied. Solder paste is not required for FCPBGA replacement. If solder is completely removed from the PC board, solder paste may need to be re-applied.

The same careful temperature profiling procedures used during the original reflow process should be used for rework.

- Preheat the entire board in an offline bake oven to minimize “oil canning” type PCB warpage under the BGA package. Preheat SnPb soldered boards to a minimum of 125 ºC and Pb-free boards to a minimum of 150 ºC.
- After desoldering the package, remove residual solder from the PCB solder pads while the PCB is still hot using solder wick and a soldering iron.
- Apply a small volume of no clean flux to the cleaned PCB solder pads.
- Place the new BGA using a microscope or rework station that incorporates a vision system capable of viewing the BGA spheres as well as the PCB solder pads.
- NXP does not recommend using re-balled BGAs on products due to long-term solder joint reliability concerns.

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7 Board level reliability

Board level reliability (BLR) testing is performed to determine a measure of board-level reliability when exposed to thermal cycling. There are several different names for BLR, including:

- Second-level reliability (2nd-level reliability)
- Solder joint reliability (SJR)
- Temperature cycling on board (TCoB)

BLR testing is performed by NXP on packages using a daisy chain ball grid array configuration. BLR temperature cycling conditions may vary widely, depending on the application and specific user. NXP recommends that users run this test using production surface-mount process and board design to develop application specific information. Typically, board level temperature cycling tests are performed according to JEDEC condition G (–40 °C to 125 °C) and IPC-9701[6].

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8 FCPBGA thermal solution considerations

With a properly designed heat-sink and thermal interface material (TIM) system, Flip Chip Ball Grid Array components can achieve very good thermal resistance values.

Table 3 and Table 4 show relative thermal performance for thermal solutions for both lidded and lidless 780 I/O 23x23mm FCPBGA packages.

Note: *These simulations assume a standard JEDEC open-flow environment. This may not always be practical, or even possible, in a high-volume manufacturing environment or end application.*

Table 3. Use case thermal characteristics for lidless 780 FCPBGA 23x23 mm die

Rating	Board	Symbol	Value	Units	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\Theta JA}$	28	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	19	°C/W	1, 2
Junction to ambient (@200ft/min)	Single-layer board (1s)	$R_{\Theta JMA}$	22	°C/W	1, 2
Junction to ambient (@200ft/min)	Four-layer board (2s2p)	$R_{\Theta JMA}$	15	°C/W	1, 2
Junction to case (top)	-	$R_{\Theta JCtop}$	<0.1	°C/W	3

Notes:

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3[7] and JESD51-6[8]. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8[9]. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883[10] Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Junction-to-lid-top thermal resistance determined using the MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.

Table 4. Use case thermal characteristics for full-lidded 780 FCPBGA 23x23 mm die

Rating	Board	Symbol	Value	Units	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\Theta JA}$	22	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	14	°C/W	1, 2
Junction to ambient (@200ft/min)	Single-layer board (1s)	$R_{\Theta JMA}$	15	°C/W	1, 2
Junction to ambient (@200ft/min)	Four-layer board (2s2p)	$R_{\Theta JMA}$	10	°C/W	1, 2
Junction to case (top)	-	$R_{\Theta JCtop}$	0.8		3

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Table 4. Use case thermal characteristics for full-lidded 780 FCPBGA 23x23 mm die*...continued*

Rating	Board	Symbol	Value	Units	Notes
Junction to lid (top)	-	-	0.35	°C/W	4

Notes:

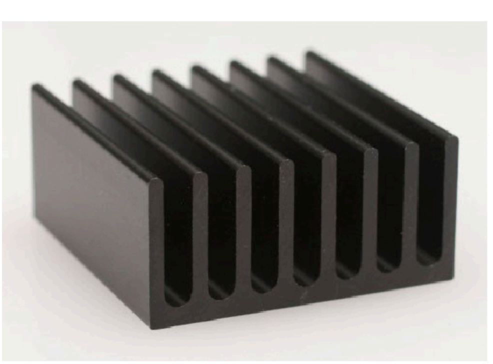
1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Junction-to-lid-top thermal resistance determined using the MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.

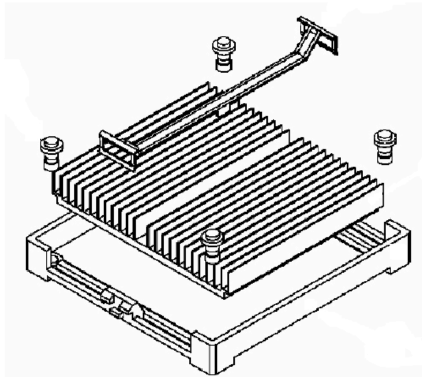
8.1 Heat sink attachment

The maximum allowable junction temperature for each product can be typically found in the hardware specification. Depending on the application and the NXP product involved, most Flip Chip PBGA applications may require a heat sink. The heat sink is selected by the customer.

NXP recommends that heat sinks be attached to the Printed Circuit Board (PCB). Clipping or attaching to the Package substrate can result in solder ball failure. A backing plate may be necessary to prevent board warpage. Ensure that the tooling and fixtures do not bend or flex the printed circuit board, and that the soldered flip-chip component, which is made from a stiff material, does not crack.

The maximum allowable heat sink attachment force is a function of the BGA solderable pad area. A general rule of thumb is a maximum of 59 gm-f per square mm of solderable pad area. If higher heat sink forces are required, please contact NXP Field Applications.





8.2 Choosing a thermal interface material

Consider the thermal interface material (TIM) options early in your design, as this choice depends on cost targets, package application, manufacturing dynamics, and the performance requirements of the thermal solution. By selecting the appropriate TIM, you

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can help reduce the size of the heat sinks and the need for larger cooling fans. In the long-term, the appropriate TIM can mitigate the potential cost of changing heat sinks or redesigning a chassis.

Because lidless flip-chip packages have a small surface area compared with that of lidded or molded packages, the combination of an adhesive TIM and heat sink is not recommended. NXP recommends the following TIMs for lidless packages:

- Phase change TIM (PCTIM)
- Cross-linked thermal gels
- Thermal pads and tapes
- Thermal grease

High-performance TIMs, like greases, compounds and gels, are expensive and may be more difficult to handle during installation. Thermal pads and tape offer an easier heat-sink attachment process, but with reduced performance. Phase-change TIMs provide a compromise solution, which offers ease-of-assembly with good performance.

This table provides advantages and disadvantages of the TIM types recommended for lidless packages.

Note: *Heat sinks can be ordered with phase-change TIMs pre-applied from the supplier.*

Table 5. Recommended TIMs for lidless packages

TIM	Description	Description	Disadvantages
Phase-change material	Remains solid at room temperature, and melts at elevated temperatures close to the package operating temperature. The material is in a liquid phase at die-operating conditions.	In its molten phase, where the material is in a viscous state, the material conforms to and wets both the heat sink and die surfaces better than any solid material. This results in a material with low thermal impedance as the thermal contact resistance is significantly reduced.	Requires about 20-40 psi of pressure to achieve the recommended TIM bond-line thickness. The heat sink must have adequate loading pressure on the die.
Cross-linked thermal gels	Dispensable materials that cure into a soft compound over time.	Being viscous in pre-cure form, it has the ability to fill into gaps and voids before curing. This enables a low inter-facial thermal resistance.	Material must be dispensed on to the die surface. Requires an automated process to ensure consistent dispensation.
Thermal pads and tapes	Prefabricated thermal interface materials which are supplied at a specified thickness (~0.25-1 mm).	• Most have a core material or wire mesh to retain the structural integrity of the material. • Pre-cut to size (~20% larger than the die size). • Most are tacky on one side for self-adhesion to the heat-sink surface.	Thermal performance is relatively poor compared to the cross-linked thermal gels and phase-change material options.
Thermal grease	Typically, silicone oils embedded with thermally conductive filler particles	• Highly conductive • Low thermal resistance • Flows and conforms to surfaces • May be applied with a thin bond-line thickness	Greases can pump-out and dry out over extended periods of operation. Careful application is required to maintain consistent bond-line thickness.

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8.3 Attaching the heat sink to a lidless package

The selection and attachment of a heat sink is as important as the selection of the TIM material. Typically, the device data sheet provides the maximum allowable junction temperature for the device. Depending on the application and the NXP device involved, most applications require a heat sink, which is selected by the customer.

For lidless configurations, use a heat sink anchored to the PCB for robust mechanical integrity. The heat sink can be anchored using a clip, spring loaded screws, or push pins. To prevent board warpage, a backing plate may be necessary on the side of the printed circuit board opposite the Flip-Chip device.

Aligning the heat sink and package

To avoid die damage or TIM damage during heat sink assembly to package, ensure that the heat sink base remains parallel to the package, and that a uniform layer of thermal interface material is present between the heat sink and the exposed die. The heat sink must not directly contact the exposed die surface.

Note: *Non-parallel alignment of heat sink and die may damage the die.*

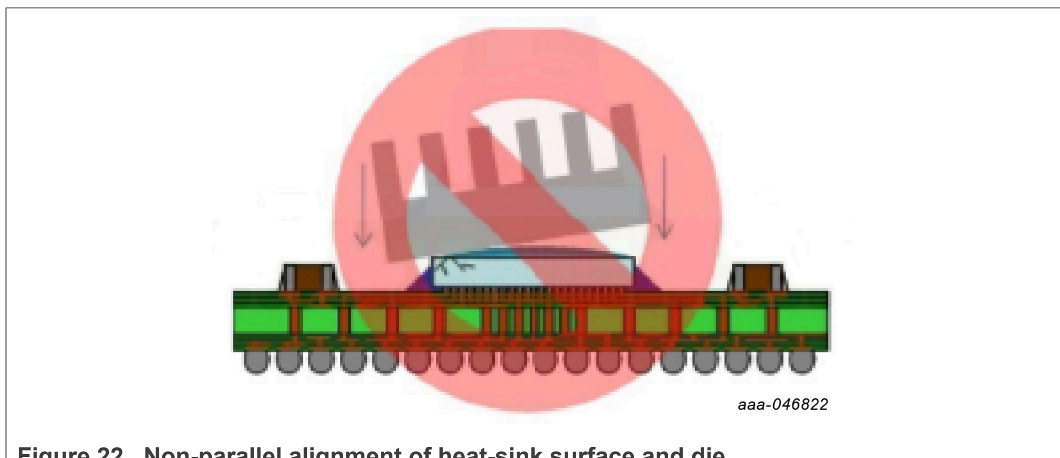

Figure 22. Non-parallel alignment of heat-sink surface and die

Use alignment foam or bumpers around the heat sink periphery to ensure that the base of the heat sink is parallel to the die surface prior to clamping. Apply even pressure on the clip anchor or pushpins located on the opposite sides of the heat sink. Uneven pressure may cause the heat sink to tilt, resulting in an uneven TIM bond-line thickness.

Important

Thermal Interface Material is not a glue. Do not rely on it for adhesion. Ensure that the heat sink is parallel to the backside surface of the die, as shown in Figure 23.

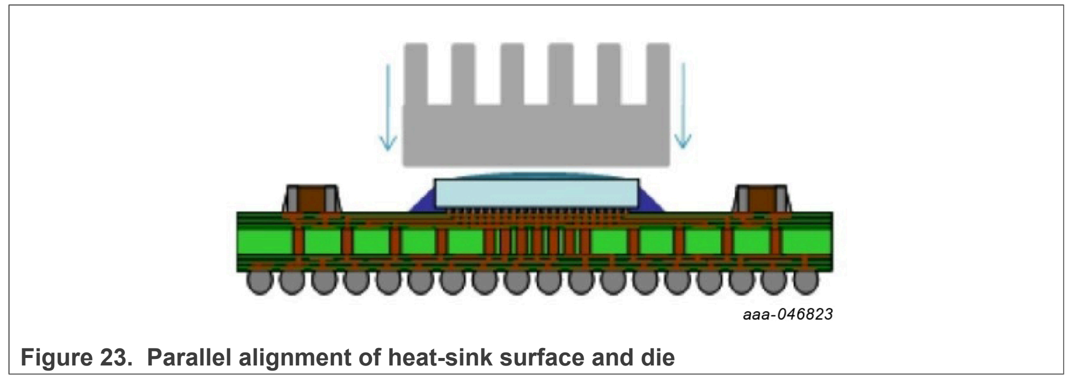

Figure 23. Parallel alignment of heat-sink surface and die

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8.4 Removing or reworking the heat sink attachment

Before you remove a heat sink, ensure your work area is free of materials that may cause damage, and that the backside surface of the die is clean.

To remove a heat sink, follow these steps:

1. Remove the heat sink by completing the attachment process in reverse order.
2. After removing the clip or anchoring screws, squirt or spray solvent, or other material recommend by the TIM supplier (for example, isopropyl alcohol (IPA)), at the die to heat-sink base interface to soften the TIM material.
3. Slide a dental floss under the heat sink and use a sawing motion to cut the TIM.
4. Use a lint-free cloth, and the same dental floss material mentioned previously, to clean the remnants of the TIM from the die surface.
5. Before mounting the new heat sink, inspect the die backside surface to ensure that there is no residual TIM or die scratching, chipping, or cracking present.

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9 Downloading package information from NXP website

9.1 Performing a product search on NXP website

At www.nxp.com NXP offers packaging, environmental, and compliance information in the parametric tables and in the device information details. Enter the part number in the search box and review the package information details for the specific part.

9.2 Moisture sensitivity level

The Moisture Sensitivity Level (MSL) indicates the component floor life, storage conditions, and handling precautions after the original container has been opened. The permissible time (from opening the moisture barrier bag until the final soldering process) that a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity.

In many cases, moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process. The expansion of trapped moisture can result in interfacial separation7 of the mold compound from the die or substrate, wire bond damage, die damage, and internal cracks. In the most severe cases, the component can bulge and pop, known as the "popcorn" effect.

It is necessary to seal dry moisture-sensitive components in a moisture barrier antistatic bag with a desiccant and a moisture indicator card. Vacuum seal the bag according to IPC/JEDEC J-STD-033[12] and only remove immediately prior to assembly to the PCB.

Table 6 presents the MSL definitions per IPC/JEDEC J-STD-20. Refer to the “Moisture Sensitivity Caution Label” on the packing material, which contains information about the moisture sensitivity level of NXP products. Components must be mounted and reflowed within the allowable time period (floor life out of the bag). The maximum reflow temperature shall not be exceeded during board assembly at the customer’s facility.

If moisture-sensitive components have been exposed to ambient air for longer than the specified time according to their MSL rating, or the humidity indicator card (HIC) indicates too much moisture after opening a moisture-barrier bag (MBB), baking the components is required prior to the assembly process. To determine allowable maximum temperature, refer to imprints/labels on the respective packing.

The higher the MSL value, more attention is required to store the components. NXP packages use JEDEC standard IPC/JEDEC J-STD-020 for classification of its package.

Table 6. MSL descriptions

Level Rating	Floor Life	
	Time	Conditions
1	Unlimited	30 °C / 85% RH
2	1 Year	30 °C / 60% RH
2a	4 Weeks	30 °C / 60% RH
3	168 Hours	30 °C / 60% RH
4	72 Hours	30 °C / 60% RH
5	48 Hours	30 °C / 60% RH
5a	24 Hours	30 °C / 60% RH

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Table 6. MSL descriptions...*continued*

Level Rating	Floor Life	
	Time	Conditions
6	Time on Label (TOL)	30 °C / 60% RH

9.3 Retrieving package outline drawing, MCD and MSL rating

The complete case outline drawing and the Material Composition Declaration Sheet (MCDS), following the IPC-1752-A[11] reporting format, can be downloaded as a PDF file. Information on product-specific moisture sensitivity level (MSL) is also available in the part details.

- Click on the "Package/Quality" tab to view environmental and quality information.
- Click on the "Material Declaration" link to go to the "Chemical Content" site. Material information is displayed. The MCD sheet can be downloaded in .xlsx, XML and PDF formats.
- Click the "Package" link to go to the "Package Overview" site. Package information is displayed. A PDF file with the package outline drawing can be downloaded.

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10 Package handling

10.1 Handling ESD devices

Semiconductor Integrated Circuits (ICs) and components are Electrostatic Discharge Sensitive devices (ESDS). Proper precautions are required for handling and processing them. Electrostatic Discharge (ESD) is one of the significant factors leading to damage and failure of semiconductor ICs, and components. Comprehensive ESD controls to protect ESDS during handling and processing should be considered.

The following industry standards describe detailed requirements for proper ESD controls. NXP recommends users meet the standards before handling and processing ESDS. Detailed ESD specifications of devices are available in each device data sheet.

JESD615-B[13] – Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

IEC-101/61340-5[14]– Specification for the Protection of Electronic Devices from Electrostatic Phenomena.

10.2 Handling moisture-sensitive SMD devices

Flip Chip PBGA devices are moisture/reflow sensitive surface mount devices (SMD) and proper precautions are required for handling, packing, shipping, and use. Moisture from atmospheric humidity enters permeable packaging materials by diffusion. Assembly processes used to solder SMD packages to PCBs expose the entire package body to temperatures higher than 200 °C. As noted in Section 9.2 "Moisture sensitivity level", during solder reflow, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the package. Cracking and/or delamination can lead to failure and reliability concern. Proper handling of SMDs should be considered.

Dried moisture-sensitive SMDs are placed in trays or tape-and-reels, and dry-packed for proper transportation and storage. SMDs are sealed with desiccant material and a humidity indicator card (HIC) inside a Moisture-Barrier Bag (MBB). The shelf life of dry-packed SMDs is 12 months from the dry pack seal date when stored in ≤ 40 °C / 90% RH environment.

Proper use and storage of moisture-sensitive SMDs is required after the MBB is opened. Improper use and storage increase various quality and reliability risks. SMDs subjected to reflow solder or other high temperature processes must be mounted within the period of floor environment specified by MSL or stored per J-STD-033D standard.

The baking of SMDs is required before mounting if any of the following conditions is experienced:

- SMDs exposed to a specified floor environment greater than specified period
- Humidity Indicator Card (HIC) reading > 10 % for level 2a – 5a or > 60 % for level 2 devices when read at 23 °C ± –5 °C environment.
- SMDs not stored according to J-STD-033D standard
- The baking procedure, and more detailed requirements and procedures of handling moisture-sensitive SMDs can be found in the following industry standard: J-STD-033D – Handling, Packing, Shipping, and Use of Moisture/Reflow Sensitive Surface Mount Devices

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10.3 Packing of devices

Flip Chip BGA devices are contained in tray or tape-and-reel configuration. The trays and tape-and-reels are dry-packed for transportation and storage. Packing media is designed to protect devices from electrical, mechanical, and chemical damage as well as moisture absorption. However, proper handling and storage of dry packs are recommended. Improper handling and storage (dropping dry packs, storage exceeding 40 °C / 90 % RH environment, excessive stacking of dry packs, etc.) increase various quality and reliability risks.

Tray

- NXP complies with standard JEDEC tray design configuration, see Figure 24.
- Pin 1 of the devices is oriented with lead 1 toward the chamfered corner of the tray.
- Trays are designed to be baked for moisture sensitive SMDs, but the temperature rating of tray should NOT be exceeded when devices are baked. The temperature rating can be found at the tray end-tab. Recommended baking temperature of trays is 125 °C.
- Trays are typically banded together with 5+1 (five fully loaded trays and one cover tray) stacking and dry-packed in a moisture barrier bag. Partial stacking (1+1, 2+1,etc.) is also available depending on individual requirements.

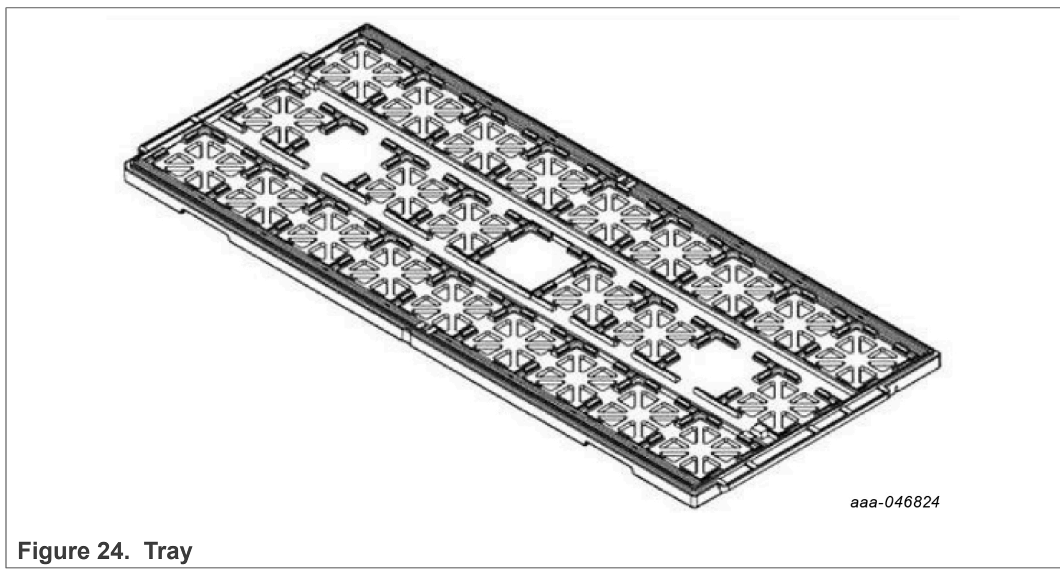

Figure 24. Tray

Tape and reel

- NXP complies with EIA-481-E[15]for carrier tape and reel configuration, see Figure 25 and Figure 26.
- NXP complies with pin 1 orientation of devices with EIA-481-E.
- Tape-and-reels are NOT designed to be baked at high temperature.
- Each tape-and-reel is typically dry-packed in a moisture barrier bag

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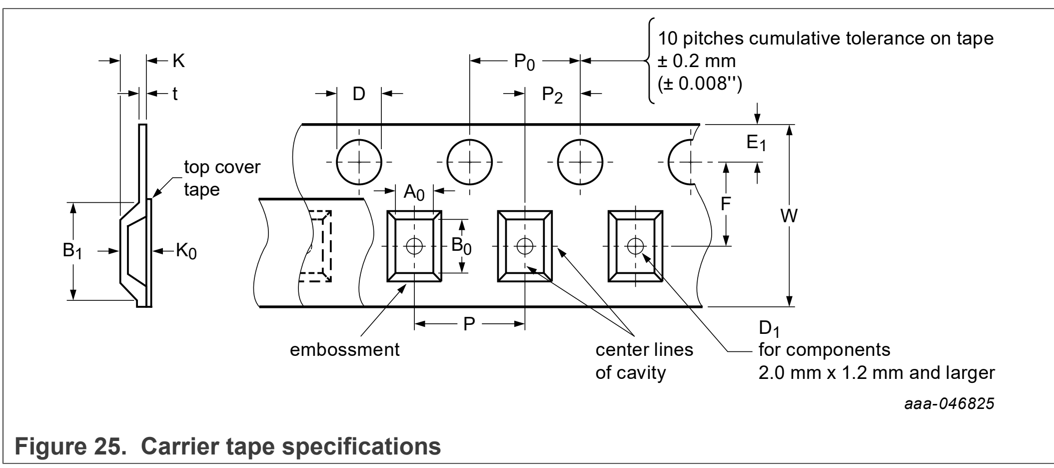

Figure 25. Carrier tape specifications

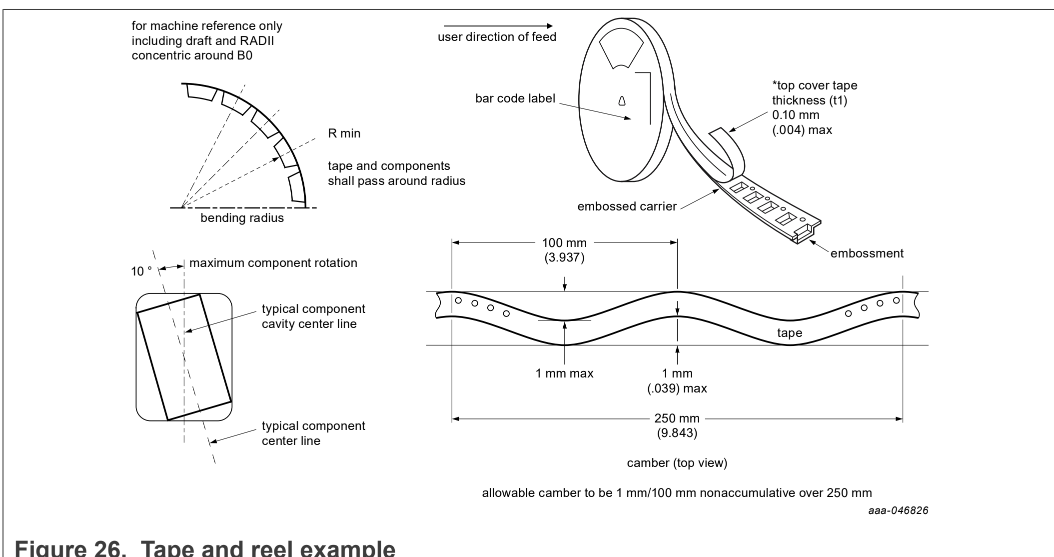

Figure 26. Tape and reel example

Dry packing

- Trays and tape-and-reels loaded with devices are sealed in a moisture barrier bag, labeled, and packed in dedicated boxes with dunnage for the final shipment.
- Each dry pack bag contains a desiccant pouch and a humidity indicator card (HIC).
  - NXP encourages the recycling and reuse of materials whenever possible.
- NXP does not use packing media items processed with or containing Class 1 ozone depleting substances.
- Whenever possible, NXP designs its packing configurations to optimize volumetric efficiency and package density to minimize the amount of packing material entering the industrial waste stream.
- NXP complies with the following environmental standards conformance guidelines/ directives:
  - ISPM 15[16], *Guidelines for Regulating Wood Packaging Material in International Trade*
  - EPCD 94/62/EC[17], *European Parliament and Council Directive 94/62/EC of 20 December 1994 on packaging and packaging waste*

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12 Abbreviations

Table 7.

Acronyms	Description
AEC	Automotive Electronics Council
BLR	board level reliability
BU	build-up (refers to package substate structure)
C	core (refers to package substate structure)
DFM	design for manufacturability
ESD	electrostatic discharge
ESDS	dlectrostatic discharge sensitive devices
FCCSP	Flip Chip chip-scale package
FCPBGA	Flip Chip plastic ball grid array
HASL	hot air solder leveled
HDI	high density interconnect
HIP	head in pillow
HIC	humidity indicator card
IPA	isopropyl alcohol
MBB	moisture-barrier bag
MSL	moisture sensitivity sevel
NiAu	nickel (Ni) gold (Au)
NSMD	non-soldermask defined
PCB	printed circuit board
PC	printed circuit
PCTIM	phase change TIM
PPT	package peak temperature
SAC	tin (Sn) silver (Ag) copper (Cu) solder
SJR	solder joint reliability
SJT	solder joint temperature
SMD	soldermask defined
SMT	surface mount technology
SnAg	tin (Sn) silver (Ag) solder
OSP	organic solderability protectant
TCoB	temperature cycle on board
TIM	thermal interface material

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Date of release: 1 September 2022
Document identifier: AN13536