AN13803

How to Migrate LPC84x to LPC86x

Rev. 0 — 22 May 2023 Application note

Document Information

Information	Content
Keywords	LPC86x, LPC84x, AN13803
Abstract	This application note lists the significant differences between the LPC84x and LPC86x families and the general considerations for migrating from LPC84x to LPC86x

1 Introduction

This application note lists the significant differences between the LPC84x and LPC86x families and the general considerations for migrating from LPC84x to LPC86x. This document focuses mainly on the LPC845 and LPC865 devices and their features. Based on the LPC84x motor control support, personal computer accessories and applications, the LPC86x enhances its performance and features.

The LPC84x series has eight parts, see Table 1.

Table 1. LPC84x series

Type number	Frequency(MHz)	Flash/kB	SRAM/ kB	USART	I2C	I3C	SPI	DAC	Capacitive touch	GPIO	Package
LPC845M301JBD64	30	64	16	5	4	-	2	2	yes	54	LQFP64
LPC845M301JBD48	30	64	16	5	4	-	2	2	yes	42	LQFP48
LPC845M301JHI48	30	64	16	5	4	-	2	2	yes	42	HVQFN48
LPC845M301JHI33	30	64	16	5	4	-	2	1	yes	29	HVQFN33
LPC844M201JBD64	30	64	8	2	2	-	2	-	-	54	LQFP64
LPC844M201JBD48	30	64	8	2	2	-	2	-	-	42	LQFP48
LPC844M201JHI48	30	64	8	2	2	-	2	-	-	42	HVQFN48
LPC844M201JHI33	30	64	8	2	2	-	2	-	-	29	HVQFN33

And, the LPC86x series currently has only three parts, see Table 2.

Table 2. LPC86x series

Type number	Frequency(MHz)	Flash/kB	SRAM/ kB	USART	I2C	I3C	SPI	DAC	Capacitive touch	GPIO	Package
LPC865M201JBD64	60	64	8	3	1	1	2	-	-	54	LQFP64
LPC865M201JHI48	60	64	8	3	1	1	2	-	-	42	HVQFN48
LPC865M201JHI33	60	64	8	3	1	1	2	-	-	29	HVQFN33

For LPC84x and LPC86x system block diagram, see Figure 1.

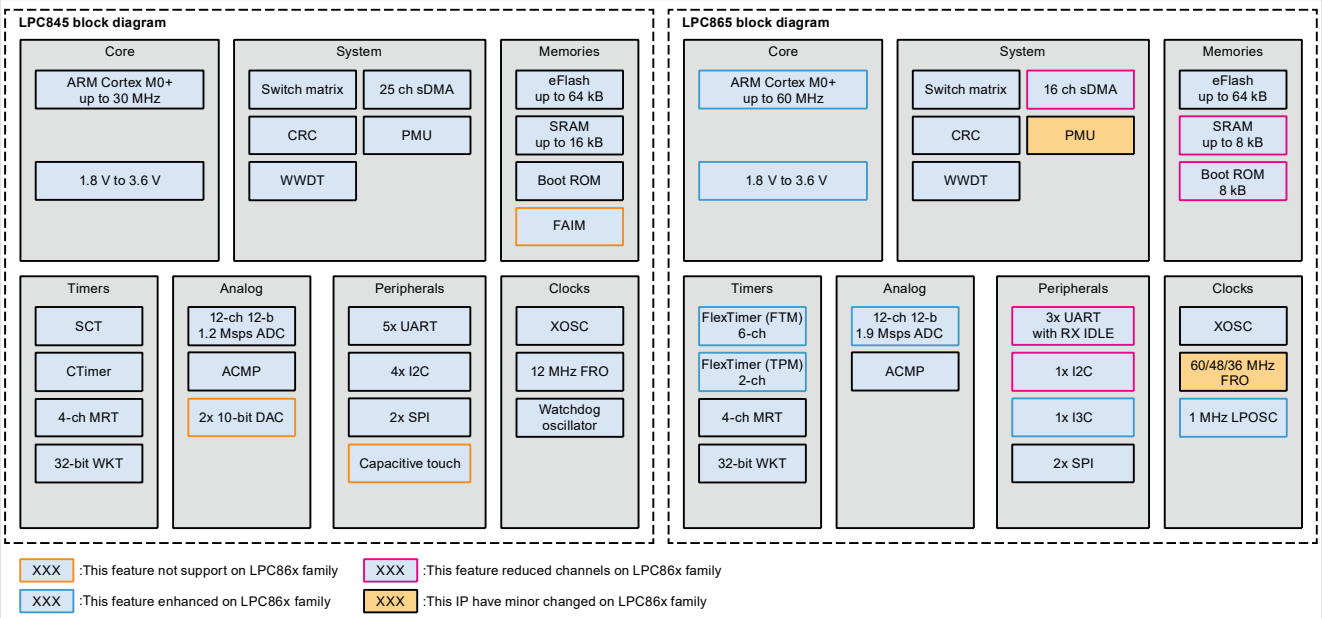

Figure 1. LPC84x and LPC86x system block diagram

2 Acronyms and abbreviations

Table 3 defines the acronyms and abbreviations used in this document.

Table 3. Acronyms and abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
ACMP	Analog Comparator
CLKGEN	Clock Generator
CRP	Code Read Protection
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
FAIM	Fast Initialization Memory
FRO	Free Running Oscillator
FTM	Timer - FlexTimer
GPIO	General-Purpose Input/Output
ISP	In-System Programming
IOCON	Input/Output configuration
LPOSC	Low-Power Oscillator
MTB	Micro Trace Buffer
MRT	Multi-Rate Timer
PIO	Programmable Input/Output
PMU	Power Management Unit

Table 3. Acronyms and abbreviations...*continued*

Acronym	Description
ROM	Read-Only Memory
SCT	Semi-Conductor Tracker
SCRP	Strength Code Read Protection
SRAM	Static Random-Access Memory
UART	Universal Asynchronous Receiver/Transmitter
ULPOSC	Ultra Low-Power Oscillator
USART	Universal Synchronous and Asynchronous Receiver/Transmitter
WWDT	Windowed Watchdog Timer
WKT	Wake-up Timer

3 High-level change summary

Keeping the LPC845 as a reference, Table 4 shows the high-level changes and the features for all LPC86x family.

Table 4 includes a difference column to indicate the level of changes. This "**Difference**" column is classified as the following:

- High: Completely new peripheral / IP block. Might require a significant change in software.
- Mid: Major changes to an existing IP, impacting software changes.
- Low: Minor changes to the new IP, minor or no software changes required.

Table 4. LPC845 and LPC865 family level comparison

Items	System resource		LPC845	Difference	LPC865	Description
Core	Core type		Arm Cortex-M0+	NA	Arm Cortex-M0+	-
	Core max Frequency		30 MHz	Low	60 MHz	-
Memory	Flash	Size	64 kB	NA	64 kB	-
		Cache	-	Low	32 bytes	-
		Buffer	-	Low	Add flash line buffer	-
	SRAM		16 kB	Low	8 kB	-
	MTB		8 kB (shared with SRAM)	High	-	LPC86x do not supports MTB
	Boot ROM		16 kB	High	8 kB	LPC86x support only UART ISP
	FAIM		256-bit	High	-	LPC86x do not supports FAIM
DMA	sDMA		25ch / 13trigger	Low	16 ch / 13 trigger	-
Clock	external crystal(XOSC)		1 MHz to 25 MHz	NA	1 MHz to 25 MHz	-
	FRO		YES (default 24 MHz)	Mid	YES(default 48 MHz)	-
	Watchdog OSC		YES	High	-	LPC86x can use LPOSC instead of Watchdog OSC
	1 MHz LPOSC		-	High	YES	-
	External clock input		Up to 25 MHz	NA	Up to 25 MHz	-
Analog	ADC		1.2 Msps / 12 bit	Mid	1.9 Msps / 12bit	ADC channel 0 can link to internal PMU

Table 4. LPC845 and LPC865 family level comparison*...continued*

Items	System resource	LPC845	Difference	LPC865	Description
	DAC	2x10 bit	High	-	-
	ACMP (comparator)	5x inputs	NA	5x inputs	-
Timers	SCT	1x32 bit(or 2x16 bit)	High	-	LPC86x can use FTM0 to do part of SCT feature, use FTM1 to do part of CTimer
	CTimer	1x32 bit	High	-	
	FlexTimer	-	High	FTM0 6-ch FTM1 4-ch	
	MRT	4x	NA	4x	-
	Wake-up Timer (WKT)	YES	NA	YES	-
	WWDT	YES	NA	YES	-
Peripheral	UASRT	5	Low	3	LPC86x USART enhanced with received idle interrupt
	SPI	2	NA	2	-
	I2C	2	NA	1	-
	I3C	-	High	YES	New feature on LPC865, I3C 1.1
	Capacitive touch	YES	High	-	-
System Feature	Switch-Matrix	YES	High	YES	-
	System default clock	12 MHz	Mid	24 MHz	-
	Code protection	CRP	Mid	SCRP	LPC86x enhanced this feature
	GPIO reset status	With internal pull-up except I2C pins	High	Tri-status	Important to hardware design
Package	LQFP64	YES	NA	YES	Pin2Pin
	LQFP48	YES	-	-	-
	HVQFN48	YES	NA	YES	Pin2Pin
	HVQFN32	YES	NA	YES	Pin2Pin

In summary:

- Enhances MCU core running frequency up to 60 MHz
- ADC channel 0 can link to internal PMU 0.9 V source
- Flash support 32 Byte cache interface
- Flash support line buffer
- Reduced system SRAM from 16 kB to 8 kB
- Reduced ROM size from 16 kB to 8 kB (LPC86x ROM only support UART ISP)
- Replace 30/24 MHz FRO with new 60/48/36 MHz version
- Replace watchdog oscillator with 1 MHz LPOSC from LPC80x series
- Keep 3x USART (removed 2x from LPC84x)
- Enhanced USART with received idle interrupt
- Keep 1x I2C (removed 3x from LPC84x)
- Replace SCT timer with 6-ch FlexTimer (FTM0)
- Replace CTimer32 with 4-ch FlexTimer (FTM1)
- Add AIPS_Lite bridge for FlexTimers
- Change GPIO reset state to tri-state
- Add I3C (version 1.1)
- Add a Low-power operating mode

- Reduced DMA channels
- Removed FAIM memory
- Removed DAC
- Removed Capacitive touch
- Redesign AHB matrix, Switch-Matrix, IOCON, Syscon, CLKGEN, DMA, peripheral Input Muxes, and so on

4 Memory

This section compares the differences between LPC84x and LPC86x in terms of memory. For the memory comparison of LPC844, LPC845, and LPC86x, see Table 5.

Table 5. LPC84x and LPC86x memory comparison

Memory	LPC844	LPC845	LPC86x
Flash	64 kB 0x0000_0000 - 0x0001_0000	64 kB 0x0000_0000 - 0x0001_0000	64 kB 0x0000_0000 - 0x0001_0000
SRAM	8 kB 0x1000_0000 - 0x1000_2000	16 kB 0x1000_0000 - 0x1000_4000	8 kB 0x1000_0000 - 0x1000_2000
Boot ROM	16 kB 0x0F00_0000 - 0x0F00_4000	16 kB 0x0F00_0000 - 0x0F00_4000	8 kB 0x0F00_0000 - 0x0F00_2000

4.1 Flash memory

The flash size of LPC84x and LPC86x is 64 kB, but the LPC86x flash enhances with 32 Bytes cache and line buffers to improve the code execution performance.

4.2 SRAM

The SRAM size as follows:

- LPC86x is 8 kB
- LPC845 is 16 kB
- LPC844 is 8 kB

Note: *For the LPC845, there are 8 kB RAM shared with MTB.*

4.3 ROM

The LPC86x ROM is only 8 kB and only supports the UART ISP function, but it supports SCRP to improve Code Read Protection compared to the LPC84x series. The LPC86x ROM API only supports the FRO setting.

The LPC84x ROM supports more functions than LPC86x, including ROM divider API, FAIM setting, and so on.

4.4 FAIM

The LPC86x do not support FAIM, but the LPC84x supports 256-bit memory for FAIM.

5 Clock distribution

Compared the LPC84x and LPC86x FRO default setting on 48 MHz, which supports three frequencies 60 MHz, 48 MHz, and 36 MHz. The LPC86x supports 1 MHz LPOSC, and LPOSC is the only source for Window Watchdog Timer. See Figure 2 for the clock distribution of LPC86x.

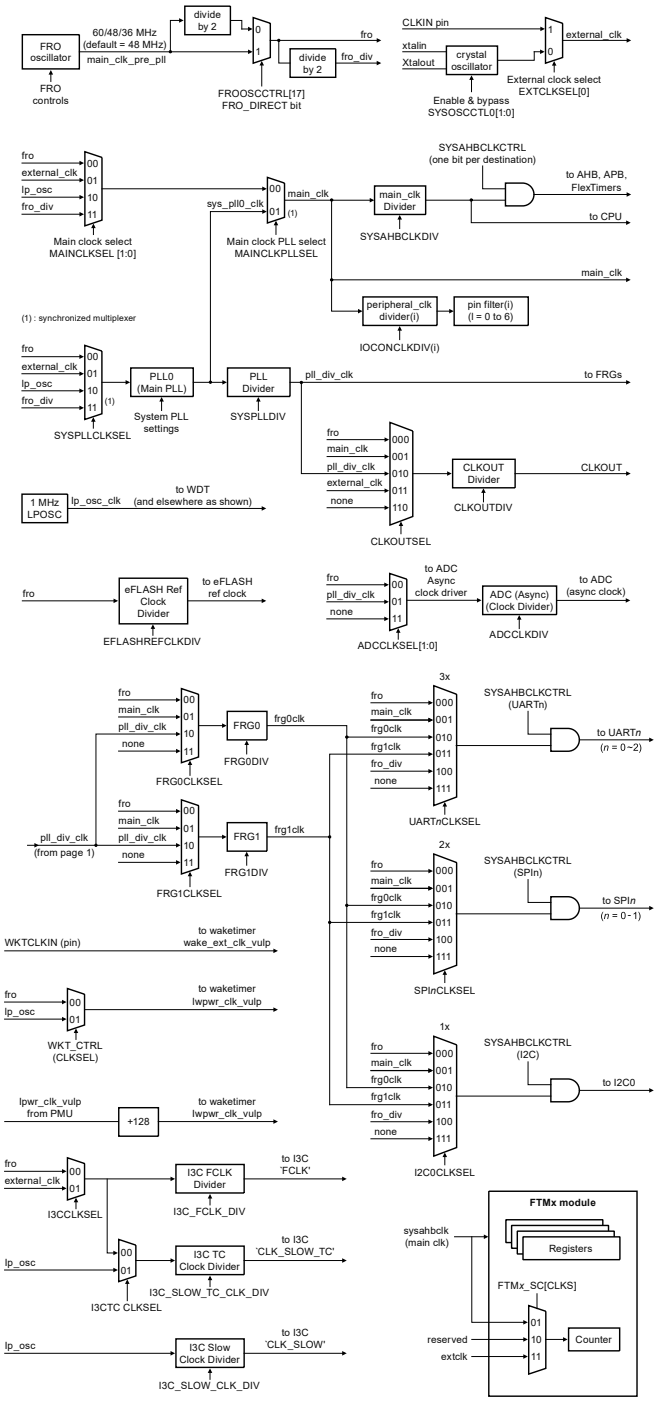

Figure 2. LPC86x clock generation diagram

6 Pinout

For the LP86x in LQFP64, HVQFN48, and HVQFN32 packages, its pin assignment is compatible with LPC84x. The number and position of PIO pins are the same, see Figure 3. But, in the Switch-Matrix table, some functions are different for FlexTimer pins. For more details on the pin assignment of each peripheral, see Figure 3.

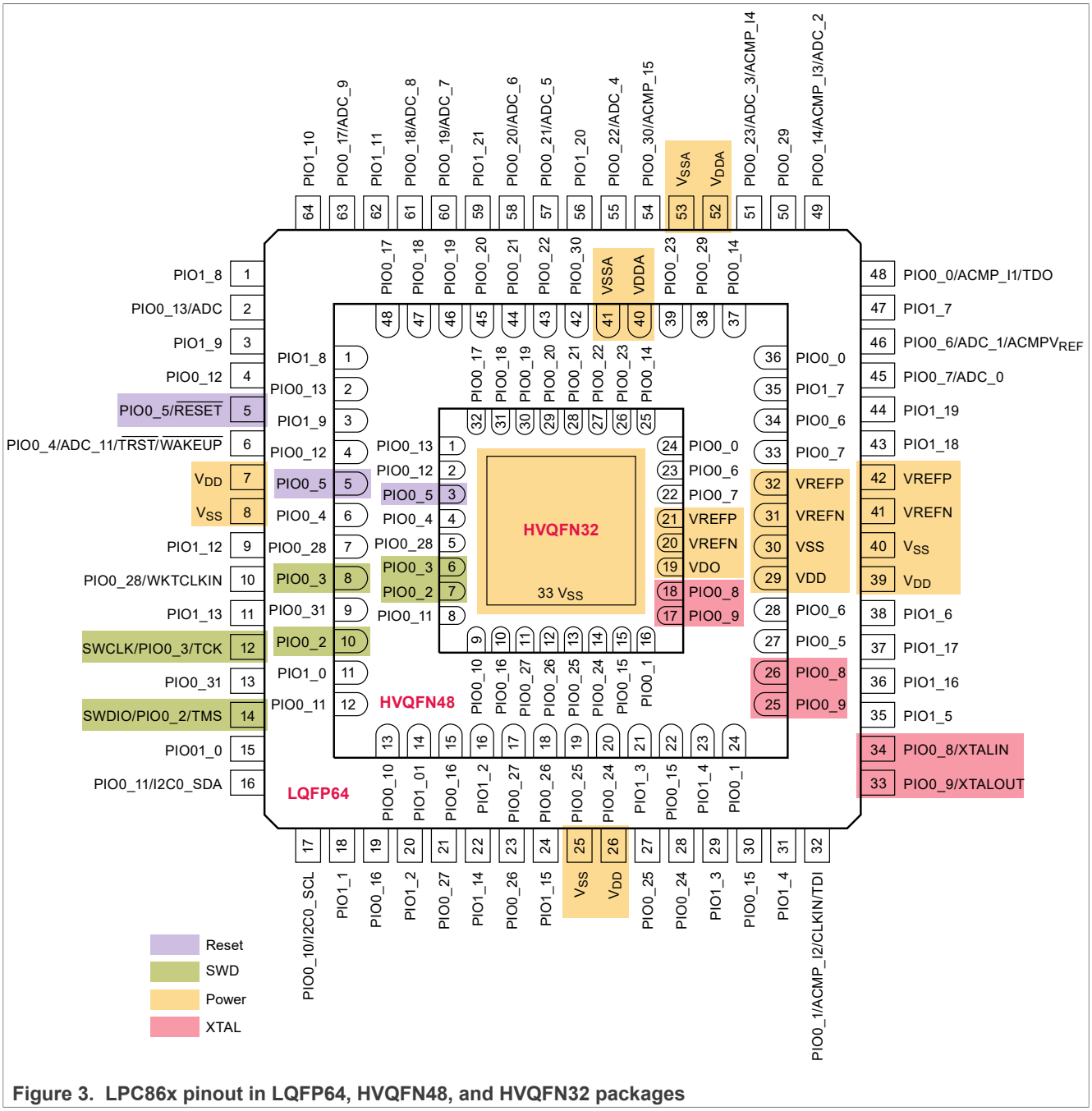

Figure 3. LPC86x pinout in LQFP64, HVQFN48, and HVQFN32 packages

7 Analog

The LPC86x enhanced the ADC sampling performance, and the others are the same as LPC84x.

7.1 ADC

The LPC84x and LPC86x both have one ADC module. The number of external channels for different packages supports the same 12 channels, see Table 6. The ADC input function can be enabled through Switch-Matrix register `PINENABLE0` but enable bits are different between LPC84x and LPC86x.

The LPC86x ADC sampling performance improves from 1.2 Msps (was in LPC84x) to 1.9 Msps. The LPC86x can use ADC channel 0 links to internal PMU 0.9 V voltage reference by setting SYSCON register, 0.9 V voltage reference actual value is stored with pert ID and can be read from IAP command.

Table 6. ADC input pin assignment and SWM configuration bit of LPC84x and LPC86x

LQFP64	HVQFN48	HVQFN32	Pin Name	ADC Pin	LPC84x PINENABLE0	LPC86x PINENABLE0
45	33	22	PIO0_7	ADC_0	bit 14	bit 12
46	34	23	PIO0_6	ADC_1	bit 15	bit 13
49	37	25	PIO0_14	ADC_2	bit 16	bit 14
51	39	26	PIO0_23	ADC_3	bit 17	bit 15
55	43	27	PIO0_22	ADC_4	bit 18	bit 16
57	44	28	PIO0_21	ADC_5	bit 19	bit 17
58	45	29	PIO0_20	ADC_6	bit 20	bit 18
60	46	30	PIO0_19	ADC_7	bit 21	bit 19
61	47	31	PIO0_18	ADC_8	bit 22	bit 20
64	48	32	PIO0_17	ADC_9	bit 23	bit 21
2	2	1	PIO0_13	ADC_10	bit 24	bit 22
6	6	4	PIO0_4	ADC_11	bit 25	bit 23

7.1.1 Analog Comparator (ACMP)

The LPC84x and LPC86x both have one ACMP module. The number of inputs supported for different packages depends on the package, 5x inputs for LQFP64 and HVQFN48 and 4x inputs for HVQFN32. For the pin assignment and SWM configuration setting, see Table 7.

Table 7. ACMP input pin assignment and SWM configuration bit of LPC84x and LPC86x

LQFP64	HVQFN48	HVQFN32	Pin Name	ACMP Pin	LPC84x PINENABLE0	LPC86x PINENABLE0
48	36	24	PIO0_0	ACMP_I1	bit 0	bit 0
32	24	16	PIO0_1	ACMP_I2	bit 1	bit 1
49	37	25	PIO0_14	ACMP_I3	bit 2	bit 2
51	39	26	PIO0_23	ACMP_I4	bit 3	bit 3
54	42	-	PIO0_30	ACMP_I5	bit 4	bit 4

8 Timers

The LPC86x uses FlexTimer (FTM0 and FTM1) to replace SCT and CTimer32, FlexTimer can support motor control applications.

8.1 Timer - FlexTimer (FTM)

Two FlexTimers are implemented on the LPC86x, and both FlexTimers are 16-bit counters. The first FlexTimer FTM0 provides six channels and includes support for motor control, including fault control. The second FlexTimer FTM1 provides four channels; this timer does not have fault control but includes a quadrature encoder.

Both FlexTimers are provided with a selection of hardware triggers. Both FlexTimers are DMA supported:

- FTM0 can be replaced as a part of SCT features on LPC84x
- FTM1 can be replaced as a part of CTimer32 features on LPC84x, CTimer 32-bit

As compared to the LPC84x, the LPC86x FlexTimer function pins can only be placed to a selection of up to three pins through the Switch-Matrix using FTM_PINASSIGN0 and FTM_PINASSIGN1 registers, see Table 8. The SCT and CTimer32 function pins can be assigned to any PIO pins through the Switch-Matrix.

Table 8. FlexTimer pin assignments

Function Name	Type	Selection 0	Selection 1	Selection 2	Selection 3	FTM_PINASSIGN0	FTM_PINASSIGN1
FTM0_EXTCLK	I	P0_24	P0_30	-	Not connected	bit 1:0	-
FTM0_CH0	I/O	P0_17	P1_1	-	Not connected	bit 3:2	-
FTM0_CH1	I/O	P0_18	P1_2	P0_16	Not connected	bit 5:4	-
FTM0_CH2	I/O	P0_19	P1_3	P1_2	Not connected	bit 7:6	-
FTM0_CH3	I/O	P0_20	P1_4	P0_27	Not connected	bit 9:8	-
FTM0_CH4	I/O	P0_21	P1_5	P0_25	Not connected	bit 11:10	-
FTM0_CH5	I/O	P0_22	P1_6	P0_24	Not connected	bit 13:12	-
FTM0_FAULT0	I	P0_10	P1_7	P0_28	Not connected	bit 15:14	-
FTM0_FAULT1	I	P0_11	P1_12	P1_3	Not connected	bit 17:16	-
FTM0_FAULT2	I	P0_13	P1_13	-	Not connected	bit 19:18	-
FTM0_FAULT3	I	P0_23	P1_14	-	Not connected	bit 21:20	-
FTM1_EXTCLK	I	P0_25	P0_29	-	Not connected	bit 23:22	-
FTM1_CH0	I/O	P0_15	P1_8	-	Not connected	bit 25:24	-
FTM1_CH1	I/O	P0_16	P1_9	-	Not connected	bit 27:26	-
FTM1_CH2	I/O	P0_26	P0_31	-	Not connected	bit 29:28	-
FTM1_CH3	I/O	P0_27	P1_0	-	Not connected	bit 31:30	-
FTM1_QD_PHA	I	P0_24	P0_29	-	Not connected	-	bit 1:0
FTM1_QD_PHB	I	P0_25	P0_30	-	Not connected	-	bit 3:2

8.2 Multi-Rate Timer (MRT)

The LPC86x has a standard four-channel MRT, which is same as the LPC84x series.

8.3 Windowed Watchdog Timer (WWDT)

The LPC86x provides the same WWDT as LPC84x. The only difference is that LPC86x WWDT uses 1 MHz LPOSC as the only clock source, but the LPC84x uses a programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.

Note: *Once these WWDT bits are set, there should be no way for software to halt the 1 MHz LPOSC – including when entering a Low-power mode.*

8.4 Wake-up Timer (WKT)

The LPC86x provides the same WKT as LPC84x, but the LPC86x WKT clock source can select from LPOSC/FRO (1 MHz), ULPOSC (10 kHz) in PMU and external WKTCLKIN input pin.

The LPC84x WKT clock source only supports FRO, ULPOSC in PMU, and external WKTCLKIN input pins.

9 Peripherals

This section lists the information about I3C, USART, SPI, I2C, and GPIO pins.

9.1 I3C

The LPC86x support one master/slave I3C interface. This I3C IP supports I3C v1.1. The I3C function pins can be assigned to any PIO pins through Switch-Matrix.

9.2 USART

The LPC86x provides the same USART IP as LPC84x, but the LPC86x enhances the USART feature with received idle timeout status detection and interrupt support.

9.3 SPI

The LPC86x use the same SPI IP as LPC84x.

9.4 I2C

The LPC86x use the same I2C IP as LPC84x.

9.5 Pin and GPIO

The LPC86x all I/O default to GPIO inputs with High-Z (tri-state) status after reset except for the I2C bus true open-drain pins `PIO0_10` and `PIO0_11`.

For the LPC84x, all I/O default to GPIO inputs with internal pull-up resistors, enabled after reset, except for the I2C bus true open-drain pins `PIO0_10` and `PIO0_11`.

By default, both the LPC86x and LPC84x GPIO function are selected except on the pins `PIO0_2`, `PIO0_3`, and `PIO0_5`.

10 System

This section lists the details about the reset and boot.

10.1 Reset and boot

The LPC84x and LPC86x use `PIO0_12` as the ISP entry pin; when `PIO0_12` is pulled low on reset, the part enters ISP mode, and the ISP command handler startup.

The boot-up timings between the LPC86x and LPC84x are different, see Figure 4 and Table 9.

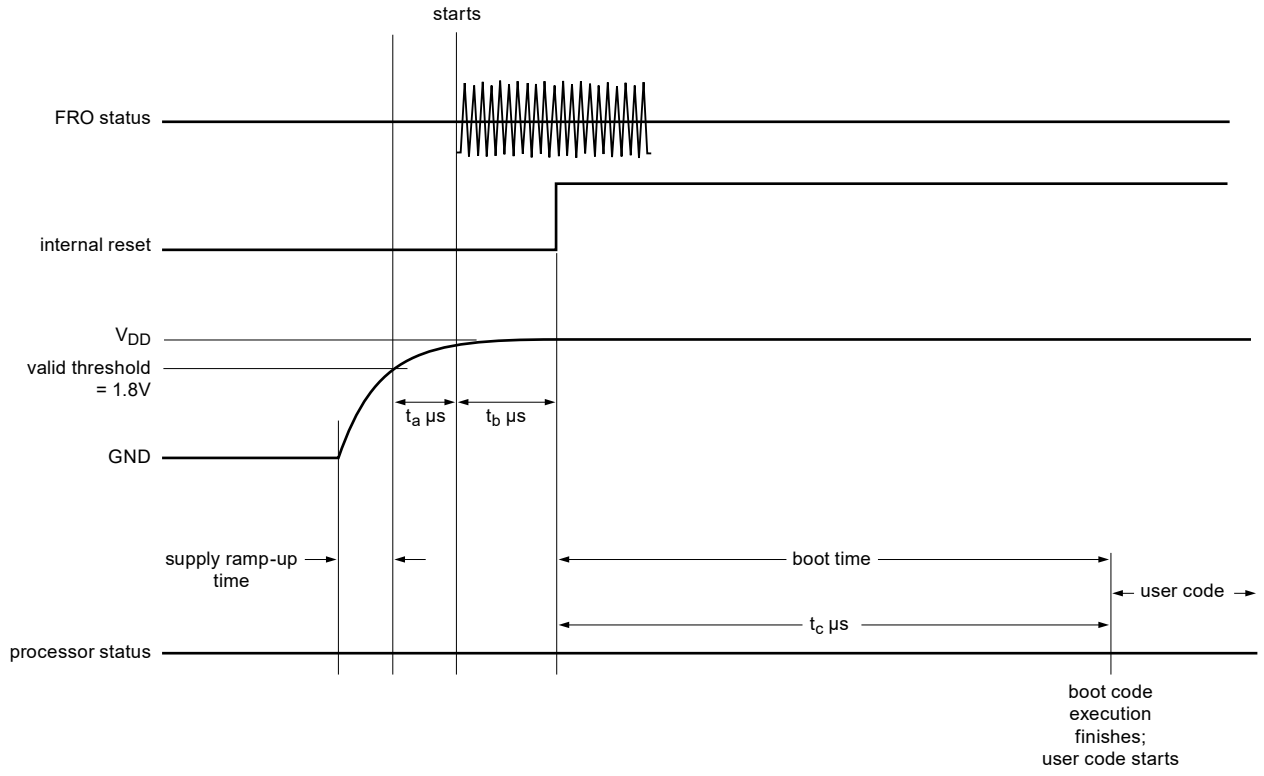

Figure 4. Startup timing

Table 9. Typical startup timing parameters

Parameter	Description	LPC84x	LPC86x
ta	FRO start time	≤ 26 µS	≤ 9.2 µS
tb	Internal reset deasserted	101 µS	54 µS
tc	Boot time	51 µS	99 µS

11 Software

This section lists the details about SDK startup file, SDK linker file, ROM API, SCRP, and CRP.

11.1 SDK startup file

Compared with the LPC84x, and the LPC86x changed some peripheral modules, so their interrupt vector table is different, see Table 10.

Table 10. Interrupt vector table comparison

Address	Vector	Interrupt number	LPC84x source module	LPC86x source module
Arm core system handler vectors				
0x0000_0000	0	-	CSTACK	CSTACK
0x0000_0004	1	-	Reset_Handler	Reset_Handler
0x0000_0008	2	-	NMI	NMI

Table 10. Interrupt vector table comparison*...continued*

Address	Vector	Interrupt number	LPC84x source module	LPC86x source module
Arm core system handler vectors				
0x0000_000C	3	-	HardFault	HardFault
0x0000_0010	4	-	-	-
0x0000_0014	5	-	-	-
0x0000_0018	6	-	-	-
0x0000_001C	7	-	-	-
0x0000_0020	8	-	-	-
0x0000_0024	9	-	-	-
0x0000_0028	10	-	-	-
0x0000_002C	11	-	SVCall	SVCall
0x0000_0030	12	-	-	-
0x0000_0034	13	-	-	-
0x0000_0038	14	-	PendSV	PendSV
0x0000_003C	15	-	Systick	Systick
External Interrupts				
0x0000_0040	16	0	SPI0 interrupt	SPI0 interrupt
0x0000_0044	17	1	SPI1 interrupt	SPI1 interrupt
0x0000_0048	18	2	DAC0 interrupt	Reserved
0x0000_004C	19	3	USART0 interrupt	USART0 interrupt
0x0000_0050	20	4	USART1 interrupt	USART1 interrupt
0x0000_0054	21	5	USART2 interrupt	USART2 interrupt
0x0000_0058	22	6	Reserved	FlexTimer0 interrupt
0x0000_005C	23	7	I2C1 interrupt	FlexTimer1 interrupt
0x0000_0060	24	8	I2C0 interrupt	I2C0 interrupt
0x0000_0064	25	9	SCT timer interrupt	Reserved
0x0000_0068	26	10	MRT timer interrupt	MRT timer interrupt
0x0000_006C	27	11	comparator interrupt	comparator interrupt
0x0000_0070	28	12	watchdog interrupt	watchdog interrupt
0x0000_0074	29	13	BOD interrupt	BOD interrupt
0x0000_0078	30	14	Flash interrupt	Flash interrupt
0x0000_007C	31	15	WKT timer interrupt	WKT timer interrupt
0x0000_0080	32	16	ADC sequence A completion interrupt	ADC sequence A completion interrupt
0x0000_0084	33	17	ADC sequence B completion interrupt	ADC sequence B completion interrupt
0x0000_0088	34	18	ADC threshold compares interrupt	ADC threshold compares interrupt

Table 10. Interrupt vector table comparison*...continued*

Address	Vector	Interrupt number	LPC84x source module	LPC86x source module
Arm core system handler vectors				
0x0000_008C	35	19	ADC overrun interrupt	ADC overrun interrupt
0x0000_0090	36	20	DMA0 interrupt	DMA0 interrupt
0x0000_0094	37	21	I2C2 interrupt	I3C0 interrupt
0x0000_0098	38	22	I2C3 interrupt	GPIO group A interrupt
0x0000_009C	39	23	CTimer32 interrupt	GPIO group B interrupt
0x0000_00A0	40	24	Pin interrupt 0	Pin interrupt 0
0x0000_00A4	41	25	Pin interrupt 1	Pin interrupt 1
0x0000_00A8	42	26	Pin interrupt 2	Pin interrupt 2
0x0000_00AC	43	27	Pin interrupt 3	Pin interrupt 3
0x0000_00B0	44	28	Pin interrupt 4	Pin interrupt 4
0x0000_00B4	45	29	Pin interrupt 5	Pin interrupt 5
0x0000_00B8	46	30	Pin interrupt 6	Pin interrupt 6
0x0000_00BC	47	31	Pin interrupt 7	Pin interrupt 7

11.2 SDK linker file

As default in the section SRAM memory, the SRAM sizes of LPC84x and LPC86x are different, so in the linker file, the address of the usable SRAM is also different. For detail, see Table 11.

Table 11. SRAM address range in the link file of LPC84x and LPC86x

Define symbol	LPC845 SRAM address	LPC86x SRAM address
m_data_start	0x10000000	0x10000000
m_data_end	0x10003FFF	0x10001FFF

11.3 ROM API

The LPC84x ROM code provides divider API, but the LPC86x does not. For details about divider ROM code in library format under Keil, IAR, and MCUXpresso IDEs, refer to *Programming LPC800 Using USART ISP* (document AN13815).

11.4 SCRP and CRP

The LPC86x improves the CRP mechanism based on LPC84x, which call SCRP (Strength Code Read Protection). The LPC84x and LPC86x CRP pattern values are programmed in 0x0000_02FC, but the pattern value is different, see Table 12.

Table 12. SCRP / CRP modes pattern values

Name	LPC84x	LPC86x	Description
	Pattern programmed in 0x0000_02FC	Pattern programmed in 0x0000_02FC	
NO_ISP	0x4E697370	0x536AAC95	Access to the chip via the SWD pins is enabled. Prevents sampling of the pins for entering ISP

Table 12. SCRP / CRP modes pattern values*...continued*

Name	LPC84x	LPC86x	Description
	Pattern programmed in 0x0000_02FC	Pattern programmed in 0x0000_02FC	
			mode. ISP sampling pin is available for other applications.
CRP0/NO_CRP	0xFFFFFFFF	0xFFFFFFFF	All USART ISP commands are supported.
CRP1	0x12345678	0x5963A69C	Access to the chip via the SWD pins is disabled. This mode allows partial flash update using the following USART ISP commands and restrictions: • Write to RAM command cannot access RAM below 0x1000 0600. Access to addresses below 0x1000 0600 is disabled. • Copy RAM to flash command cannot write to Sector 0. • Erase command can erase Sector 0 only when all sectors are selected for erase. • Compare command is disabled. • Read Memory command is disabled. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased. Since compare command is disabled in case of partial updates the secondary loader should implement checksum mechanism to verify the integrity of the flash.
CRP2	0x87654321	0x963569CA	Access to chip via the SWD pins is disabled. The following ISP commands are disabled: • Read Memory • Write to RAM • Go • Copy RAM to flash • Compare When CRP2 is enabled the ISP erase command only allows erasure of all user sectors.
CRP3	0x43218765	0x63599CA6	Access to chip via the SWD pins is disabled. ISP entry selected via the ISP entry pin is disabled if a valid user code is present in flash sector 0. This mode effectively disables ISP override using the entry pin. It is up to the application of the user to provide a flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via USART. ***CAUTION:*** *If CRP3 is selected, no future factory testing can be performed on the device.*
Others	No Support	Others	All the value other than mentioned above are treated as CRP2.

12 Conclusion

This application note compares the system resources and software differences between the LPC84x and LPC86x. Users can refer to this document quickly to migrate projects from the LPC84x to LPC86x.

13 References

- *LPC84x User Manual* (document UM11029)
- *LPC86x User Manual* (document UM11607)

14 Revision history

Table 13 summarizes the changes done to this document since the initial release.

Table 13. Revision history

Revision number	Date	Substantive change
0	22 May 2022	Initial release

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