AN14249

Migration Guide from LPC55xx to MCX Nx4x

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Document information

Information	Content
Keywords	AN14249, migration guide
Abstract	This document provides an overview of the differences between the LPC55xx and MCX Nx4x chips and helps to migrate from LPC55xx to MCX Nx4x.

1 Introduction

This document provides an overview of the differences between the LPC55xx and MCX Nx4x chips and helps to migrate from LPC55xx to MCX Nx4x. The migration between these chips requires the software changes. This document describes the changes require to migrate from LPC55xx to MCX Nx4x. LPC553x, LPC556x, and MCX Nx4x are used as the examples in this document.

This guide is released along with the relevant device specific hardware documentation such as data sheets, reference manuals, and application notes available on nxp.com.

2 Chip comparison

This section compares the main features between the LPC553x, LPC556x, and MCX Nx4x chips.

2.1 MCX Nx4x series overview

The MCX Nx4x chip is based on the Arm Dual Cortex-M33 core and operates at the speed of up to 150 MHz and provide for industrial and consumer IoT applications. It has three features:

- Highly secure: TrustZone for Armv8-M, secure boot/update ROM, and the NXP EdgeLock secure subsystem (ELS) S50 black-box secure enclave with key storage and crypto algorithms protected from side-channel attacks as well as internal/external tamper events, flash encryption, external memory interface with on-the-fly PRINCE decryption, options for hardware Physically Unclonable Function (PUF) and Factory Root of Trust programming.
- Industrial Strength: Industrial communication protocol support, 15-year longevity, high-resolution mixed signal analog, CAN-FD, BLDC/PMSM Motor Control support, integrated sensor interfaces (MIPI-I3C, I^2C, SPI).
- Power-efficient:
  - < 75 µA/MHz active current,
  - < 10 µA power-down mode with RTC enabled and 8 kB SRAM retention,
  - < 2.5 µA Deep power-down mode with RTC active and 8 kB SRAM.

2.2 LPC55xx series overview

All LPC55Sxx/LPC55xx families are based on Arm Cortex-M33 core, with PowerQuad accelerator and CASPER accelerator. The **S** in the middle of part name means that this part provides more security features, such as TrustZone support.

- Power-efficient:
  - < 82 µA/MHz active current,
  - < 8 µA Power-down mode with RTC enabled and 8 kB SRAM retention
  - < 2.5 µA Deep power-down mode with RTC active and 4 kB SRAM

2.3 High-level comparison

Table 1. High-level comparison of MCX Nx4x and LPC55xx

Features		LPC55S69	LPC55S36	MCX N947
CPU core platform	M33 @150 MHz	2	1	2
Co-processor	PowerQuad (DSP)	YES	YES	YES
	Smart DMA	—	—	YES
	NPU	—	—	YES

Table 1. High-level comparison of MCX Nx4x and LPC55xx*...continued*

Features		LPC55S69	LPC55S36	MCX N947
	CoolFlux DSP	—	—	YES
	CASPER	YES	—	—
Memory	Flash	640 kB	256 kB	2 MB, Dual bank
	Flash cache	—	8 kB	16 kB
	SRAM	320 kB	Up to 112 kB, no ECC	Up to 480 kB, no ECC
	SRAM ECC	—	16 kB	32 kB
	FlexSPI	—	YES, with **8 kB** cache, supporting XIP, Octal/Quad SPI	YES, with **16 kB** cache, supporting XIP, Octal/Quad SPI
	ROM	YES	YES	YES
Security	EdgeLock	—	—	EdgeLock 50 B
	Secure key management	PUF	PUF/UDF	PUF/UDF
	Secure subsystem	—	YES	YES
	Anti-tamper pin	—	4 × Pins	8 × Pins
General system	DMA	2 × (22 channels/10 channels)	2 × DMA (52 channels/16 channels)	2 × DMA/16 channels each
	CRC	YES	YES	YES
Clocking	FRO-1 MHz	YES	YES	—
	FRO-12 MHz	—	—	YES
	FRO-96/12 MHz	YES	YES	—
	FRO-144 MHz	—	—	YES
	FRO-16 kHz	—	—	YES
	FRO-32 kHz	YES	Yes	—
	32 kHz low-power crystal oscillator	YES, with cap-bank	YES, with cap-bank	YES, with cap-bank
	External crystal oscillator	16 MHz to 32 MHz, with cap-bank	16 MHz to 32 MHz, with cap-bank	16 MHz to 50 MHz low-power crystal oscillator
	PLL	2 ×	2 ×	2 ×
Communication Interface	USART	10 × Flexcomm, each supporting SPI, I^2C, USART, and I^2S	8 × Flexcomm, each supporting SPI, I^2C,USART, and I^2S	10 × LP Flexcomm, each supporting SPI, I^2C, UART
	SPI			
	I^2C			
	I^2S/SAI			2 × SAI
	HighSpeed SPI	1 × 50 MHz	1 × 50 MHz	—
	I^3C	—	1 ×	2 ×
	eSPI	—	—	1 ×

Table 1. High-level comparison of MCX Nx4x and LPC55xx*...continued*

Features		LPC55S69	LPC55S36	MCX N947
	SPI Filter	—	1 ×	YES
	FlexIO	—	—	1 ×
	EVM smart card	—	—	2 ×
	CAN-FD	—	1 ×	2 ×
	HighSpeed USB	1 × Device/Host	—	1 × Device/Host
	Full Speed USB	1 × Device/Host	1 × Device with Crystal-less	1 × Device/Host
	uSDHC	1 ×	—	1 ×
	Ethernet	—	—	1 ×
Analog	ADC	1 × 16-bit ADC with 1.0 Msps, supporting five differential inputs or 10 single-ended inputs	4 × single-ended input 16-bit 2.0 Msps	4 × single-ended input 16-bit 2.0Msps
			2 × differential input 16-bit 2.0 Msps	2 × differential input 16-bit 2.0 Msps
			4 × single-ended input 12-bit 3.2 Msps	4 × single-ended input 12-bit 3.16 Msps
			2 × differential input 12-bit 3.2 Msps	2 × differential input 12-bit 3.16 Msps
	DAC	—	3 × 12-bit DAC 1 Msps	2 × 12-bit 1 Msps 1 × 14-bit 5 Msps
	Comparator	1 × with 5 inputs	—	—
	High-speed comparator	—	3 ×	3 × High Speed, with 17 inputs
	Opamp	—	4 ×	3 ×
	Accurate V_{ref}	—	—	YES
Motor control subsystem	FlexPWM	—	2 × FlexPWM (4 submodule for each)	2 × FlexPWM (4 submodule for each)
	ENC/QEI/QDC	—	2 × QEI	2 × ENC
	Event generator	—	—	1 × (including two AOI)
	AOI	—	2 ×	—
	SINC filter	—	—	YES (third order, 5-ch)
Timers	CTimer	5 × 32-bit	5 × 32-bit	5 × 32-bit
	SCTimer/PWM	1 × 32-bit or 2 × 16-bit	1 × 32-bit or 2 × 16-bit	1 × 32-bit or 2 × 16-bit
	LPTimer	—	—	1 ×
	Encoder	—	—	1 ×

Table 1. High-level comparison of MCX Nx4x and LPC55xx*...continued*

Features		LPC55S69	LPC55S36	MCX N947
	Frequency measurement timer	1 ×	1 ×	1 ×
	Multi-Rate Timer (MRT)	4 ×	4 ×	1 ×
	Windowed Watchdog timer	1 ×	1 ×	1 ×
	RTC	RTC without calendar	RTC with calendar	RTC with calendar
	Micro Timer	1 ×	1 ×	1 ×
	OS Event Timer	1 ×	1 ×	1 ×
HMI	Digital PDM Microphone	No	1 ch - Allows connection of up to 2 × MEMS	Supporting the connection of up to four MEMS
	Capacitive Touch Sensor Interface (TSI)	No	No	Up to 25 self-channels, and up to 8 TX × 17 RX mutual-cap channels
	GPIO	64 GPIOs on HLQFP100 36 GPIOs on HTQFP64	66 GPIOs on HLQFP100 39 GPIOs on HTQFP64	Up to 124 × GPIOs on VFBGA184, 100 MHz IO on P2 and P3
Operation Details	Internal Core Buck DC-DC	YES	YES, 1.8 V to 3.6 V	YES
	Internal Core LDO	No	YES, 1.8 V to 3.6 V	YES
	Always On Domain on `VDD_VBAT` pin	No	YES, 1.71 V to 3.6 V	YES
	Operating Voltage	1.8 V to 3.6 V	1.8 V to 3.6 V	1.71 V to 3.6 V
	IOs	1.8 V to 3.6 V	`VDDIO_1` is 1.8 V - 3.6 V. `VDDIO_2` is 1.08 V to 3.6 V.	1.71 V to 3.6 V at full-performance 1.2 V supporting at reduced performance
	VHBM	± 2000 V	± 2000 V	+-± 2000 V
	VCDM	± 500 V	± 500 V	± 500 V
Package	VFBGA184	—	—	YES
	HLQFP100	YES	YES	YES
	VFBGA98	YES	—	—
	HTQFP64	YES	YES	—
	HVQFN48	—	YES	—

3 System modules comparison

3.1 Memory system difference

3.1.1 Memory system on LPC55xx

Table 2. Memory system on LPC55xx

Memory type	Start address	Size	MCU	Comment
Internal Flash	0x0000 0000	Up to 640 kB	All LPC55xx	—
SRAM	0x2000 0000	Up to 272 kB	All LPC55xx	SRAM on CM33 data bus
SRAM X	0x0400 0000	Up to 32 kB	All LPC55xx	SRAM X on CM33 code bus
FlexSPI	0x0800 0000	Up to 128 MB	Only LPC553x	—
Boot ROM	0x0300 0000	Up to 192 kB	All LPC55xx	On CM33 code bus

3.1.2 Memory system on MCX Nx4x

Table 3. Memory system on MCX Nx4x

Memory type	Start address	Size	MCU	Comment
Internal Flash	0x0000 0000	Up to 2 MB	All MCX Nx4x	—
SRAM	0x2000 0000	Up to 512 kB, including ECC RAM	All MCX Nx4x	SRAM on CM33 data bus
SRAM X	0x0400 0000	96 kB	All MCX Nx4x	SRAM X on CM33 code bus
FlexSPI	0x0800 0000	Up to 128 MB	All MCX Nx4x	—
Boot ROM	0x0300 0000	256 kB	All MCX Nx4x	On CM33 code bus

3.1.3 Memory system comparison

On the MCX Nx4x chips, the memory address is compatible with LPC55xx series.

3.2 Clocking differences

The system clocking module provides the clock signals to the core, memories, and peripherals (register interfaces and peripheral clocks).

3.2.1 Clocking diagram on LPC55xx

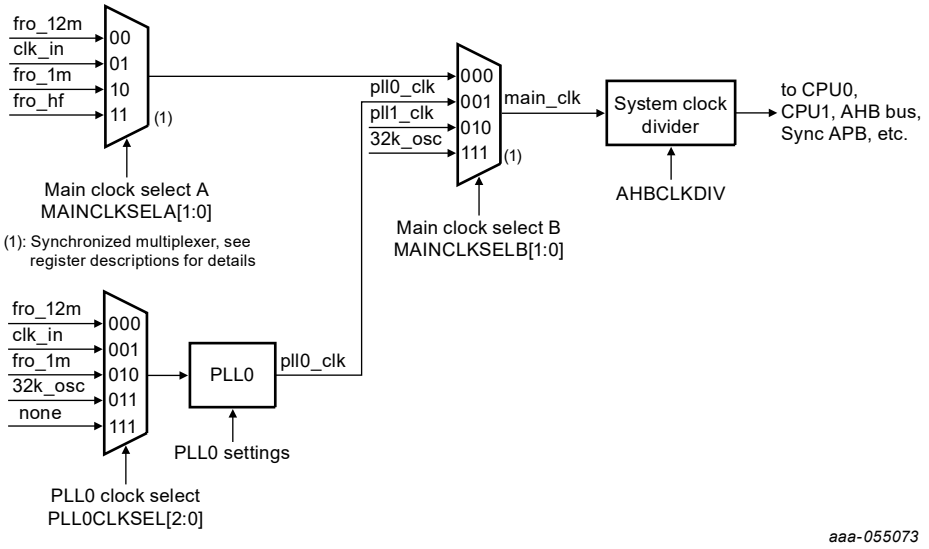

Figure 1. LPC55xx CPU, AHB, and APB bus clock diagram

3.2.2 Clocking diagram on MCX Nx4x

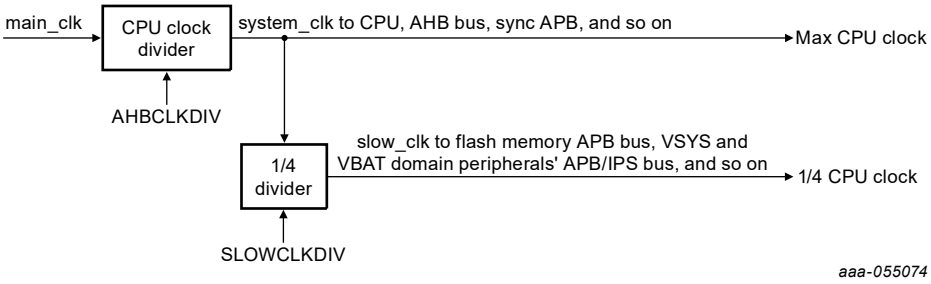

Figure 2. MCX Nx4x CPU, AHB, and APB bus clock diagram

MCX Nx4x series added SLOW clock (1/4 CPU clock) to flash memory, APB bus, and other domain. LPC55xx series do not have this clock.

3.2.3 Clock feature comparison

Table 4. Comparison of MCX Nx4x and LPC55xx clock features

Feature	MCX Nx4x	LPC55xx
Maximum core frequency	150 MHz	150 MHz
PLL	2 × PLL up to 550 MHz	2 × PLL up to 550 MHz
External oscillator	16 MHz to 50 MHz 32.768 kHz	16 MHz or 32 MHz 32.768 kHz
Internal FRO	FRO: 144 MHz FRO: 12 MHz FRO: 16 kHz	FRO: 96/12 MHz FRO: 1 MHz FRO: 32 kHz

4 Peripheral module comparison

4.1 Changed modules

4.1.1 SYSCON

The whole SYSCON module is changed, but the functionality remains similar.

4.1.2 Internal Flash Memory

The whole Flash module is changed, but the functionality remains similar.

Table 5. Comparison of internal flash

Feature	Description	MCXN	LPC55xx
Flash array • Phrase	It represents the smallest portion of the flash memory that can be programmed in one operation.	16 bytes	The LPC55xx does no have flash phrase, and the LPC55xx minimum program size is 512 bytes.
Flash array • Sector	It represents the smallest portion of the flash memory that can be erased in one operation.	8 kB	The minimum erase size is 512 bytes.
Flash array • Page	It represents the largest portion of the flash memory that can be programmed in one operation.	128 bytes	512 bytes
Flash memory controller • Prefetch buffer	It prefetches the next 128-bit flash memory location.	16 bytes	—
Flash memory controller • Cache	Flash Cache memory stores already fetched data. This code is immediately available for repeated execution without any wait states, if needed. It is a one set, four-way associative cache with 128-bit (or 16-byte) size entries.	64 bytes	—
Functional safety • Flash ECC		• One-bit error correction. • Two-bit error detection capability	One-bit error correction
Functional safety • Flash ERM	ERM provides information and optional interrupt notification on memory ECC and parity error events.	Report ECC two- bit error	—
Functional safety • Flash EIM	EIM provides a method for diagnostic coverage of internal memories. It enables you to induce artificial errors on error-checking mechanisms.	• One-bit error injection • Two-bit error injection	—
Flash performance • Access frequency	Configured by FCTRL[RWSC] or FLASHTIM	150 MHz/4 = 37.5 MHz; when RWSC = 3	• 150 MHz, when FLASHTIM = 0xB, 12 system clocks flash access time.

Table 5. Comparison of internal flash*...continued*

Feature	Description	MCXN	LPC55xx
			• 100 MHz, when FLASHTIM = 0x7, eight system clocks flash access time. • 12 MHz, when FLASHTIM = 0x1, two system clocks flash access time.

4.1.3 IOCON to PORT comparison

MCX Nx4x uses PORT to replace the IOCON of LPC55xx, but the functionality remains similar.

4.1.4 GPIO

The whole GPIO module is changed, but the functionality remains similar.

The GPIO of MCX Nx4x supports 1.2 V at the reduced performance (available only on Fast pads).

The GPIO of MCX Nx4x supports 1.71 V -~ 3.6 V IO supply range.

LPC553x supports two main IO supplies: `VDDIO_1` is 1.8 V to 3.6 V, and `VDDIO_2` is 1.08 V to 3.6 V.

LPC556x only supports 1.8 V to 3.6 V.

4.1.5 Real Time Calendar (RTC)

The RTC module is changed, but the functionality remains similar.

4.1.6 Low-power Timer (LPTMR) and WKT

LPC55xx series integrate with WKT, and MCX N series have this LPTMR feature. The LPTMR and WKT functionality remains similar.

You can configure LPTMR to operate as a time counter with an optional pre-scaler, or as a pulse counter with an optional glitch.

Filter, across all power modes, includes low-power modes. It is reset only on VSYS warm reset, allowing it to be used as a time-of-day counter.

4.1.7 I^3C

The I^3C module is updated on MCX Nx4x, but the functionality remains similar.

4.1.8 Controller Area Networ (CAN)

LPC556x series do not have CAN module. LPC553x and MCX Nx4x have the CAN module.

The whole CAN module is changed, but the functionality remains similar. Both of them support CAN2.0 and CAN-FD.

4.1.9 Flexcomm and `LP_Flexcomm`

LPC55xx series use Flexcomm linked with USART, SPI, I^2C, and I^2S serial peripherals.

MCX Nx4x series use `LP_Flexcomm` linked with LPUART, LPSPI, and LPI2C.

The whole UART module is changed, but the functionality remains similar.

The whole I^2C module is changed, but the functionality remains similar.

The whole SPI module is changed, but the functionality remains similar. LPSPI on MCX Nx4x supports 4-bit mode where SPI of LPC553x and LPC556x does not support.

4.1.10 I^2S and Serial Audio Interface (SAI)

LPC55xx series use I^2S interface from Flexcomm to connect audio codec. MCX Nx4x uses the SAI interface connected with audio codec. The I^2S and SAI functionalities remain similar.

4.1.11 DMIC and MICFIL

LPC553x series use Digital Microphone (DMIC) interface to receive Pulse Density Modulated (PDM) data from multiple digital microphones and process it to produce 24-bit PCM data.

MCX Nx4x uses PDM Microphone Interface (MICFIL) delivers audio from microphones to the processor in several applications, such as mobile telephones. As the current digital audio systems use a multi-bit audio signal (also known as multi-bit PCM) to represent the signal, this module implements the required digital interface (a series of filters) to transform a PDM microphone bitstream into a 24-bit PCM signal in the audio band, at a configurable output sample rate.

Both DMIC and MICFIL functionalities remain similar.

4.1.12 USB

The whole USB module is changed, but the functionality remains similar.

4.1.13 Secure Digital Input Outpu (SDIO)

LPC553x series do not integrate with SDIO.

LPC556x has one SDIO. The whole SDIO module is changed on MCX Nx4x, but the functionality remains similar.

4.1.14 Semaphores2 (SEMA42) and Inter-CPU mailbox

LPC55xx series integrate Inter-CPU mailbox and MCX N series have this SEMA42 feature. The SEMA42 and Inter-CPU mailbox functionality remains similar.

SEMA42 is a memory-mapped module that provides robust hardware support needed in multi-core systems for implementing semaphores and provides a simple mechanism to achieve **lock and unlock** operations via a single-write access. The hardware semaphore module provides hardware-enforced gates and other useful system functions related to the gating mechanisms.

4.1.15 Direct Memory Access (DMA)

The whole DMA module is changed, but the functionality remains similar.

4.2 New modules

4.2.1 Core Mode Controller (CMC)

LPC55xx series do not integrate with CMC, but MCX N series have this feature.

CMC provides the sequencing of the CPU and associated logic through the different operating modes.

4.2.2 Interrupt Monitor (INTM)

LPC55xx series do not integrate with INTM, but MCX N series have this feature.

INTM provides a mechanism to monitor the latency of the responses on interrupt requests to ensure that the processing of these critical interrupts executes within the expected time frame, increasing the reliability of the device.

4.2.3 Error Injection Module (EIM)

LPC55xx series do not integrate with EIM, but MCX N series have this feature.

EIM is used for diagnostic purposes. It provides a method for diagnostic coverage of internal memories (for example, system RAM, cache RAMs, and peripheral memories). To determine which functional safety features that this method supports, see the chip-specific EIM information.

EIM enables you to induce artificial errors on error-checking mechanisms of a system, such as ECC for RAM read data and parity bits. For each mechanism that EIM supports on the chip, EIM can inject single-bit and multi-bit inversions on data in the applicable target bus. Injecting faults on memory accesses can be used to exercise the SEC-DED ECC function of the related system.

4.2.4 Error Recording Module (ERM)

LPC55xx series do not integrate with ERM, but MCX N series have this feature.

ERM provides information and optional interrupt notification on memory error events associated with ECC and parity. ERM collects error events on memory accesses for memory arrays, such as flash memory, system RAM, or peripheral RAMs. ERM supports various channels for memory sources where each ERM channel is associated with a different memory module. See the chip-specific ERM information for details about supported memory sources and specific memory channel assignments. If the memory supports ECC, then ERM syndrome and error address information are captured along with the error event. ERM does not capture syndrome or error address for cache memories or memory with parity instead of ECC.

4.2.5 Event Generator (EVTG) and AOI

LPC556x does not have this feature. LPC553x series integrate with AOI. MCX N series integrate with EVTG.

EVTG includes two parts:

- Two AND/OR/INVERT (known as the AOI) modules.
- One configurable flip-flop

It supports the generation of a configurable number of Event signals. The two AOI combinational expressions share the four associated EVTG inputs: An, Bn, Cn, and Dn. You can configure the flip-flop to make the two expressions act as the Reset port, Set port or D port, CLK port or go through to EVTG output with the flip-flop bypassed.

This module is a slave peripheral module-connecting event input indicators from various chip modules and generates event output signals that you can route to an inter-peripheral crossbar switch or other peripherals. You can access its programming model through the standard IPS (sky blue) slave interface. EVTG is configurable in the integrated AOI functionality and flip-flop variety.

4.2.6 Neural Processing Unit (NPU)

LPC55xx series do not integrate with NPU, but MCX N series have this feature.

NPU is dedicated for accelerate machine learning algorithms.

NPU is a configurable architecture comprising three aspects:

- Weight decoding
- Compute engine
- Data canvas

4.2.7 External Watchdog Monitor (EWM)

LPC55xx series do not integrate with EWM, but MCX N series have this feature.

For safety purposes, a redundant watchdog system, EWM, is designed to monitor external circuits and the MCU software flow. This provides a backup mechanism to the internal watchdog that resets the CPU and peripherals of the MCU.

The internal watchdog is used to monitor the flow and execution of the embedded software within the MCU. If allowed to overflow, it consists of a counter that forces an internal and asynchronous reset to all on-chip peripherals. The counter also optionally asserts the `RESET_B` pin to reset external devices and circuits. The watchdog counter must not overflow if the software code works well and services the watchdog to restart the actual counter.

The EWM does not reset the CPU and peripherals of the MCU, making it different from the internal watchdog.

4.2.8 14-bit DAC and 12-bit DAC

LPC556x series do not integrate DAC.

LPC553x has three instances of the 12-bit 1 Msps DAC module, DAC0, DAC1, and DAC2 with a compatible DAC controller.

MCX Nx4x has two instances of the 12-bit 1 Msps DAC module, DAC0, DAC1, with a compatible DAC controller.

MCX Nx4x has of the 12-bit 1 Msps DAC module, with a compatible DAC controller.

MCX Nx4x has one instance of the 14-bit 10 Msps DAC module, DAC2, with a compatible DAC controller.

4.2.9 SINC filter

LPC55xx series do not integrate with SINC Filter, but MCX N series have this feature.

SINC converts an external ADC sigma-delta modulator bitstream to a data stream. The converters are based on:

- A maximum of 3-order sinc digital decimation filters with FastSinc support.
- A maximum selectable Over Sampling Ratio (OSR) of 2048.

You can combine SINC functionality with more software-based filtering.

4.2.10 Touch Sensor Interface (TSI)

LPC55xx series do not integrate with TSI, but MCX N series have this feature.

TSI provides touch sensing detection on capacitive touch sensors. The external capacitive touch sensor is typically formed on a Printed Circuit Board (PCB) and the sensor electrodes are connected to TSI input channels through the I/O pins in the chip. The TSI module operates in a switching-integration style to achieve low-power, high-sensitivity, and advanced ElectroMagnetic Compatibility (EMC) robustness.

The module supports:

- Self-Capacitance mode: In this mode, TSI requires only one pin for each touch sensor.

- Mutual-Capacitance mode: In this mode, TSI performs sensing using a capacitive touch matrix in various TX-RX configurations. TSI requires one pin per TX and RX line.

TSI fully supports the NXP touch library based on SDK, which provides a solid capacitive measurement module for the implementation of touch keyboard, rotaries, and sliders.

4.2.11 FlexIO

LPC55xx series do not integrate with FlexIO, but MCX N series have this feature.

The FlexIO module was first introduced in the Freescale Kinetis KL43 family. It can emulate various serial communication protocols including: UART, SPI, and I^2C. The FlexIO module is flexible, and you can configure it according to your communication needs. The main components of the FlexIO module are the shifters, timers, and pins. Data is loaded onto a shifter and a timer is assigned to generate the shifter clock and use a pin to output the data from the shifter.

4.2.12 Ethernet

LPC55xx series do not integrate Ethernet. MCX N series has one instance of the Ethernet QoS module, ENET0.

The Ethernet module enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard. The Ethernet interface contains a fully-featured 10 Mbps or 100 Mbps Ethernet Media Access Controller (MAC) designed to provide optimized performance by using the DMA hardware acceleration.

4.2.13 USBDCD

LPC55xx series do not integrate with USBDCD feature, but MCX N series have this feature.

USBDCD works with the USB transceiver to detect whether the USB device is attached to a Charging Port, either a Dedicated Charging Port (DCP) or a Charging Downstream Port (CDP). The system software coordinates the detection activities of the module and controls an off-chip integrated circuit that performs the battery charging.

4.2.14 EMVSIM

LPC55xx series do not integrate EMVSIM. MCX N series have two instances of the EMVSIM module, EMVSIM0, and EMVSIM1.

EMVSIM facilitates communication with smart cards that are compatible with these standards:

- EMV v4.3 (Book 1)
- ISO/IEC 7816-3

4.2.15 SmartDMA

LPC55xx series do not integrate SmartDMA in official document. MCX N series has one SmartDMA.

SmartDMA is a core that supports unique, reduced instruction sets. It works in a similar way to the Arm core. Being the controller of the AHB matrix, SmartDMA can access:

- All its targets.

The GPIO peripheral control and data registers.

The purpose of SmartDMA is to perform event- and I/O-driven handling to offload the Arm processor in the system.

4.2.16 Coolflux BSP32

LPC55xx series do not integrate Coolflux BSP32. MCX N series has one Coolflux BSP32 co-processor.

The CoolFlux BSP32 is a programmable digital signal processor, where BSP stands for Baseband Signal Processor and the 32 indicates that is has a 32-bit data path and 32-bit data memories. It is a dual Harvard, dual multiplier processor based on the ultra-low power CoolFlux architecture. It supports 16-bit and 32-bit scalar operations as well as complex and SIMD operations and data types. CoolFlux BSP32 is fully programmable in C and comes with an optimizing compiler and tool suite.

5 Boot mode

5.1 Serial downloader mode

Both MCX Nx4x and LPC55xx chips have the serial downloader mode feature. The serial downloader provides a means to download a program image to the chip via a USB or UART serial connection. In this mode, a host PC can communicate with the ROM bootloader using the serial download protocol. You may use the blhost tool to run the serial downloader. The serial downloader tool is useful in mass production.

5.2 Serial downloader mode

Table 6. Comparison of boot device

—	Boot device	Description
MCX Nx4x	Internal flash Serial Nor flash via FlexSPI Serial Nand flash via FlexSPI	
LPC553x	Internal flash Serial Nor flash via FlexSPI Serial Nand flash via FlexSPI	
LPC556x	Internal flash	Most LPC55xx chips support booting only from the internal flash. LPC55xx has serial flash recover boot.

For more information about the MCX Nx4x boot, see the chip reference manual.

6 Development environment and tools

6.1 Software-supported packages and tools

Table 7. Comparison of software-support packages and tools

	MCX Nx4x	LPC55xx	Description
SDK	MCUXpresso SDK	MCUXpresso SDK	Providing the drivers and examples for the MCX N4x4 and LPC55xx chips.
IDE	IAR KEIL MCUXpresso GCC visual studio code	IAR KEIL MCUXpresso GCC visual studio code	Providing the development IDEs to program, compile, debug, and download.
Debug tool	J-Link	J-Link	Used to debug the software on the chips.

Table 7. Comparison of software-support packages and tools...*continued*

	MCX Nx4x	LPC55xx	Description
	ULINK2 DAP-Link MCU-Link	ULINK2 DAP-Link MCU-Link	
Serial download tool	blhost.exe	blhost.exe	Like the MFG tool, it is used to program images to the boot devices directly using the serial downloader.
Image tool	elftosb.exe	elftosb.exe	Used to generate bootable images, including signed or encrypted images.

7 Hardware design

7.1 Power supply

7.1.1 Power supply on MCX Nx4x chips

MCX Nx4x supports two kinds of power supply mode, power-efficient supply mode, and low-cost supply configuration.

Figure 3 shows a power-efficient configuration of the chip power supplies. This configuration uses the on-chip DCDC_CORE switching regulator to power the VDD_CORE supply rail efficiently.

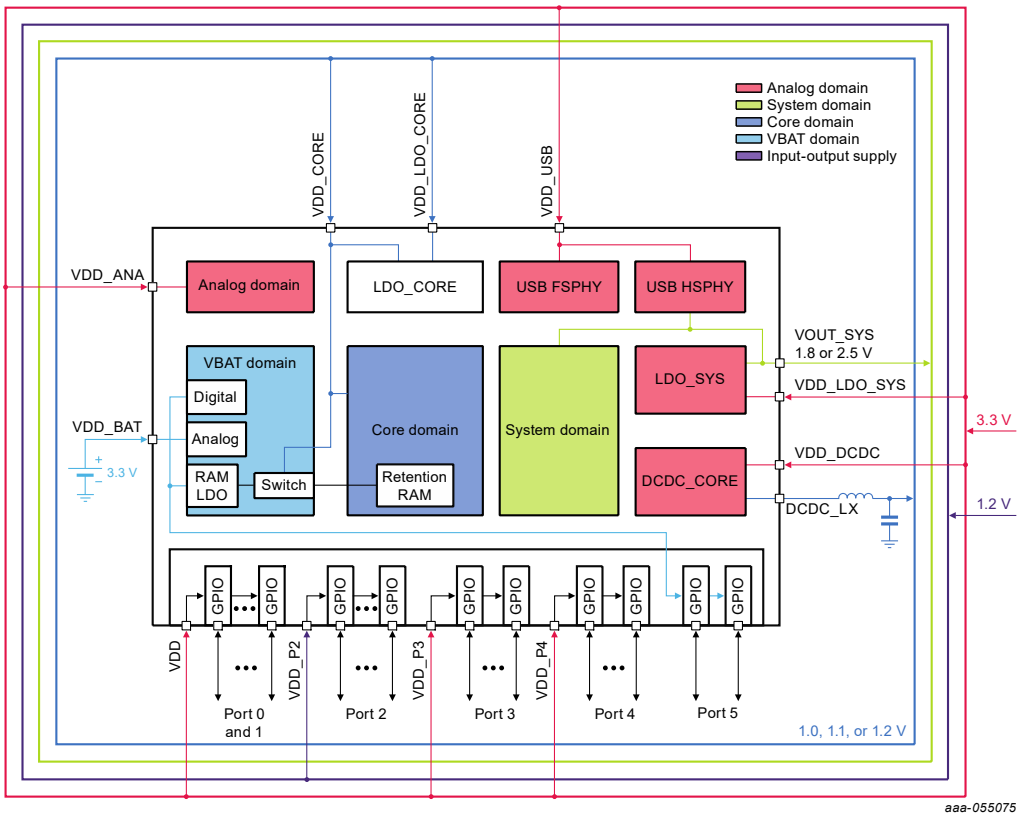

Figure 3. MCX Nx4x power-efficient schematic

Figure 4 shows a low-cost configuration of the chip power supplies. This configuration uses the on-chip LDO_CORE regulator to save cost and eliminate the passive components for the DCDC_CORE regulator.

For packages where VDD_DCDC has an independent pin, you can connect VDD_DCDC and DCDC_LX to GND with a 10-kΩ resistor to disable DCDC. Your software must disable DCDC.

For packages where VDD_DCDC and VDD_LDO_SYS share a package pin, to disable DCDC, float the DCDC_LX and disable DCDC.

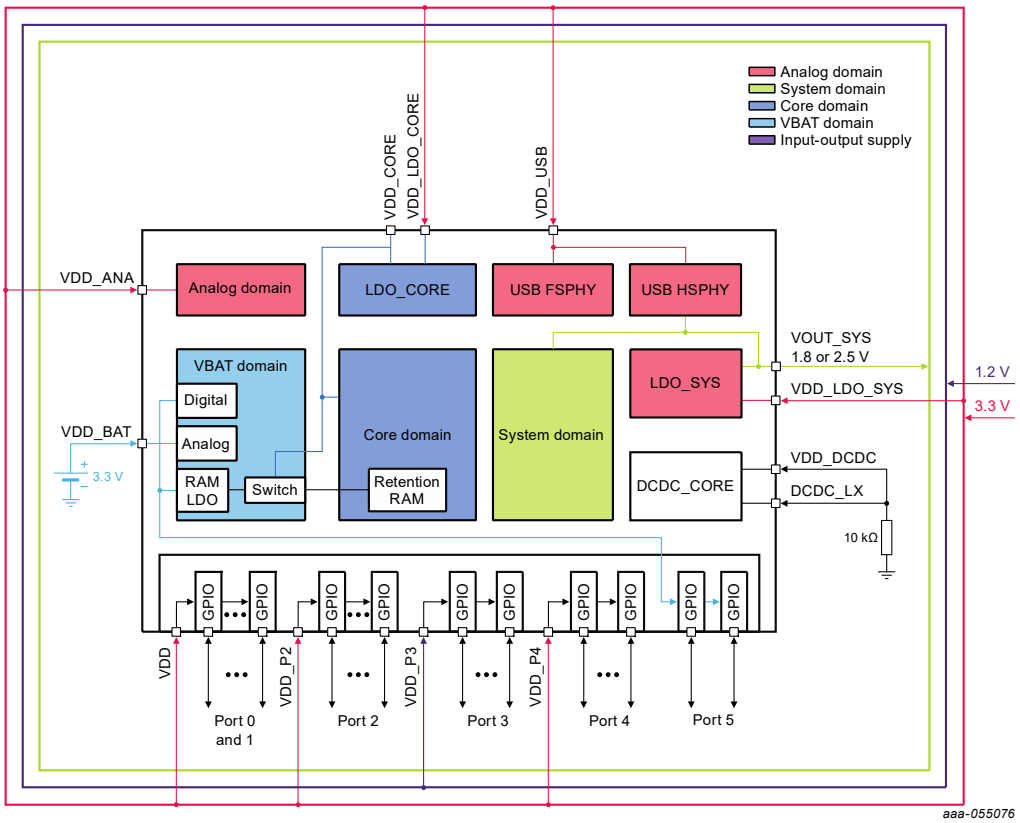

Figure 4. MCX Nx4x low-cost schematic

7.1.2 Power supply on LPC55xx chips

All LPC55xx series support the internal DC-DC converter power supply mode, except LPC553x.

LPC553x supports the internal DC-DC converter power supply mode and internal LDO power supply mode.

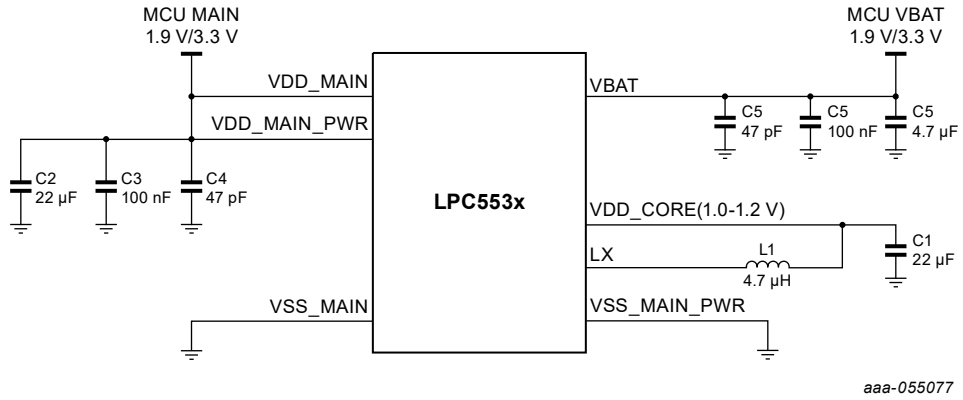

Figure 5. Using internal DC-DC converter (power-efficient)

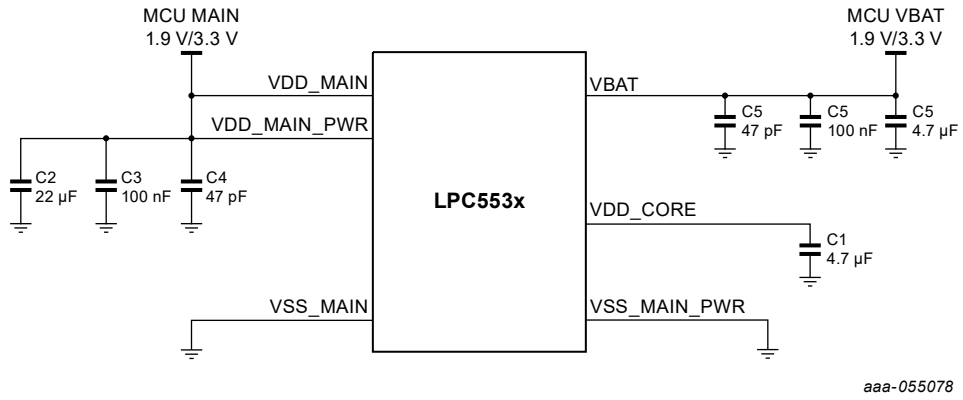

Figure 6. Using internal LDO (low-cost)

7.2 Oscillator design

Table 8. Oscillator design

	MCX Nx4x	LPC55xx
Oscillator design	Supporting the external oscillator range at 16 MHz to 50 MHz	Supporting the external oscillator range at 16 MHz or 32 MHz. **Supporting the software-configurable capacitor bank.**
	Supporting the external 32.768-kHz oscillator (OSC32k) **OSC32k supports the software-configurable capacitor bank.**	Supporting the external 32.768 kHz oscillator. **Supporting the software-configurable capacitor bank.**

Note: *Only a certain frequency (16 MHz) works with USB ISP on LPC5500 series. The USB ISP must configure the clock frequency in CMPA on MCX Nx4x if the non-default (24 MHz) crystal is used.*

7.3 Wakeup timing

Table 9. Comparison of wakeup timing

	Sleep	Deep sleep	Power down	Deep power down
LPC553x	3.2 µS	76 µS	405 µS	2.9 mS

Table 9. Comparison of wakeup timing*...continued*

	Sleep	Deep sleep	Power down	Deep power down
LPC556x	0.5 µS	64 µS	346 µS	4.6 mS
MCX Nx4x	0.22 µS	8.7 µS	9.8 µS	5.3 mS

7.4 Package/Pinout differences

The MCX Nx4x device offered 100HLQFP package and 184VFBGA package.

The LPC553x device offered 48HVQFN package and 100HLQFP package.

The LPC556x device offered 64HTQFP package, 98VFBGA package, and 100HLQFP package.

The drawing for the package can be found in the data sheet.

7.5 Minimum system consideration

There are some additional hardware considerations when migrating from LPC55xx to MCX Nx4x.

The LPC55xx and MCX Nx4x devices have the similar reset, ISP, and debug circuit for the minimum system, but for the power supply circuit, in the DC-DC mode, components are different at values.

8 Conclusion

This document describes the differences between the MCX Nx4x and LPC55xx chips. When migrating from LPC55xx to MCX Nx4x chips, consider the differences described in this document.

9 Reference

- *MCXNx4x Hardware Design Guide* (document UG10092)
- *DCDC Usage on MCXNx4x/Nx3x* (document AN14185)
- *Hardware Design Guidelines for LPC55(S)xx Microcontrollers* (document AN13033)
- *Hardware Design Guidelines for LPC553x/LPC55S3x Microcontrollers* (document AN13707)

10 Revision history

Table 10 summarizes the revisions to this document.

Table 10. Revision history

Document ID	Release date	Description
AN14249 v.1	02 April 2024	Initial public release

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