Sensitivity of High Power RF Transistors to Source and Output Loads

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INTRODUCTION

New generations of cellular radio systems, such as GSM EDGE or UMTS, require more powerful base stations and more powerful transistors to operate with a correct back-off due to linearity constraints.

At the same time, base station manufacturers require warranted performances for the high power RF transistors used in transceivers.

Consequently, transistor manufacturers are required to provide more accurate testing, at increasingly higher power levels.

As power increases, the input and output impedances of the transistors decrease, making the devices more sensitive to the test environment. Therefore, measurement correlation between transistor manufacturer and equipment manufacturer is becoming a real challenge.

An ideal 50 ohm test system does not exist for high power RF transistors, mainly because of the hardware equipment's power handling limitations at frequencies of 1 GHz or higher. The common assumption is that the accuracy of a high power RF test bench relies on the load quality presented to the device under test by its test ports, that is, source load and output load. [1]

This application note discusses the sensitivity of high power transistors to the source load and output load. It describes the test bench used for this study and then explains the experiment process. The influence of source and load quality of the test bench on the main CW performances of an RF device is also covered. The vehicle chosen for this study is a high power, high frequency device from Freescale [2], associated with its manufacturing test circuit, an 85 Watt input/output matched single-ended LDMOS transistor designed for GSM and GSM EDGE applications at 1800 MHz and 1900 MHz.

MEASUREMENT TOOLS AND TEST BENCH

Different kinds of test benches exist for high power and high frequency measurements. For single-tone applications such as GSM, the test bench can be articulated around a Vector Network Analyzer (VNA). For design cycle time optimization, the VNA has some attractive features such as sweep time, gain and Input Return Loss (IRL) versus frequency, power or time. [3]

In the gain versus input power sweep configuration, a 1 dB compression point parameter can be displayed in sweep time. For GSM power amplifiers, the P1dB parameter is the key criteria; the power at which the linearity specification is met is related to this P1dB value.

The engineering test bench shown in Figure 1 measures the magnitude and phase of the incident power (R), reflected power (A), output power (B), IRL (A/R) and gain (B/R) in vector mode.

To measure output power, a power sensor is coupled to a power meter, providing better absolute accuracy than does the (B) measurement of the VNA.

The source port is calibrated with a short circuit, an open circuit and a 50 ohm termination (SOL calibration). The vector type correction ensures an accurate measurement of the IRL of the Device Under Test (DUT), even if the source system load is not ideal.

The calibration for the gain response is a response "thru" calibration, which consists of connecting the source port to the output port by a through connector. This calibration is essentially a normalized measurement that compensates the given source-output load mismatch loss.

For the source port, the standard version test bench used for the current study has a 20 dB IRL value. The output load has a 30 dB IRL value or a Voltage-Standing-Wave Ratio (VSWR) equal to 1.07.

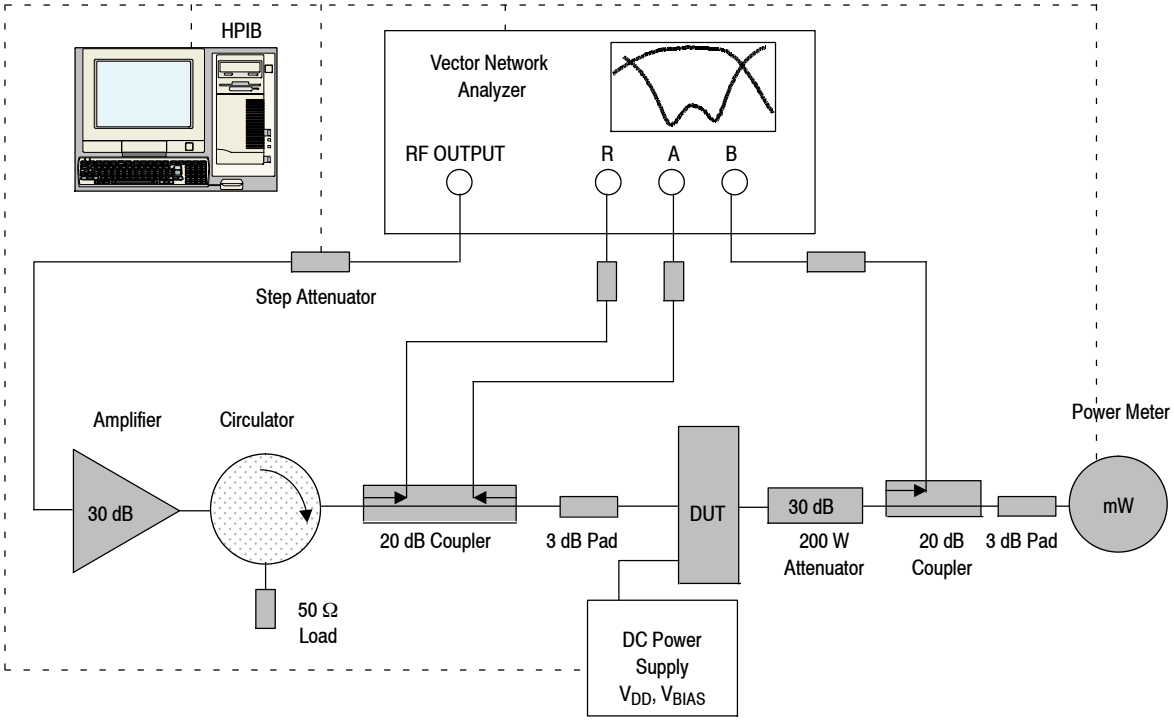

Figure 1. Engineering Test Bench Using a VNA

DESCRIPTION OF THE EXPERIMENT

The purpose of the experiment is to explore the impact of source and output load quality on RF performances of a high power device. This experiment varies both magnitude and phase for the source and only phase for the output.

The quality of a load is commonly characterized by its IRL value or its VSWR to 50 ohms. However, it does not completely describe a load because a load is a complex figure, with an associated magnitude and phase.

This study focuses on four phases, in quadrature, to simplify the experiment. To generate these four phase points on the Smith chart, a 90° phase shifter system is required. A male/female SMA connector at 1880 MHz can be used. Cascading a set of 0, 1, 2 and 3 SMA connectors leads to four different phase shifts (phase 1 to 4). The impact on IRL magnitude when using these connectors is limited, as shown in Figure 2.

To illustrate how the SMA connector operates, the plots on the complex impedance chart and log/mag grid in Figure 2 show a load quality of 10 dB IRL @ 1880 MHz with four phases, corresponding to the introduction of 0, 1, 2 and 3 connectors in the source or the output path.

The Freescale 85 W LDMOS device (MRF18085A) used for this study is an input and output pre-matched transistor designed for GSM1800 applications. It is associated with its production test circuit and has an operating point of V_{DD} = 26 Volts and I_{DQ} = 800 mA.

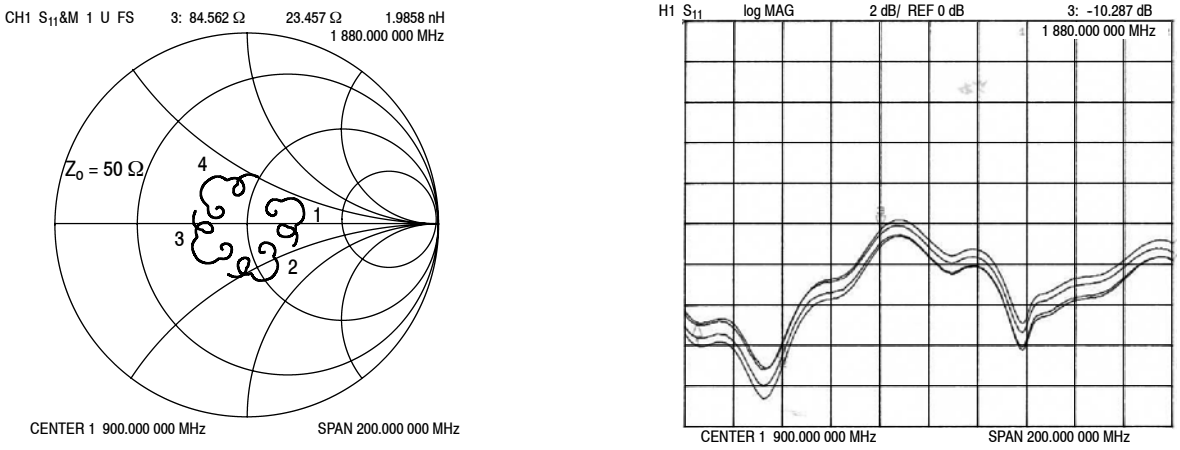

Figure 2. 10 dB IRL @ 1880 MHz Plot on Smith Chart and log/mag Grid with Four Phases

To perform accurate measurements, the transistor and its production test circuit are not removed after each measurement. The use of the engineering bench ensures nonheating effects, because of the fast measurement time.

The values in the following tables are the results of the average of five measurements. However, note that the bench used is very repeatable as the maximum shift among the five measurements is about 1 W in power, 0.1 dB in gain and 0.3% in efficiency.

In this experiment, the effects of the source load and the output load of the test bench are studied separately. However, these effects can be cumulated to determine the overall impact of the test bench load quality on the measured performances.

SOURCE LOAD QUALITY INFLUENCE ON CW PERFORMANCES

To evaluate the influence of the phase and magnitude variations on RF performances for this transistor, the quality of the source port on the design engineering bench is voluntarily lowered. For instance, the 3 dB pad at the source port has been removed (see Figure 1).

Four different source loads are generated at 1880 MHz. Experiments are run at two IRL levels: 10 dB and 15 dB for source load. The test bench is recalibrated before obtaining all of the data.

In this experiment, the IRL value of the example device under Test A (Part 1) in the production test fixture is 12 dB @ 1880 MHz.

All of the results given are at 1880 MHz. The “comp” suffix indicates that the transistor is measured at the P1dB gain compression point (see Tables 1 and 2).

The first observation concerns the impact on P1dB (P_{comp}), due to the nonunilaterality or high value of forward and reverse transconductance of the device. This effect can be minimized by improving the quality of the source load as a difference of 2 W (equal to 0.1 dB) obtained with a 15 dB IRL level compared to 3.5 W (0.16 dB) with a 10 dB source IRL.

No significant impact is observed concerning efficiency, whatever the source IRL level is. However, the impact on gain is really significant, but it can be reduced by using a better source load quality (0.8 dB on gain compared to 0.26 dB for 10 dB and 15 dB source load, respectively, IRL).

Note: The “thru” calibration of the Vector Network Analyzer corrects the mismatch loss between source load (here, 15 dB or 10 dB IRL) and output load (typically, 30 dB IRL). When measuring a device, what is presented to the source load is now the DUT input impedance, as shown in Figure 3.

Consequently, because the measurement mismatch loss and the calibration mismatch loss are different, the measured gain may not be accurately corrected.

Table 3 shows the impact of a 10 dB source IRL on the example device under Test B (Part 2) with a 19 dB IRL value @ 1880 MHz. Compare these results with Table 1 in which a 12 dB IRL device was tested under the same conditions.

Because Part 2 has an input impedance closer to the test bench output impedance than that of Part 1, the impact on measured gain is lower (0.16 dB compared to 0.8 dB). However, the impact on P1dB remains the same (3.5 W).

Table 1. Impact of the Phase Variation of a 10 dB IRL Source Load on CW Performances (Part #1)

	Z_{source} (Ω)	P_{comp} (W)	G_{comp} (dB)	Eff_{comp} (%)
Phase 1	84.5 + j 23.3	91.6	11.8	53.3
Phase 2	60.8 – j 33.0	93.5	12.15	53.6
Phase 3	30.7 – j 13.2	95.1	12.58	53.8
Phase 4	30.4 + j 11.7	92.1	12.32	53.3
Source Load IRL = 10 dB	min	91.6	11.8	53.3
	max	95.1	12.6	53.8
	delta	3.5 W	0.8 dB	0.5 %

Table 2. Impact of the Phase Variation of a 15 dB IRL Source Load on CW Performances (Part #1)

	Z_{source} (Ω)	P_{comp} (W)	G_{comp} (dB)	Eff_{comp} (%)
Phase 1	61.6 + j 17.1	91.0	12.20	53.2
Phase 2	67.8 + j 13.0	91.9	12.21	53.3
Phase 3	42.2 – j 14.4	93.0	12.42	53.4
Phase 4	35.9 + j 2.6	92.9	12.46	53.5
Source Load IRL = 15 dB	min	91.0	12.20	53.2
	max	93.0	12.46	53.5
	delta	2 W	0.26 dB	0.3 %

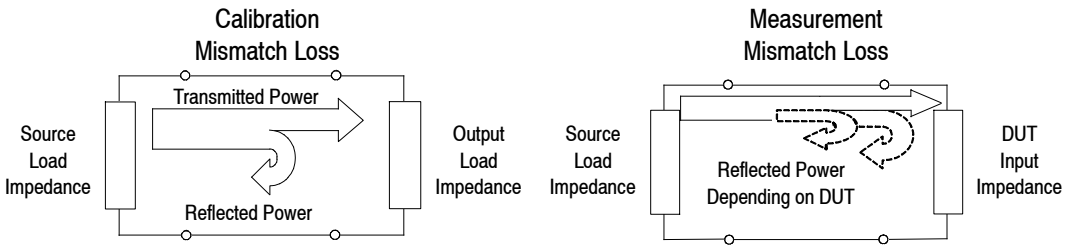

Figure 3. Calibration and Measurement Mismatch Losses

Table 3. Impact of the Phase Variation of a 10 dB IRL Source Load on a 19 dB IRL Device (Part #2)

	Z_{source} (Ω)	P_{comp} (W)	G_{comp} (dB)	Eff_{comp} (%)
Phase 1	84.5 + j 23.3	95.8	13.13	54.2
Phase 2	60.8 - j 33.0	97.0	12.97	54.5
Phase 3	30.7 - j 13.2	99.3	12.99	53.8
Phase 4	30.4 + j 11.7	99.0	13.09	54.7
Source Load IRL = 10 dB	min	95.8	12.97	54.2
	max	99.3	13.13	54.8
	delta	3.5 W	0.16 dB	0.6 %

IMPACT OF THE OUTPUT LOAD ON CW PERFORMANCES

For the source port, the test bench is used in its standard version, resulting in an IRL value of higher than 20 dB in the whole frequency range. The device used is Part 2 (19 dB IRL @ 1880 MHz associated to the production circuit). These two conditions ensure essentially a limited impact on gain and P1dB due to source load.

The output load IRL level is maintained to 30 dB, but four phases have been generated with the same technique as explained in the previous section.

Table 4 shows the output impedances corresponding to the four phases and the associated performances at 1880 MHz. The “comp” suffix indicates that the transistor is measured at the P1dB gain compression point.

A variation of 3.2 W (equal to 0.15 dB) can be observed for P_{comp} and 2.6% for efficiency at P1dB compression. Variation in gain is around 0.3 dB.

The impact of the output phase is significant, because it mainly affects the P1dB compression point and the efficiency performance, even at 30 dB IRL. This may cause miscorrelation between two benches using two different output loads.

This experiment demonstrates that the performances of a given transistor are associated to a given output load. On another output load, for example in the customer’s application, the same performances can be achieved. By fine-tuning the output matching network circuit, it is possible to present to a device the impedances leading to the optimal performances.

Table 4. Influence of the Phase Variation of the Output Load on CW Performances (Part #2)

	Z_{source} (Ω)	P_{comp} (W)	G_{comp} (dB)	Eff_{comp} (%)
Phase 1	49 + j 2.3	92.7	13.22	53.50
Phase 2	53.3 + j 2.0	95.9	13.10	54.0
Phase 3	53.3 - j 2.4	94.6	12.91	51.43
Phase 4	49.3 - j 2.0	94.0	12.91	52.39
Output Load IRL = 30 dB	min	92.7	12.91	51.43
	max	95.9	13.22	54.0
	delta	3.2 W	0.31 dB	2.57 %

CONCLUSION

This application note highlights the difficulty of obtaining accurate measurements for high power RF transistors.

On the source side of the test bench, special attention was given to set up the test bench. A 15 dB IRL is the minimum value required to obtain an accurate measurement because the input source load impacts gain and P1dB. This can be improved by adding an isolator before the input coupler and/or adding a pad (for instance, 3 dB) before or after the input coupler.

When varying the phase of the output load, even at 30 dB IRL, the impact on P1dB and efficiency is significant. At 1 GHz and higher, a load quality better than 30 dB is not realistic because of power load or attenuator (100 W and higher) manufacturing constraints. However, by retuning the circuit on the application load, it is possible to recover the same performances as in the production test fixture.

Therefore, each measured data should be associated with an R + j X format of the source and output loads at the test fixture connector reference plane, for example, when correlation issues have to be solved.

Note that the load quality is not the only cause of miscorrelation. Other causes can be heating effects, device positioning and so on.

For two-tone tests or complex signals such as W-CDMA, the low frequency loads and harmonic loads must be taken into account on both the source and output sides. A more complex study is needed to quantify their corresponding impacts on device performances.

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