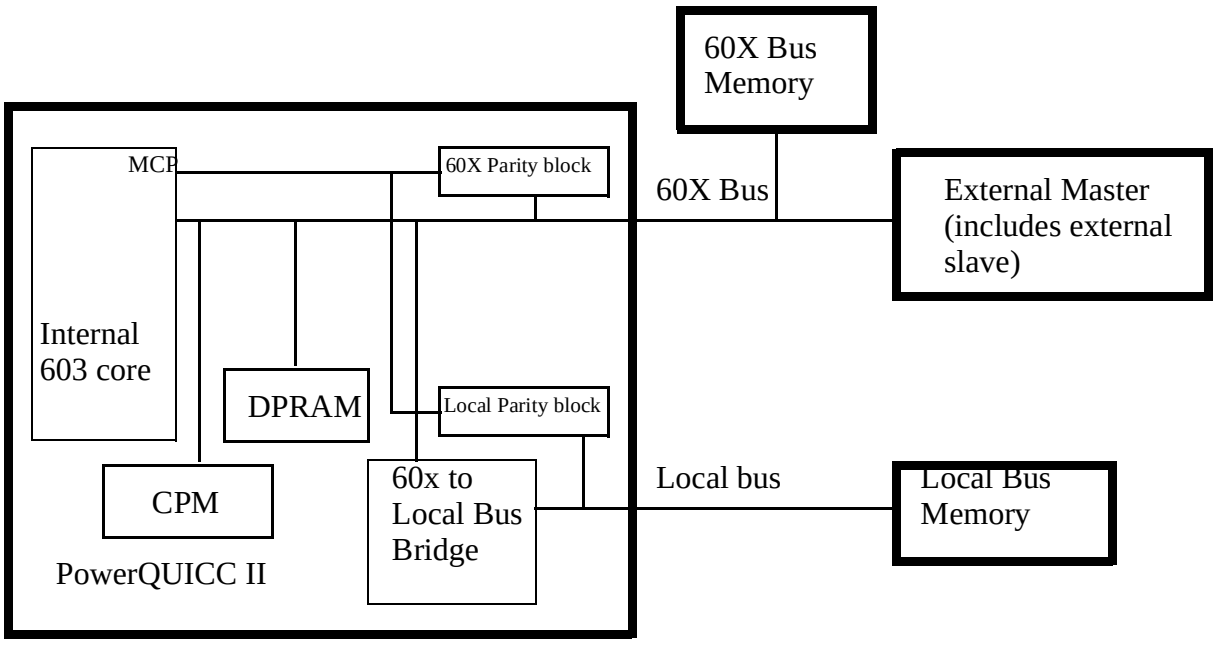
PowerPC™

Application Note

PowerQUICC II Data Error Protection Implementation

This application note describes the data error protection mechanism in systems including PowerQUICC II. Different scenarios involving transactions initiated by PowerQUICC II and external masters are analyzed and some advice on the programming of the data error protection related PQII resources is provided.

The following picture shows a generic system which includes PQII. All the transactions described in this application note are related to this system.



General Considerations

The parity or ECC is generated and checked by two blocks (60X/Local Parity block) which are part of the memory controller. These blocks are logically placed at the edge of the data paths (close to the external pins). Since both transactions initiated by the 60X core and the CPM SDMA engine must be handled by the same mechanism, the data bus parity logic included in the 603 core is not used and must be disabled (by resetting the bit EBD in the HID0 register).

The Parity/ECC logic is controlled by the Chip Select mechanism. For each memory bank the type of data error protection must be selected in the BRx[DECC] field. Furthermore, the Parity/ECC will be generated and checked on the bus associated with the respective memory bank (as an example, if BRx[MS] = 001 and BRx[DECC]=10, RMW parity will be generated and checked on the Local Bus). If a transaction does not hit in any of the defined memory banks, there will be no Parity/ECC generation or checking.

Parity errors or ECC fatal errors are reported to core using the MCP signal.

If the internal 60X core is enabled the result will be a Machine Check Exception or Checkstop State. The 603 core external MCP input must be enabled by setting bits HID0[EMCP]. If a Machine Check Exception is required, also the MSR[ME] bit must be set. For more details regarding the Machine Check Exception, see section 4.5.2 in the MCP603e Risc Microprocessor User Manual.

If the internal 603 core is disabled, the NMI_OUT pin will be asserted as a result of parity errors or ECC fatal errors. The NMI_OUT is automatically configured as an output when the internal core is disabled.

The following sections of this application note describes possible transactions and the data error protection resources involved.

Transactions initiated by the 603 core or CPM and targeted to external memories or peripherals

These transactions are usually assisted by the memory controller. The desired type of data error protection must be selected in the BRx[DECC] register. If an external memory controller is used and data error protection is required, a memory bank must be defined (using a BRx/ORx register pair) and the bit BRx[EMEMC] must be set. If RMW or ECC is selected, the external memory controller must be able to handle read-modify-write cycles.

Transactions initiated by the 603 core or CPM and targeted to external 60X slaves

In order to support data error protection for transactions targeted to external 60X bus slaves a memory bank which covers the external slave address range must be defined using a BRx/ORx register pair. The BRx[EMEMC] bit must be set since the external slave does not need the assistance of the memory controller. Also the BRx[DECC] field must be set to 01 in order to generate and check normal parity. It is possible to select (using the BRx[DECC] field) RMW parity or ECC but in this case the external slave must be able to support read-modify-write cycles.

Transactions initiated by external masters and targeted to external 60X bus memories

If the PQII memory controller is used to assist the external master in these transactions it is possible to program the respective BRx[DECC] field for normal parity. In this case the PQII will drive and check normal

parity on the 60X bus, to and from the memories. RMW parity or ECC can also be selected if the external master is designed to generate read-modify-write transactions for write cycles with the transfer size smaller than the port size (or if the external master will initiate only transactions with the transfer size of full port size (64 bits)). An second PQII is an example of such a master, however there aren't others available to the best of my knowledge.

Transactions initiated by external masters and targeted to external local bus memories

In this case the memory controller is programmed to assist transactions on the local bus. The data error protection mechanism will generate and check parity or ECC (as programmed in the BRx[DECC]) on the local bus and report errors either to the internal 603 core (if enabled) or to an external core using the NMI_OUT signal. No data error protection is available on the 60X bus. If data parity is required on the 60X bus an external chip is recommended for parity generation and checking.

Transactions initiated by external masters and targeted to DPRAM

For these transactions no data error protection is available on the 60X bus. If data parity is required on the 60X bus an external chip is recommended for parity generation and checking.

Summary

In order to use the PQII data error protection mechanism the following bits and fields must be programmed:

- HID0[EBD] in order to disable the 603 core data parity checking
- HID0[EMCP] = 1 in order to enable the MCP input of the 603 core (if the 603 core is enabled)
- MSR[ME]=1 to enable machine check exceptions (if required)
- ORx/BRx for each of the banks (address windows) where data error checking must be enabled
- BRx[DECC] to select the type of data error protection
- BRx[EMEMC] =1 if the respective bank is associated with an external slave which does not need the assistance of the memory controller

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