MPC8260ADS
REVISION CHANGES FROM ENG BOARD TO PILOT REVISION BOARD
10/19/1999

I. Purpose –

There are differences between the ENG and PILOT revisions of the MPC8260ADS board which may impact Third Party Developers' BSP's and/or preliminary application development. This document lists the features of the new PILOT board, then details the changes between the ENG and PILOT revisions. For complete information on the MPC8260ADS, refer to the MPC8260ADS User's Manual, Rev 0.213, dated November, 1999 at:
http://www.mot.com/netcomm).

The ENG board is the 1st revision of the board, the final of these will have been shipped in November, 1999. The PILOT board is the 2nd revision of the board, due to begin shipping in November 1999. Both boards have a sticker which clearly indicates if they are ENG or PILOT. The ENG revision's sticker is located between DS1 and LD16. The PILOT revision's sticker is located just above the ATM phy, U1.

II. Features of the new PILOT board:

*64-bit MPC8260, running @ 66MHz external bus frequency.

*16 MByte, Unbuffered, 168 pin Synchronous Dram DIMM, residing on 60X bus, controlled by SDRAM machine 1. Support for 64 MBytes DIMM (single-bank 1only). Optional address Latch - Multiplexer is required if an L2-cache module is assembled.

*Support for PBI (Page Based Interleaving) in both Single and 60X-Bus 2 modes.

*Support for Automatic DIMM Identification via MPC8260's I2C port and DIMM's serial EEPROM.

*Optional 1/2 MByte L2-Cache on-board using 2 MPC2605 Lookaside cache modules.

*8 MByte, 80 pin Flash SIMM, buffered from 60X bus. Support for up to 32 MByte, controlled by GPCM, with Automatic Flash SIMM identification, via BCSR. Support for both ON- and OFF-SIMM Flash reset.

*5V/12V VPP for Flash SIMM, Jumper Selectable.

*4 MByte unbuffered SDRAM on Local bus, controlled by SDRAM machine 2, soldered directly on board.

*Board Control & Status Register - BCSR, controlling board's operation.

*Fast Download support via JTAG.

*Power-On Reset Option via JTAG.

*Programmable Power-On-Reset and Hard Reset Configurations via FLASH memory, optionally provided by BCSR (dip-switch selectable), providing a rescue mode in case of inadvertent Flash erasure.

*Module Enable Indications for all on-board communication modules.

*High density (MICTOR) Logic Analyzer connectors, carrying all MPC8260 signals, for fast logic analyzer connection.

*155 Mbps ATM UNI on FCC1 with Optical I/f, connected to the MPC8260 via UTOPIA I/F, using the PMC-SIERA 5350.

*10/100-Base-T Port on FCC2 with T.P. I/F, MII controlled, using Level-One LXT970.

*Dual RS232 port residing on SCC1 & SCC2.

*Module disable (i.e., low-power mode) option for all communication transceivers - BCSR controlled, enabling use of communication ports, off-board via expansion connectors.

*Dedicated MPC8260's communication ports expansion connectors for convenient tools' connection, carrying also necessary bus signals, for transceivers' M/P I/F connection. Implemented with 2 X 128 pin DIN 41612 receptacle connectors.

*External Tools Identification & status read Capability, via BCSR.

*Power-On Reset Push - Button

*Soft/Hard Reset Push - Button

*ABORT Push - Button

*Single 5V Supply.

*Reverse/Over Voltage Protection for Power Inputs.

*Multi-Range MPC8260 Internal Logic supply. Ranges include - 1.7V to 1.9V, 1.8Vto 2.0V and 2.3V - 2.7V, currently changeable within a range.

*Software Option Switch provides 8 S/W options via BCSR.

III. Functional changes from the ENG revision to the PILOT revision:

A. BCSR

*The BCSR address space was doubled. It now contains eight 32 bit registers (part of which are yet reserved) allowing space for future expansion.

*BCSR0 and BCSR1 were moved to D(0:7) instead of D(24:31). Notice that this change will affect current usage of the BCSRs, even for simply turning on LED's.

*Added optional Power-On and Hard Reset configurations, dip-switch enabled, with full MODCK control via dip-switches.

*On BCSR0 added 2 control bits PBI (Page Based Interleaving) and DIMM_SIZE to provide PBI support when
working with L2-Cache. These bits have no use in Single-MPC8260 mode.

*Added support for Fast Download via JTAG (BCSR6 & BCSR7), with internal and external bypass options for ENG compatibility. The ADS wakes up in ENG compatibility mode.

*Added support for Power-On Reset via JTAG (BCSR6 & BCSR7).

*The codes for L2Cache size were changed: 'X0' is now reserved, '11' is no L2Cache, '01' is 512K L2Cache.

B. SDRAM DIMM (PPC-Bus)

*Added PBI (Page Based Interleaving) support. In order to support PBI, the addressing scheme was changed so that
BKSEL(0:2) are connected to (NC, BA1, BA0) correspondingly, rather than -
(BA1, BA0, A11) correspondingly. In addition for 60X mode PBI support, the Latch-Mux was enlarged and qualified by PBI and DIMM_SIZE bits in BCSR0.

C. FLASH SIMM

*Low order address lines are connected to BADDR(27:29) lines. This allows operation in 60X mode. However, due to rev 0.X errata, **Power On Reset configuration with rev 0.2 MPC8260s, must be taken from the PAL.**

*Added Power-On Reset connection to FLASH SIMMs Reset input, to allow use of SIMMs which require external reset.

D. Power

*VDDL may now be regulated within 3 voltage ranges, jumper selectable:
2.3V to 2.7 (original MPC8260 spec)
1.7V to 1.9V (HIP4 spec)
1.8V to 2.0V (2V capable HIP4 devices)

*3.3V bus which drives also VDDH bus, may be optionally (production option) regulated between 3.0 to 3.3V.

*Better Heat-Sinking for both Power Regulators.

E. Communication Ports

*Unified ATM transceiver's receive and transmit FIFO clocks (ATMRFCLK & ATMT-FCLK) into ATMFCLK.

*ATM Rx and Tx indication LEDs are now operational only when ATM is enabled via BCSR.

*ATMRCLK signal (previously unused) is connected to P4 for SRTS support. When an ENG revision T/ECOM board is connected to the ADS, this signal is tri-stated.

*RS232 ports' (1,2) CTS~ lines are now controllable by S/W, via PI/O lines.

F. Miscellaneous Changes

*ALE signal design is changed to allow proper operation in both Single/60X bus modes (production configured)

*Added more ground lines to P5 - JTAG connector, to provide better noise immunity.

*THERM(0:1) signals are detached from GND plane and available at a dedicated header - J3.

*Reduced most of the MPC8260's damping resistors to 22 W.

*HP Logic Analyzer POD's Shrouds may now be soldered in place.