AN2162
Rev. 2, 11/2005

Comparing the MSC8101 and MPC8260

By Donald Simon

Although the Freescale MSC8101 and MPC8260 support different types of applications, there is an overlap in functionality since both devices share a similar communications processor module (CPM) and system interface unit (SIU). Also, both devices use a 60x-compatible external system bus. The MSC8101 SC140 core performs high-speed arithmetic calculations, primarily to analyze and modify digitized versions of analog signals. The SC140 core is based on the StarCore DSP technology. The MPC8260 is a high-performance general-purpose microprocessor with a powerful 32-bit MPC603e RISC core. Understanding the similarities and differences between these devices gives a designer a broader base to determine a system solution. Refer to the MSC8101, MSC8103, and MPC8260 documentation for more information. The MSC8101 is identical to the MSC8103, except that the MSC8101 includes an enhanced filter coprocessor (EFCOP). This application note focuses on MSC8101/MSC8103 mask set 2K87M and MPC8260 HiP4 devices.

CONTENTS

1 Internal Modules

The MSC8101 and MPC8260 comprise three internal modules: CPM, SIU, and SC140 extended core for the MSC8101 or the MPC603e RISC core for the MPC8260

The CPMs in the MSC8101 and MPC8260 are similar, but each uses a different revision of the CPM die. To minimize the size of the MSC8101 package footprint, the MSC8101 allocates fewer I/O pins for the CPM functionality. Refer to AN1851, *Functional Pin Differences Between the MSC8101 and MPC8260 CPMs*.

The MSC8101 and MPC8260 SIUs both employ a flexible memory controller that interfaces to almost any memory system.

The biggest difference between the MSC8101 and MPC8260 lies in the cores. The MSC8101 core is a high-performance, low-power DSP. The MPC8260 core is a high-performance, low-power RISC microprocessor derived from the 603e microprocessor with 16 KB of instruction cache, 16 KB of data cache, and a floating-point unit. As a result, each device supports different types of applications. The following definitions of *DSP* and *RISC* derive from *Newton's Telecom Dictionary* by Harry Newton.

> DSPs are specialized digital microprocessors that perform calculations on digitized signals that were originally analog (and then send the results on)… One advantage DSPs have is their powerful mathematical computational abilities. DSPs are used extensively in telecommunications for tasks such as echo cancellation, call progress monitoring, voice processing and for the compression of voice and video signals.

Computers based on RISC use an unusual high speed processing technology that uses a far simpler set of operating commands. … RISC is a design that achieves high performance by doing the most common computer operations very quickly.

2 Target Applications

The MSC8101 and MPC8260 are tailored for different sets of applications. **Table 1** shows typical applications for each device. Both devices provide a system-on-a-chip for many communication applications. The MSC8101 targets wireless infrastructure systems and wireline multichannel applications that require networking support. In addition, the MSC8101 supports an 8-bit UTOPIA interface. Applications include second and third generation systems, packet telephony, and modem banks.

The MPC8260 targets high-speed microprocessor networking applications and those requiring a memory management unit (MMU) and cache. In addition, the MPC8260 supports a 16-bit UTOPIA interface. Applications include remote access concentrators, regional office routers, and telecom switching equipment

Acronyms and Abbreviations

AAL2	ATM adaptation layer 2
ALU	arithmetic logic unit
ATM	asynchronous transfer mode
BRG	baud-rate generator
CLK	clock
CP	communications processor
CPM	communications processor module
DACK	DMA data acknowledge
DLL	delay lock loop
DMA	direct memory access
DRACK	data request acknowledgement
DSP	digital signal processor
EFCOP	enhanced filter coprocessor
FC-PBGA	flip chip-plastic ball grid array
FCC	fast communications controller
HDI16	host data interface, 16-bit
HiP	high performance
HPE	host port enable
HRCW	host reset configuration word
IC	interrupt controller
IDMA	independent DMA
IMP	integrated multiprotocol processor
I/O	input/output
ISB	internal space base
IU	integer unit
MAC	multiply accumulate unit
MCC	multi-channel controller
MIP	million instructions per second
MMU	memory management unit
PIC	programmable interrupt controller
PIO	parallel input / output
PLL	phase lock loop
QUICC	quad integrated communications controller
RISC	reduced instruction set computing
ROM	read only memory

Table 1. Typical Applications

MSC8101	MPC8260
Wireless infrastructure 2G, 2.5G, 3G systems Packet telephony Voice, fax, modem, video Modem banks (xDSL) WAN switching and transmission Compression/echo cancellation	Wireless infrastructure Remote access concentrators Regional office routers Cellular infrastructure equipment Telecom switching equipment Ethernet switches T1/E1 to T3/E3 bridges WAN switching and transmission LAN to WAN bridges/routers

Many applications run on either the MSC8101 or the MPC8260. The following list of considerations may be helpful in deciding whether to use an MSC8101 or MPC8260 for a specific application.

- Cost
- Part availability
- Power usage
- Operating speed
- Package size
- Third-party support
- Legacy code reuse
- Engineering support
- Previous device experience
- Device errata
- Device functionality (cache, DMA, I/O, and so forth)

3 General Characteristics

Table 2 shows the general characteristics of the MSC8101 and the MPC8260 devices. This section discusses each row.

Table 2. MSC8101 and MPC8260 General Characteristics[1]

Characteristic	MSC8101	MPC8260[2]
Core Developed By	StarCore LLC	StarCore LLC
Naming Prefix	MSC	MPC
Number Pins	332	480
Package	FC-PBGA (17 x 17 mm, 0.8 mm pitch)	TBGA (37.5 x 37.5 mm, 1.27 mm pitch)
Technology	0.18 µm (HiP6)	0.29 µm (HiP3, moving to 0.25 µm HiP4)
Power Supplies	2 (core/SIU/CPM: 1.6 V, I/O: 3.3 V)	2 (core/SIU/CPM: 2.0 V, I/O: 3.3 V)
External Clocks	1	1

Table 2. MSC8101 and MPC8260 General Characteristics[1] (Continued)

Characteristic	MSC8101	MPC8260[2]
Maximum Core Clock	300 MHz	300 MHz
Maximum CPM Clock	200 MHz	208 MHz
Maximum System Bus Clock	100 MHz	83 MHz

Notes: **1.** Refer to the respective data sheet and online updates for the latest information on each device.

2. Also known as PowerQUICC™ II.

The MSC8101 supports networking (CPM internal module) and memory management (SIU internal module). At the heart of the MSC8101 device is the SC140 core. The PowerQUICC II is based on a long line of microprocessors, beginning with the MC68302 integrated multi-protocol processor (IMP). From the MC68302 came the MC68360 QUICC (Quad Integrated Communications Controller)), then the MPC860 (PowerQUICC), and finally the MPC8260 (PowerQUICC II). Performance and enhancements improved with each new part.

As **Table 2** shows, the MSC8101 contains 332 external signal connections versus 480 connections for the MPC8260. Therefore, the MSC8101 includes only 69 percent of the number of MPC8260 connections. Notice that the MSC8101 uses a much smaller package than the MPC8260.The MSC8101 requires only 21 percent of the surface real estate used by the MPC8260. Notice also that the packages of the two devices differ.

The manufacturing technology employed on the MSC8101 device (HiP6) is more advanced than that for the MPC8260 device (HiP4).[1] The MSC8101 and MPC8260 require two power supplies. Both devices require a 3.3 V power supply for the I/O, but the MSC8101 uses a lower core voltage of 1.6 V versus 1.8, 1.9, and 2 V for the MPC8260.

The MPC8260 supports a higher CPM clock than the MSC8101, even though the MSC8101 is produced using a more advanced technology process. This is due to the design trade-offs in the MSC8101.

The MSC8101 has one external 60x-compatible memory bus and a host data interface port. The MPC8260 has two external memory buses (60x-compatible system and local bus) and no host data interface port. The MSC8101 does have a local bus, but it is only available internally. If the MSC8101 uses the host interface (HDI16), the number of available data lines is cut by half to 32 bits.

4 Internal Blocks

As shown in **Table 3**, both devices contains three major blocks:

- Core
- SIU
- CPM

1. The MPC8260 device is migrating to the HiP4 process.

Table 3. MSC8101 and MPC8260 Internal Blocks

Block	MSC8101	MPC8260
Core (processor)	StarCore 140 • 16-bit DSP Extended Core • 512 KB SRAM —no instruction cache —no data cache • EFCOP • HDI16 • PIC	MPC603e • 32-bit RISC • 32 KB RAM —16 KB instruction cache —16 KB data cache • MMU
SIU	Similar to MPC8260. Adds: • DMA • Expanded SIC • Added external SIC	Enhanced MPC860 SIU • No DMA
CPM	Die similar to that of the MPC8260 but not all the pins are available externally and the functionality of some pin is mapped to other pins.	Enhanced MPC860 CPM

The following paragraphs discuss these three major block differences.

4.1 Core Differences

The MSC8101 SC140 core is part of an extended core that includes a 16-bit DSP, 512 KB RAM, an enhanced filter coprocessor (EFCOP), a 16-bit host data interface (HDI16), and a programmable interrupt controller (PIC). Unlike the MPC8260, the MSC8101 contains no instruction and data cache, and no memory management unit (MMU).

The MPC8260 includes a 32-bit reduced instruction set controller (RISC) processor, 32 KB of cache RAM (composed of a 16 KB instruction cache and a 16 KB data cache), and an MMU. The MPC8260 does not include a coprocessor.

The MSC8101 core contains sixteens times the RAM in the MPC8260 (512 KB versus 32 KB). The increased memory in the MSC8101 allows DSP applications to run out of internal RAM to reduce execution time. The MPC8260 internal memory is used as an internal cache. The MPC8260 uses an internal cache and memory management units (MMUs) to optimize execution time.

4.2 Major SIU Differences

The MSC8101 SIU is based upon the MPC8260 SIU. The MSC8101 adds a direct memory access (DMA) controller and a second interrupt controller (SIC_EXT: external SIU-CPM interrupt controller).

4.3 CPM Differences

The MSC8101 contains a CPM die similar to that of the MPC8260, but it uses a different external signal connection configuration in which some pins are not used and some pins are redefined.

Note: The MSC8101 and MPC8260 use different CPM die revision levels.

4.4 Functional Comparisons

Figure 1 and **Figure 2** show the functional diagrams for the MSC8101 and MPC8260, respectively. Note that in the MSC8101, a DMA block resides between the system bus and local bus. The DMA block can act as a bridge between the two buses. There are sixteen DMA channels. Examples of DMA usage are:

- local bus to/from system bus
- external memory to external memory
- internal peripheral to/from external memory

Notice that the local bus is not available externally.

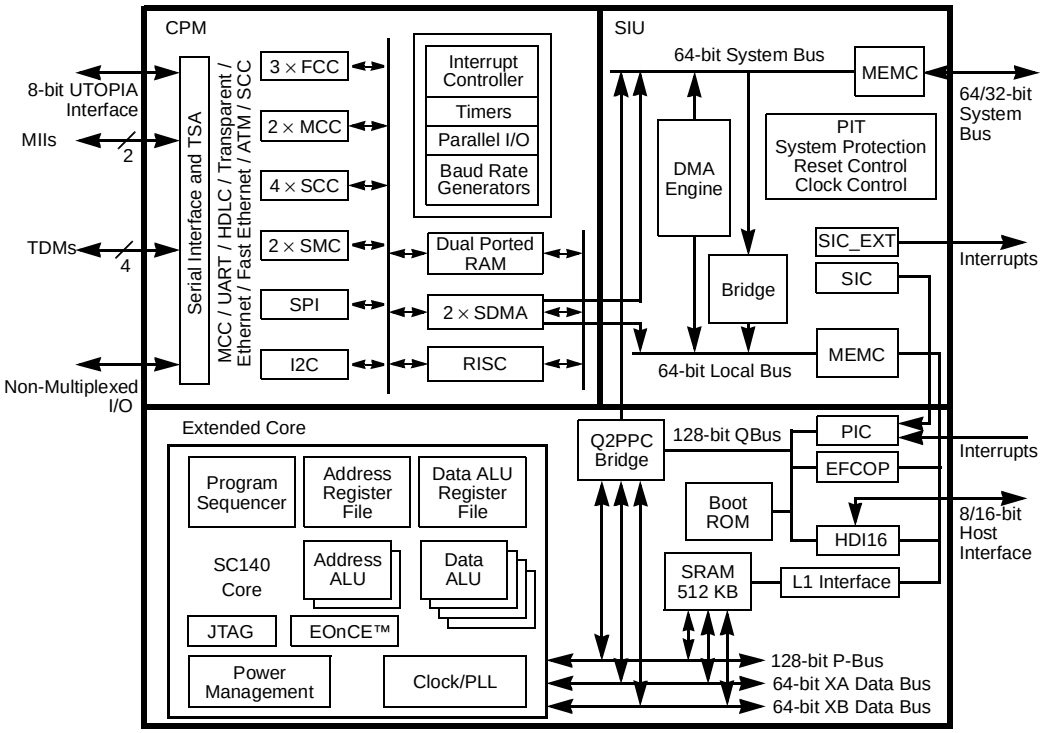


Figure 1. MSC8101 Block Diagram

Figure 2 shows that the MPC8260 supports an instruction and data MMU as well as an instruction and data cache. Unlike the MSC8101 local bus, the MPC8260 local bus is externally accessible.

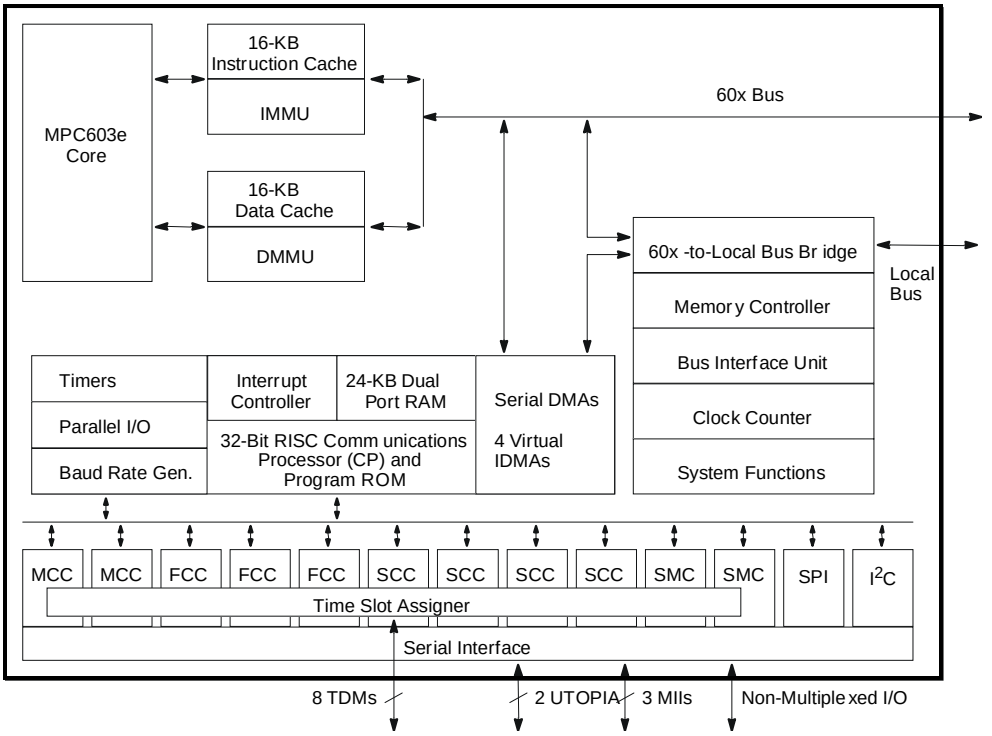


Figure 2. MPC8260 Functional Diagram

5 Performance

Performance depends on many factors, including clock speed, application-specific requirements, memory, code and device-specific resources (for example, MPC8260 cache or MSC8101 SIU DMA). The MSC8101 cannot easily be compared with the MPC8260, because the MSC8101 core is a DSP, and the MPC8260 core is a RISC processor. At a 300 MHz core clock speed, the SC140 can execute 1200 million multiply-accumulate instructions per second (1200 MMACS). Each MMACS value is the equivalent of several RISC MIPS, the performance measure used by some other DSPs. For comparison, the SC140 can be said to perform 3000 RISC MIPS—ten RISC operations per cycle at 300 MHz.

In terms of the SPEC 95 benchmark for integer operations, the MPC603e core performance ranges between 6.6 and 7.65 at 300 MHz. The MSC8101 and MPC8260 CPM performance is similar, but not all the MPC8260 CPM pins are available externally on the MSC8101. Serial bit rates up to 710 Mbps @ 133 MHz can be achieved.

6 Data Sizes

This section shows some of the supported core and C data types used by the MSC8101 and MPC8260 cores and discusses some core data type terminology. **Table 4** shows the data types for the MSC8101 SC140 core, the MPC8260 603e core, and the CPM. The CPM in both devices contains a 32-bit RISC processor.

Table 4. Core Data Types

Name	MSC8101 SC140 Core	MPC8260 603e Core	CPM/60x-Compatible Bus
Byte	8 bits	8 bits	8 bits

Table 4. Core Data Types

Name	MSC8101 SC140 Core	MPC8260 603e Core	CPM/60x-Compatible Bus
Half Word	NA	16 bits	16 bits
Word	16 bits	32 bits	32 bits
Long Word	32 bits	64 bits	64 bits
2 Long Word	64 bits	NA	NA

The MSC8101 SC140 core is a 16-bit DSP processor, because each of the four arithmetic logic units (ALU) contains a 16-bit MAC and the SC140 instruction size is 16 bits. However, the ALUs also support a 40-bit parallel barrel shifter and three 40-bit data buses. The SC140 core also supports 32- and 64-bit core data types.

The MPC8260 603e core is a 32-bit processor, because it contains a 32-bit integer unit (IU). The 603e core also supports a 64-bit data bus.

Note: The MSC8101 does not support a floating-point arithmetic unit. The latest version of the MPC8260 (HiP4) adds floating-point support.

Table 5 shows some of the C data types for the SC140 core and the 603e core.

Table 5. C Data Types

C Data Type	MSC8101 SC140 Core	MPC8260 603e Core
(unsigned) char	8 bits	8 bits
(unsigned) short integer	16 bits	16 bits
(unsigned) long integer	32 bits	32 bits
double[1]	32 bits	32 bits
Word40[2]	40 bits	not applicable
Word64[2]	64 bits	not applicable
long long integer[3]	64 bits	64 bits
double[4]	64 bits	64 bits

Notes:
1. Metrowerks® CodeWarrior® recognizes this type as a floating-point data type.
2. Word40 and Word64 are data types custom-designed by Metrowerks CodeWarrior and accessed through intrinsic functions.
3. The long long integer is a custom data type recognized by the Green Hills compiler.
4. The Green Hills compiler recognizes this as a 64-bit double-precision floating-point data type.

7 Legacy Names

Figure 2 shows the 60x-compatible system bus connected to the MPC603e core of the MPC8260. The 60x-compatible system bus is so called because it connects to the MPC603e core.

8 System Bus

Figure 3 shows the system bus for the MSC8101 and MPC8260. The MSC8101 design is based on the MPC8260 system bus. However, because it does not support cache or IDMA functionality, the MSC8101 does not include the following twenty-one signals in its system bus:

- AP[0–3] and APE (address parity)
- $\overline{\text{CI}}$ and $\overline{\text{WT}}$ (cache)
- $\overline{\text{TLBISYNC}}$ and $\overline{\text{RSRV}}$ (processor state)
- DREQ[1–4], $\overline{\text{DACK[1–4]}}$, and $\overline{\text{DONE[1–4]}}$ (IDMA-SDMA)

The MSC8101 adds the following ten signals to support the SIU DMA:

- $\overline{\text{DACK[1–4]}}$, $\overline{\text{DREQ[1–4]}}$, and $\overline{\text{DRACK[1–2]}}$/$\overline{\text{DONE[1–2]}}$

Note: The MSC8101 SIU DMA yields a higher performance than the MSC8101 and MPC8260 CPM SDMAs.

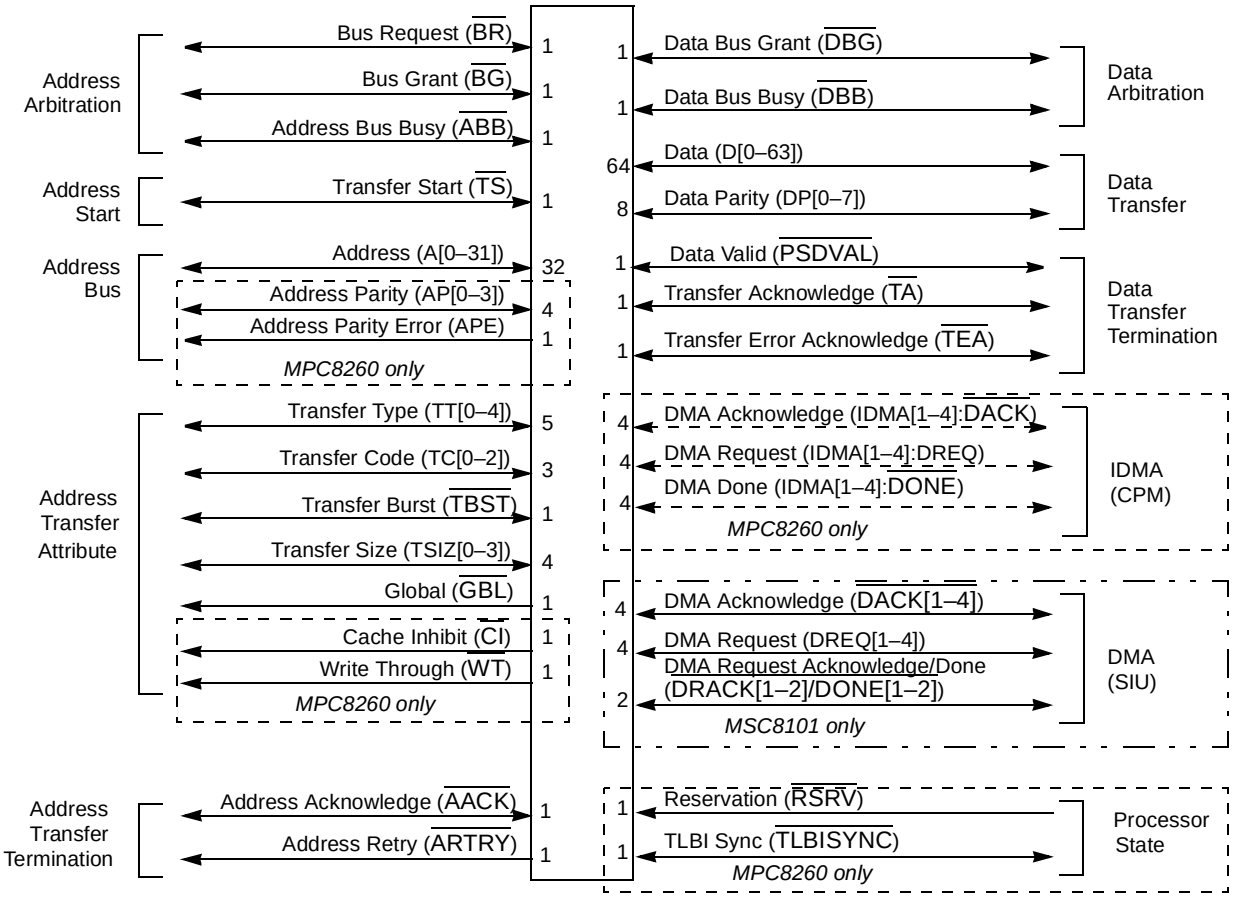


Figure 3. System Bus

9 DMA

The MSC8101 and MPC8260 contain two hardware serial direct memory access (SDMA) channels in the CPM. The MSC8101 also adds a DMA channel to the SIU. **Figure 4** shows where the DMA channels are located in the MSC8101 and MPC8260.

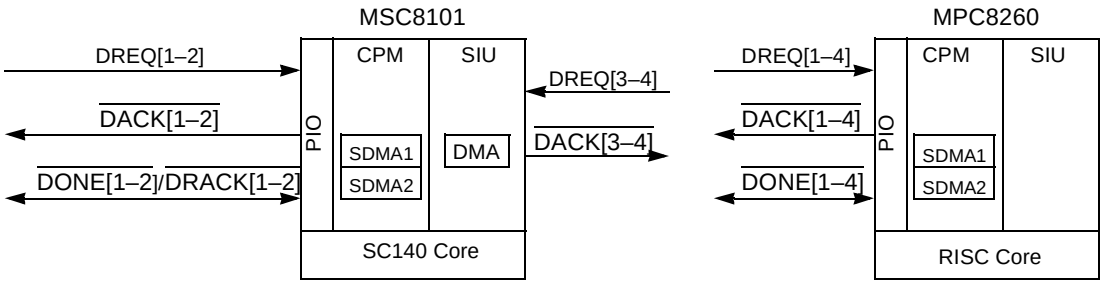


Figure 4. MSC8101/MPC8260 DMA Locations and Signals

The MPC8260 has 12 IDMA pins (four groups) that connect to the internal CPM SDMA. The MSC8101 has 10 DMA pins (four groups, two with $\overline{\text{DONE}}/\overline{\text{DRACK}}$ support), but these pins connect internally to the SIU DMA. Although the MSC8101 and MPC8260 use the same CPM die, some of the pin connections to the CPM are changed. In the MSC8101 for example, the DMA pins do not connect to the CPM in the same way as the MPC8260. In summary, the MPC8260 external IDMA pins support four CPM SDMA interfaces, while on the MSC8101, external pins connect through the CPM interface for two DMA channels and other pins connect through the system bus to the other two DMA interfaces, although they all connect internally to the SIU DMA.

With reference to **Figure 4**, the four MPC8260 $\overline{\text{DONE}}$ pins are replaced with two $\overline{\text{DONE}}/\overline{\text{DRACK}}$ pins on the MSC8101. The $\overline{\text{DRACK}}$ signals are output-only pins. The $\overline{\text{DONE}}$ pins on the MPC8260 are bidirectional open-drain signals that indicate the last IDMA transfer. When a peripheral requires IDMA service, the MPC8260 asserts DREQ and the MPC8260 begins the IDMA process. When the IDMA service is in progress, $\overline{\text{DACK}}$ is asserted during accesses to the peripheral. IDMA and virtual DMA utilize the two hardware SDMA channels in the CPM. Virtual DMA transfers data from a peripheral controller (FCC, MCC, SCC, SMC, SPI, I^2C) to/from internal memory. **Table 6** lists the SIU DMA signals multiplexed through the MSC8101 CPM I/O interface.

Table 6. MSC8101 SIU DMA Signals Multiplexed through the CPM I/O Interface

SIU DMA Signal	Port—PIO Signal
$\overline{\text{DACK2}}$	Port C—PC25
DREQ2	Port C—PC24
$\overline{\text{DACK1}}$	Port C—PC23
DREQ1	Port C—PC22
$\overline{\text{DRACK1}}/\overline{\text{DONE1}}$	Port D—PD31
$\overline{\text{DRACK2}}/\overline{\text{DONE2}}$	Port D—PD30

Table 7 lists the SIU DMA signals multiplexed through the MSC8101 system bus.

Table 7. MSC8101 SIU DMA Signals Multiplexed through the System Bus Interface

SIU DMA Signal	Multiplexed System Bus Signals
$\overline{\text{DACK3}}$	$\overline{\text{IRQ6}}$/DP6/$\overline{\text{DACK3}}$
DREQ3	$\overline{\text{IRQ4}}$/DP4/DREQ3/$\overline{\text{EXT\_BG3}}$

Table 7. MSC8101 SIU DMA Signals Multiplexed through the System Bus Interface

SIU DMA Signal	Multiplexed System Bus Signals
DACK4	IRQ7/DP7/DACK4
DREQ4	IRQ5/DP5/DREQ4/EXT_DBG3
Notes: Although the MSC8101 DMA supports four external peripherals, there are no external pins for DONE[3–4] and DRACK[3–4]. Refer to the *MSC8101 Reference Manual*.	

Table 8 lists the MPC8260 IDMA signals multiplexed through the CPM I/O interface.

Table 8. MPC8260 IDMA Signals Multiplexed through the CPM I/O Interface

SIU DMA Signal	Port—PIO Signal
IDMA4:DREQ	Port A—PA5
IDMA4:DONE	Port A—PA4
IDMA4:DACK	Port A—PA3
IDMA3:DACK	Port A—PA2
IDMA3:DONE	Port A—PA1
IDMA3:DREQ	Port A—PA0
IDMA1:DACK	Port C—PC23
IDMA1:DONE	Port C—PC22
IDMA2:DACK	Port C—PC3
IDMA2:DONE	Port C—PC2
IDMA2:DREQ	Port C—PC1
IDMA1:DREQ	Port C—PC0

10 Reset Sources

This section and the next cover reset sources and power-on reset, respectively. The following sources provide additional information on reset:

- *MSC8101 Reference Manual*, **Chapter 5** *Reset* and **Chapter 7** *Clocks*
- *MSC8101 User's Guide*, **Chapter 2** *Reset Configuration and Boot*
- MSC8101 Technical Data (MSC8101)
- MSC8101 Software Initialization Overview Application Note (AN1852)
- *MPC8260 PowerQUICC II™ User's Manual*, **Chapter 5** *Reset* and **Chapter 9** *Clocks and Power Control*

There are three reset pins on the MSC8101 and MPC8260: PORESET, HRESET and SRESET. They are in hierarchical order. PORESET resets (controls) HRESET and SRESET; HRESET resets (controls) SRESET. **Table 9** shows the reset sources for the MSC8101 and MPC8260. PORESET is the only reset source that initializes everything in the device including the clocks. The MSC8101 and MPC8260 must go through a power-on reset to change the system clock frequencies.

A hard reset ($\overline{\text{HRESET}}$) initializes everything in the MSC8101 except the reset logic and PLL states. Although the hard reset initializes most registers, it does not the clear the internal SRAM in the MSC8101 (the MPC8260 contains only cache SRAM). In addition to asserting $\overline{\text{HRESET}}$ as an input, there are two internal conditions that can generate an $\overline{\text{HRESET}}$ signal in the MSC8101:

- software watchdog time-out
- bus monitor time-out

In the MPC8260, there are three internal conditions that can generate an $\overline{\text{HRESET}}$ signal:

- software watchdog time-out
- bus monitor time-out
- checkstop (multiple exception conditions occur simultaneously, such as a double bus fault)

A soft reset ($\overline{\text{SRESET}}$) initializes internal logic and the core. Assertion of a JTAG reset ($\overline{\text{TRST}}$) generates an $\overline{\text{SRESET}}$ signal in both devices.

Table 9. Reset Sources

Reset Source(s)	Reset Logic and PLL States Reset	System Configuration Sampled	Clock Module Reset	$\overline{\text{HRESET}}$ Driven	Other Internal Logic Reset	$\overline{\text{SRESET}}$ Driven	Core Reset
Power-on reset External only, $\overline{\text{PORESET}}$ asserted	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Hard Reset External, $\overline{\text{HRESET}}$ asserted Internal: • Software Watchdog Reset • Bus Monitor Reset • Checkstop Reset (MPC8260 only)	No	Yes	Yes	Yes	Yes	Yes	Yes
Soft Reset External, $\overline{\text{SRESET}}$ asserted Internal, JTAG Reset	No	No	No	No	Yes	Yes	Yes

11 Power-On Reset Configurations

Table 10 shows the power-on reset configurations for the MSC8101 and MPC8260.

Table 10. Power-On Reset Configuration(s)

	Reset Configuration(s)	Hard Reset Configuration Word Read From	HPE Signal Sampled
MPC8260	Hardware Power On Reset	System Bus	not applicable
MSC8101	Hardware Power On Reset	System Bus	low
	Host Power On Reset	Host Interface	high

The MSC8101 adds support for host power-on reset configuration. The host power enable (HPE) signal determines which power-on-reset configuration is used for the MSC8101. HPE is sampled on the rising edge of $\overline{\text{PORESET}}$. When HPE is sampled high, the host port is enabled, and the host power-on reset configuration is used. That is, the external host processor initializes the reset configuration word through the host data interface.

Note: When the host port is used, the host must set the ISPS bit in the hard reset configuration word to make the system data bus 32-bits wide. Otherwise, improper operation may occur.

Alternately, when HPE is sampled low, the host port is disabled, and the hardware power-on reset configuration is used. That is, the hardware reset power-on reset sequence initializes the reset configuration word by reading data via the system bus.

Figure 5 shows the hardware power on reset sequence for both the MSC8101 and MPC8260.

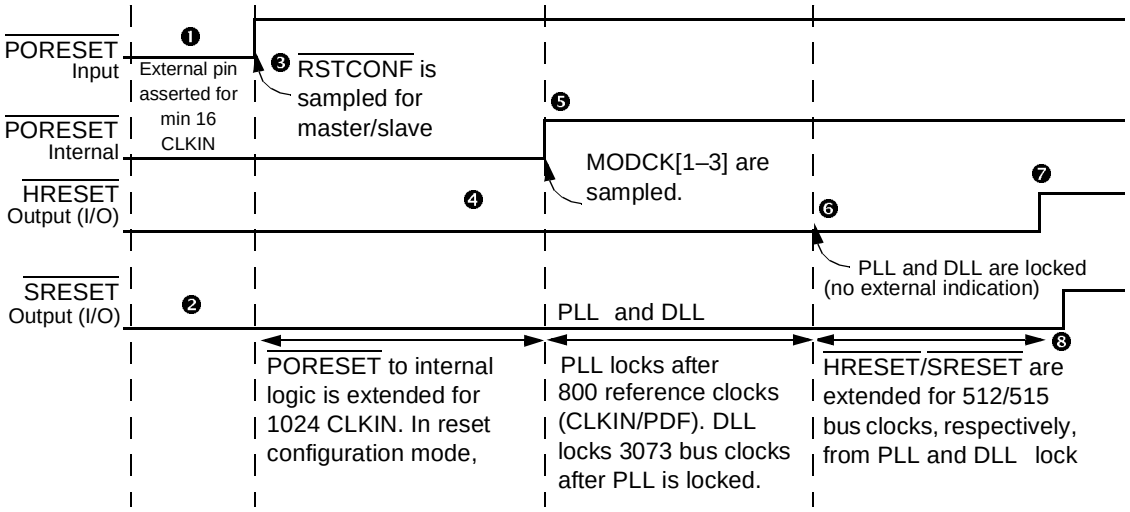


Figure 5. Hardware Reset Configuration Timing

Figure 6 shows the host reset power on reset sequence for the MSC8101. The sequence for the hardware reset configuration timing is described in **Table 11**.

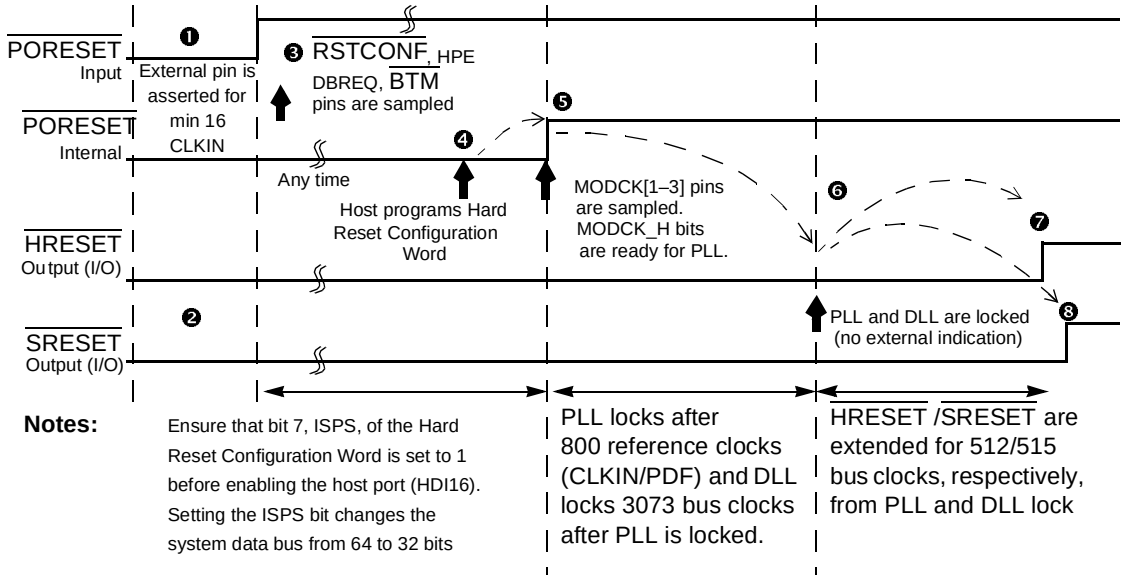


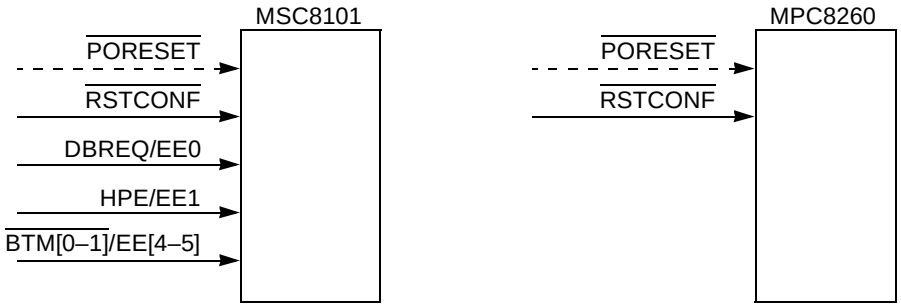
Figure 6. Host Reset Configuration Timing (MSC8101 only)

Table 11. Reset Sequence Descriptions

Sequence Number	MSC8101	MPC8260
å	The power-on reset pin (PORESET) starts the initialization process. PORESET should be asserted externally for at least 16 clock cycles after external power reaches at least 2/3 core voltage.	
ç	HRESET and SRESET pins are asserted low by the MSC8101 or MPC8260. **Notes:** HRESET and SRESET are bidirectional pins and use an open collector driver if driven externally.	
é	*Hardware Power-On Reset:* HPE is sampled low. RSTCONF is sampled on the rising edge of PORESET for master/slave determination. If RSTCONF is sampled high, there is only one MSC8101 in the system and the hard reset configuration word (HRCW) is set to all zeros. If RSTCONF is sampled low, eight HRCWs are read (corresponding to one master and seven slaves). Refer to **Section 13,** <Italics>Hard Reset Configuration Word for more information.	RSTCONF is sampled on the rising edge of PORESET for master/slave determination. If RSTCONF is sampled high, there is only one MPC8260 in the system and the hard reset configuration word (HRCW) is set to all zeros. If RSTCONF is sampled low, eight HRCWs are read (corresponding to one master and seven slaves). Refer to **Section 13,** <Italics>Hard Reset Configuration Word of this application note for more information.
	Host Power-On Reset: HPE is sampled high. The RSTCONF and BTM (boot mode) pins are sampled. The RSTCONF pin must be pulled up.	
è	*Hardware Power-On Reset:* Internally, the MSC8101 holds PORESET low for 1024 CLKIN cycles.	Internally, the MPC8260 holds PORESET low for 1024 CLKIN cycles.
	Host Power-On Reset: The MSC8101 extends the internal PORESET until the host programs the reset configuration word register. The host must write four 8-bit half-words to the host reset configuration register address to program the reset configuration word, which is 32 bits wide. **Notes:** While the host reset configuration register is programmed, the MSC8101 clocks are not set. It is assumed the host has its own clock.	
ê	When the internal PORESET line goes high, the MODCK[1–3] pins are sampled. These three pin values and the MODCK_H[28–31] bits in the HRCW define the core, CPM, and bus clock frequencies.	
ë	The phase-lock loop (PLL) is locked.	
í	The device deasserts HRESET.	
ì	Three cycles later, the device deasserts SRESET.	
î	*Hardware Power-On Reset:* The MSC8101 runs a boot program located in internal ROM. The source code for this boot program is listed in Appendix C in the *MSC8101 Reference Manual*. At the end of the boot code, the program jumps to an address located in the address table based on the ISB bits in the hard reset configuration word.	The program starts execution at the reset exception vector (0xFFF00100 or 0x00000100 depending on the CIP bit (bit 6) in the hard reset configuration word).
	Host Power-On Reset: The MSC8101 runs a boot program located in internal ROM. The source code for this boot program is listed in Appendix C in the *MSC8101 Reference Manual*. At the end of the boot code and after code is downloaded from the HDI16 port, the program jumps to the downloaded code.	

12 Power-On Reset Configuration Pins

During the power-on reset sequence and on the rising edge of PORESET, the MSC8101 samples five configuration signals versus one for the MPC8260. **Figure 7** shows PORESET and the configuration signals and their functions.



MSC8101	MPC8260
PORESET 0 = reset 1 = enter power-on reset state	PORESET 0 = reset 1 = enter power-on reset state
RSTCONF 0 = configuration master 1 = configuration slave	RSTCONF 0 = configuration master 1 = configuration slave
DBREQ/EE0 0 = core enters normal mode 1 = SC140 core enters debug mode	
HPE/EE1 0 = host port disabled (hardware power-on reset) 1 = host port enabled (host power-on reset) **Notes:** Host must program the HRCW to select system data bus size as 32 bits.	
BTM[0–1]/EE[4–5] 00 = MSC8101 boots from external memory 01 = MSC8101 boots from HDI16 10 = reserved 11 = reserved	

Figure 7. MSC8101/MPC8260 Configuration Pins

13 Hard Reset Configuration Word

The MSC8101 hard reset configuration word is based on that of the MPC8260. **Table 12** shows the fields in the MSC8101 reset configuration word that differ from those of the MPC8260.

Table 12. MSC8101 and MPC8260 HRCW Differences

HRCW Bit(s)	MSC8101 Bit Field	MPC8260 Bit Field
2	IRQINT. SIU configuration bit.	CDIS. MPC603e core disable bit.
6	SCDIS. SC140 disable bit.	CIP. Core initial exception prefix.
8–9	IRPC. SIU interrupt configuration.	L2CPC. L2 cache signal configuration.

Table 12. MSC8101 and MPC8260 HRCW Differences (Continued)

HRCW Bit(s)	MSC8101 Bit Field	MPC8260 Bit Field
12	NMIOUT. $\overline{\text{NMI}}$ service configuration.	Reserved.
13–15	ISB: • 000 = 0xF0000000 • 001 = 0xF0F00000 • 010 = 0xFF000000 • 011 = 0xFFF00000 • 100 = reserved, do not use • 101 = 0x00F00000 • 110 = 0x0F000000 • 111 = 0x0FF00000	ISB: • 000 = 0x00000000 • 001 = 0x00F00000 • 010 = 0x0F000000 • 011 = 0x0FF00000 • 100 = 0xF0000000 • 101 = 0xF0F00000 • 110 = 0xFF000000 • 111 = 0xFFF00000
16	Reserved.	BMS. Boot memory space selection.
20–21	Reserved.	LBPC. Local bus pin configuration.
22–23	TCPC. Transfer code pin configuration.	APPC. Address parity pin configuration.
24–25	BC1PC. BC1PC bit configuration.	CS10PC. CS10PC bit configuration.
27	DLLDIS. DLL disable bit.	Reserved.
28–30	MODCK_H.	MODCK_H[4–7].
31	Reserved.	

Refer to the following references for a more detailed look at the hard reset configuration words in each device.

- MSC8101 Reference Manual
- MSC8101 Software Initialization Overview Application Note (AN1852/D)
- MPC8260 PowerQUICC II User's Manual

14 Local Bus

The MSC8101 local bus is based on the local bus in the MPC8260. **Table 13** compares the local bus structures of the MSC8101 and MPC8260. The MSC8101 local bus is internally accessible only; the MPC8260 local bus is internally and externally accessible. The MSC8101 local bus supports twice as many data bits (64 versus 32) and almost twice as many address bits as the MPC8260 (32 versus 18). The MPC8260 local bus allows the CPM to support external memory independently of the system bus. If the MSC8101 CPM requires external memory, it must use the system bus. This may or may not affect performance depending on the application (that is, loading on the system bus, bus priorities, and so forth).

Table 13. Local Bus

Bus	MSC8101	MPC8260
Local	internal only	internal/external
Data	64 bits wide	32 bits wide
Address	32 bits wide	18 bits wide

15 MSC8101 Host Interface

The MSC8101 HDI16 interfaces an external host processor to the extended core. When enabled, the HDI16 replaces the lower 32 data bits (D[32–63]) in the system bus. The HDI16 is enabled during power-on reset by asserting the HPE signal. During the host power-on reset sequence, the host must set the ISPS bit in the HRCW to change the system data bus width from 64 bit to 32 bits. Failure to select the correct data bus width results in unpredictable operation. The HDI16 interface includes:

- 4 address lines
- 8 or 16 data bits
- 10 control lines

The 8 and 16 data bits support the following transfer modes:

- 8 data bits: supports 8, 16, 24 and 32 bit transfer modes
- 16 data bits: supports 16, 32, 48 and 64 bit transfer modes

The HDI16 appears as eleven memory-mapped registers:

- Interface Control Register (ICR)
- Interface Status Register (ISR)
- Transmit/Receive Data Registers (TX[0–3] and RX[0–3])
- Command Vector Register (CVR)
- Reset Configuration Registers (RSCFG[0–3])

TX[0–3] and RX[0–3] are double buffered for high speed data transfers.

One of the most innovative features of the HDI16 is the host command feature. The host can issue an interrupt request to the SC140 core. This allows the host to execute up to 128 pre-programmed application-specific functions stored in the core. The host sets up the vector address and code for the core to call and execute. The HDI16 supports an external DMA controller for 16-, 32-, 48-, and 64-bit data transfers. The HDI16 external DMA support is not related to the SIU or CPM SDMAs.

16 CPM Revisions

The MSC8101 CPM hardware and microcode are based upon the MPC8260 HiP4 MPC8260 CPM.

17 TDM Interfaces

Even though the MSC8101 and MPC8260 contain a similar CPM module, not all the CPM pins are available externally, as follows:

- The MSC8101 supports four TDM interfaces: TDMA1, TDMB2, TDMC2, and TDMD2.
- The MPC8260 supports eight TDM interfaces: TDMA1, TDMB1, TDMC1, TDMD1, TDMA2, TDMB2, TDMC2, and TDMD2.
- There are two serial interfaces (SI1 and SI2). The “1” and “2” at the end of the TDM names indicate which serial interface (SI) they belong to: SI1 or SI2. The MSC8101 has one TDM from SI1

(TDMA1) and three from SI2 (TDMB2, TDMC2, and TDMD2). The MSC8101 TDM interfaces are split between SI1 and SI2 to allow for higher system performance. TDMA1 is special because it supports both bit and nibble data modes.

18 CPM Protocols

Table 14 summarizes the protocols available for each communications controller.

Table 14. MSC8101 and MPC8260 Communications Controllers Versus Protocols

Protocol	Communications Controllers								
	FCC1	FCC2	FCC3	SCC1-2	SCC3-4	MCC1-2	SMC1-2	SPI	I^2C
ATM (Utopia 16)	D								
ATM (Utopia 8)	A	D							
ATM (serial)	A	D							
Ethernet (100BaseT)	A	A	D						
Ethernet (10BaseT)	A	A	D	A	D				
HDLC	A	A	B	A	B				
HDLC_BUS	A	A	D	A	D				
TRANSPARENT	A	A	B	A	B		A		
UART				A	D		A		
GCI							C		
Multi-channel HDLC						C			
Multi-channel transparent						C			
BISYNC				A	A				
SPI								A	
I^2C									A

Notes: **1.** The following symbols are used in this table:
- A = MSC8101 and MPC8260
- B = MSC8101 TDM only and MPC8260 TDM and NMSI
- C = MSC8101 and MPC8260 TDM only
- D = MPC8260 only

2. A serial device is not forced to choose a serial device clock from a predefined pin or BRG.

3. A group of serial receivers and transmitters can share the same clock rate from the same pin.

19 Clocks and Baud-Rate Generators

The clocks for the communications controllers, timers and time division multiplexers (TDMs) derive from a bank of eight internal baud-rate generators (BRGs) and ten external clock (CLK) pins for the MSC8101, and 20 external clock pins for the MPC8260 (see **Table 15**). **Table 16** and **Table 17** show which communications controllers, timers and TDMs can use which clock and BRG for the MSC8101 and MPC8260, respectively.

Table 15. Number of Clocks and Baud-Rate Generators

Device	Number of Clocks	Number of Baud Rate Generators
MSC8101	10	8
MPC8260	20	8

For details, refer to the chapters on CPM multiplexing and BRGs in the *MSC8101 Reference Manual*.

Table 16. MSC8101 Clock and BRG Options

Controller/ Channel	CLK										BRG							
	1	2	3	4	5	6	7	8	9	10	1	2	3	4	5	6	7	8
SCC1 Rx	+	+	+	+							+	+	+	+				
SCC1 Tx	+	+	+	+							+	+	+	+				
SCC2 Rx	+	+	+	+							+	+	+	+				
SCC2 Tx	+	+	+	+							+	+	+	+				
FCC1 Rx	+	+							+	+					+	+	+	+
FCC1 Tx	+	+							+	+					+	+	+	+
FCC2 Rx			+	+	+	+									+	+	+	+
FCC2 Tx			+	+	+	+									+	+	+	+
TDMA1 Rx	+								+									
TDMA1 Tx		+								+								
TDMB2 Rx					+		+											
TDMB2 Tx						+		+										
TDMC2 Rx			+				+											
TDMC2 Tx				+				+										
TDMD2 Rx	+								+									
TDMD2 Tx		+								+								
SMC1 Rx							+		+		+						+	
SMC1 Tx							+		+		+						+	
SMC2 Rx									+	+		+						+
SMC2 Tx									+	+		+						+
TIN1				+														
TIN2			+															
TIN3								+										
TIN4							+											
BRG1			+		+													
BRG2			+		+													

Table 16. MSC8101 Clock and BRG Options (Continued)

Controller/ Channel	CLK										BRG							
	1	2	3	4	5	6	7	8	9	10	1	2	3	4	5	6	7	8
BRG3					+				+									
BRG4					+				+									
BRG5			+		+													
BRG6			+		+													
BRG7					+				+									
BRG8					+				+									

Table 17. MCP8260 Clock and BRG Options

Controller/ Channel	CLK																				BRG							
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	1	2	3	4	5	6	7	8
SCC1 Rx			+	+						+	+										+	+	+	+				
SCC1 Tx			+	+						+	+										+	+	+	+				
SCC2 Rx			+	+						+	+										+	+	+	+				
SCC2 Tx			+	+						+	+										+	+	+	+				
SCC3 Rx					+	+	+	+													+	+	+	+				
SCC3 Tx					+	+	+	+													+	+	+	+				
SCC4 Rx					+	+	+	+													+	+	+	+				
SCC4 Tx					+	+	+	+													+	+	+	+				
FCC1 Rx									+	+	+	+													+	+	+	+
FCC1 Tx									+	+	+	+													+	+	+	+
FCC2 Rx													+	+	+	+									+	+	+	+
FCC2 Tx													+	+	+	+									+	+	+	+
FCC3 Rx													+	+	+	+									+	+	+	+
FCC3 Tx													+	+	+	+									+	+	+	+
TDMA1 Rx	+																		+									
TDMA1 Tx		+																		+								
TDMB1 Rx			+						+																			
TDMB1 Tx				+						+																		
TDMC1 Rx					+								+															
TDMC1 Tx						+								+														
TDMD1 Rx							+								+													
TDMD1 Tx								+								+												
TDMA2 Rx					+								+															
TDMA2 Tx						+								+														
TDMB2 Rx															+		+											
TDMB2 Tx																+		+										
TDMC2 Rx			+														+											
TDMC2 Tx				+														+										

Table 17. MCP8260 Clock and BRG Options (Continued)

Controller/ Channel	CLK																				BRG							
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	1	2	3	4	5	6	7	8
TDMD2 Rx	+																		+									
TDMD2 Tx		+																		+								
SMC1 Rx							+		+												+						+	
SMC1 Tx							+		+												+						+	
SMC2 Rx																			+	+		+						+
SMC2 Tx																			+	+		+						+
TIN1				+																								
TIN2			+																									
TIN3																+												
TIN4															+													
BRG1			+		+																							
BRG2			+		+																							
BRG3									+						+													
BRG4									+						+													
BRG5			+		+																							
BRG6			+		+																							
BRG7									+						+													
BRG8									+						+													

20 Interrupts

The MSC8101 includes three interrupt controllers (PIC, SIC, SIC_EXT) versus one (IC) for the MPC8260. **Table 18** shows the modules to which the interrupt controllers belong. For details on interrupts, refer to the *MSC8101 Reference Manual* and *MPC8260 User's Manual.*

Table 18. Interrupt Controller Location

Interrupt Controller Location	MSC8101	MPC8260	Typical Interrupt Sources
Extended Core	PIC (programmable interrupt controller)	Not applicable	QBC, Host, EFCOP
SIU	SIC (SIU-CPM interrupt controller)	IC (interrupt controller)	PIT, TMCNT, CPM, port C
SIU	SIC_EXT (external SIU-CPM interrupt controller)	Not applicable	Same as SIC, IRQ2-3, DMA

The MPC8260 IC and MSC8101 SIC are similar. The MPC8260 interrupt controller (IC) is renamed to the SIU-CPM interrupt controller (SIC) in the MSC8101. The PIC interrupt controller is added to the MSC8101 extended core to manage the interrupts in the extended core (QBC, HOST, EFCOP, Q2PPC Bridge) and the interrupts coming from the SIC in the SIU. **Figure 8** and **Figure 9** show the functional block diagram for the MPC8260 and MSC8101 interrupt structure, respectively.

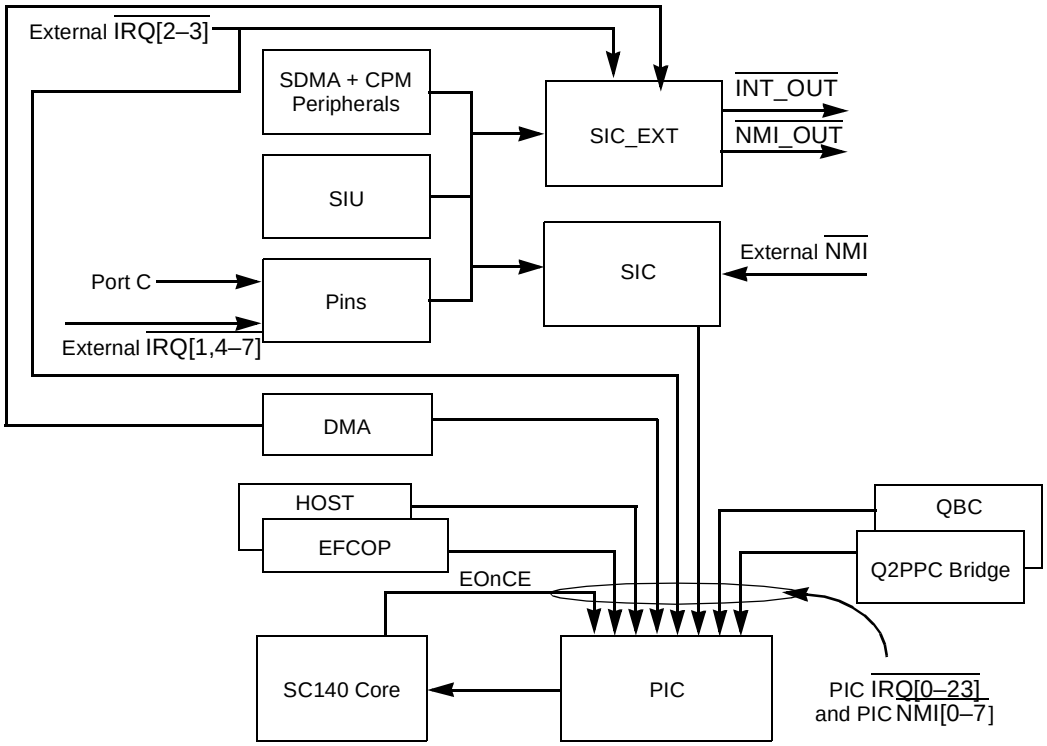


Figure 8. MSC8101 Interrupt Structure

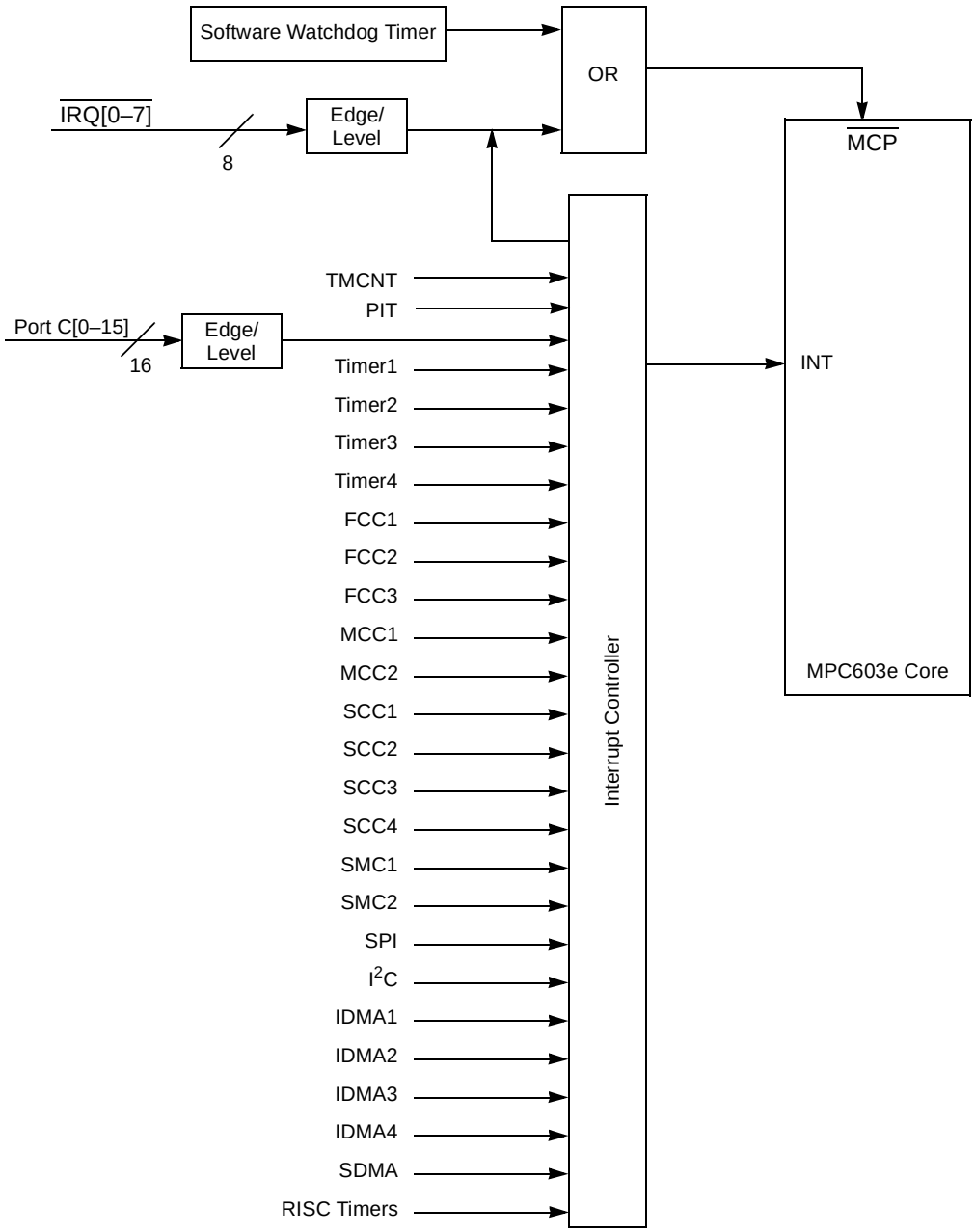


Figure 9. MPC8260 Interrupt Structure

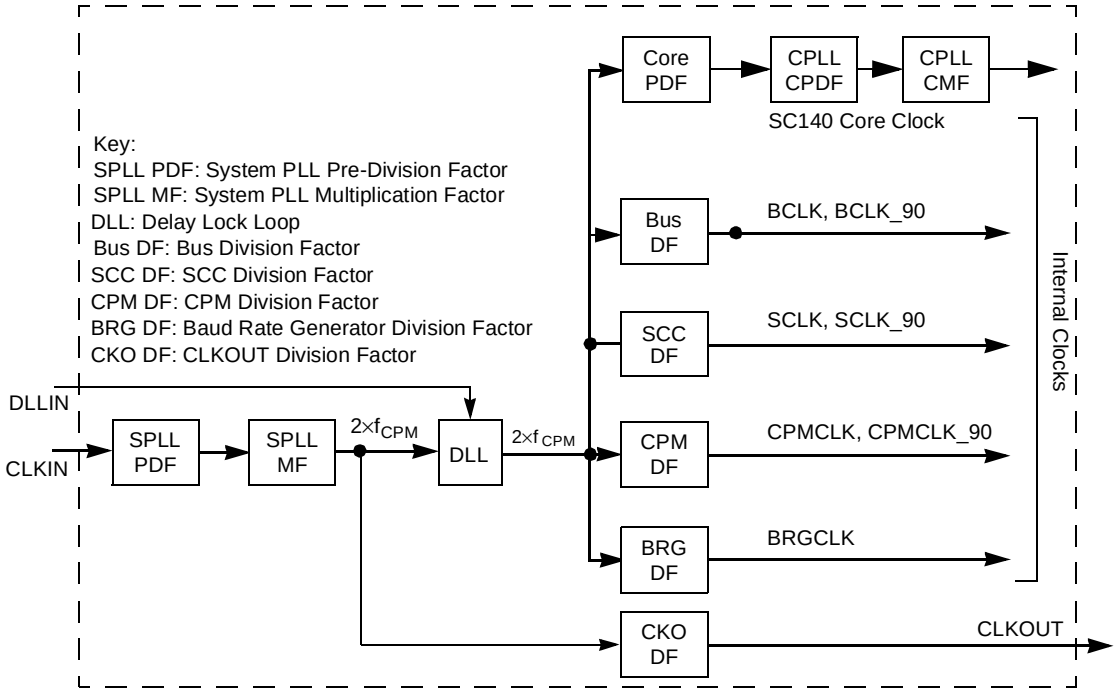
Table 19 summarizes the interrupts for the two devices. The MSC8101 has 15 interrupt lines (8 from the CPM I/O and 7 from the SIU) versus 24 interrupt lines (16 from the CPM I/O and 8 from the SIU) for the MPC8260.

Table 19. MSC8101 and MPC8260 Interrupts

Description	MSC8101	MPC8260
IRQs (CPM)	PC[4–7], PC[12–15] (8 I/O lines)	PC[0–15] (16 I/O lines)
IRQs (SIU)	$\overline{\text{IRQ[1–7]}}$ (7 interrupt lines)	IRQ[0–7] (8 interrupt lines)

21 Clocks

Figure 10 and **Figure 11** show the MSC8101 and MPC8260 clock functional block diagrams, respectively. The MSC8101 added a DLL block. Refer to the MSC8101 and MPC8260 respective data sheets and errata documents for up-to-date information. Refer to the *MSC8101 Technical Data* sheet, *MPC8260 User's Manual*, and specific device errata for clock programming information.



Notes: **1.** SPLL PDF is determined by the clock configuration mode.

1. SPLL MF is determined by the clock configuration mode.
2. The Bus DF = CLKOUT DF and is 4 or 5 as determined by the clock configuration mode.
3. SCC DF is always 4.
4. CPM DF is always 2.
5. BRG DF is set by the System Clock Control Register (SCCR) and is 4, 16 (default), 64, or 256.

Figure 10. MSC8101 Clock Functional Block Diagram

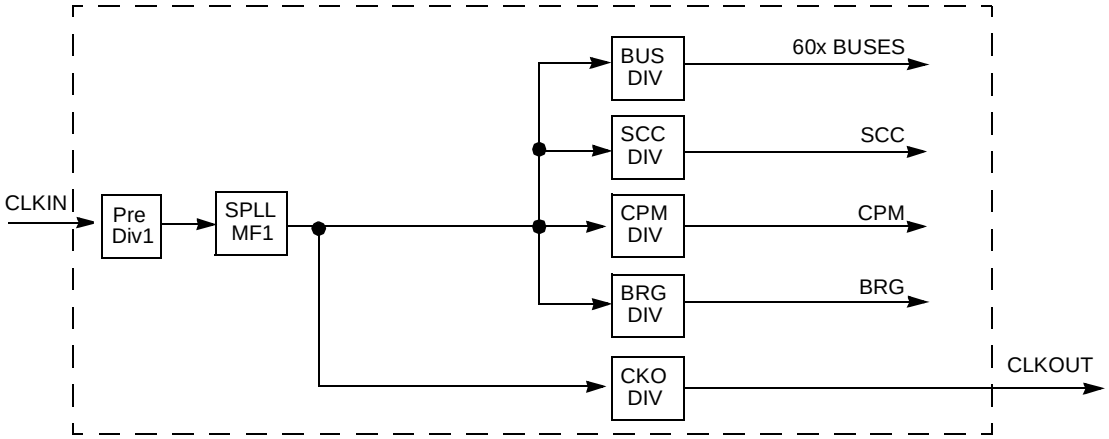


Figure 11. MPC8260 Clock Functional Block Diagram

22 References

[1] *Functional Pin Differences Between the MSC8101 and MPC8260 CPMs* (AN1851)

[2] *Initializing the MSC8101 Communications Processor Module (CPM) I/O* (AN1854)

[3] *MPC8260 PowerQUICC II™ User's Manual* (MPC8260UM)

[4] *MSC8101 Programmer User's Guide* (MSC8101UG)

[5] *MSC8101 Reference Manual* (MSC8101RM)

[6] *MSC8101 Software Initialization Overview* (AN1852)

[7] *MSC8101 Technical Data* (MSC8101)

[8] *Newton's Telecom Dictionary: The Official Dictionary of Telecommunications*, ©1998, by Harry Newton

NOTES:

NOTES:

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations not listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GMBH
Technical Information Center
Schatzbogen 7
81829 München, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T. Hong Kong
+800 2666 8080

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Order No.: AN2162
Rev. 2
11/2005