Freescale Semiconductor

Application Note

MPC8260 SDRAM Timing Diagrams

The MPC8260 PowerQUICC™ II integrated communications processor provides one SDRAM interface for the 60x bus and one for local bus. These interfaces provide the necessary control function and signals for the JEDEC-compliant SDRAM devices.

This application note presents a series of timing diagrams for several SDRAM scenarios. All the timing diagrams are based on simulations.

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1   60x Bus Access

60x bus access is partitioned to two sub-groups: single MPC8260 mode and external bus mode (60x-compatible).

1.1   Single MPC8260 Bus Mode

To enter single MPC8260 bus mode, clear the hard reset configuration word, HRCW[EBM], bit during the configuration. In this bus mode, the MPC8260 is the only bus master device in the system. The internal memory controller controls all devices on the external bus. The slave device cannot use all the 60x bus signals because the addresses have memory timing, not address/data tenure timing. See Example 1 and Example 2.

Example 1. Assembly Language Example of a Single-Beat Read/Write

```
# Setup OR1

addis r2,r0,0xfff0

ori r2,r2,0x0c40

addis r1,r0,0x0f01

ori r1,r1,0x010c

stw r2, 0x0000(r1)


# Setup BR1

addis r2,r0,0x0100

ori r2,r2,0x1841

addis r1,r0,0x0f01

ori r1,r1,0x0108

stw r2, 0x0000(r1)


# PSDMR OP = Mode Register Write

addis r2,r0,0x9800

ori r2,r2,0x9602

addis r1,r0,0x0f01

ori r1,r1,0x0100

stw r2, 0x0090(r1)


# first hit to write SDRAM mode

addis r2,r0,0x0100

ori r2,r2,0x0000

stb r1, 0x0008(r2)
```

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```
# PSDMR OP = normal

addis r2,r0,0x8000

ori r2,r2,0x9602

stw r2, 0x0090(r1)


# single write to 0x0100_0008

addis r2,r0,0x0100

ori r2,r2,0x0000

stw r1, 0x0008(r2)


# single read from 0x0100_0018

lwz r3, 0x0018(r2)
```

Example 2. Assembly Language Example of a Burst Read/Write by IDMA

```
# Setup OR1

addis r2,r0,0xffff

ori r2,r2,0x2cc0

addis r1,r0,0x0f01

ori r1,r1,0x010c

stw r2, 0x0000(r1)


#Setup BR1

addis r2,r0,0x0100

ori r2,r2,0x1841

addis r1,r0,0x0f01

ori r1,r1,0x0108

stw r2, 0x0000(r1)


# PSDMR OP = Mode Register Write

addis r2,r0,0x9b4c

ori r2,r2,0x9512

addis r1,r0,0x0f01

ori r1,r1,0x0100

stw r2, 0x0090(r1)
```

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```
# First hit to write SDRAM mode
addis r2,r0,0x0100
ori r2,r2,0x0000
stb r1, 0x0008(r2)


# PSDMR OP = normal
addis r2,r0,0x834c
ori r2,r2,0x9512
stw r2, 0x0090(r1)


# PDIRC
addis r2,r0,0x0000
ori r2,r2,0x0100
addis r1,r0,0x0f01
ori r1,r1,0x0d40
stw r2, 0x0000(r1)


# PPARC
addis r2,r0,0x8000
ori r2,r2,0x0300
addis r1,r0,0x0f01
ori r1,r1,0x0d44
stw r2, 0x0000(r1)


# PSORC
addis r2,r0,0x0000
ori r2,r2,0x0300
addis r1,r0,0x0f01
ori r1,r1,0x0d48
stw r2, 0x0000(r1)


# PODRC
addis r2,r0,0x0000
ori r2,r2,0x0200
addis r1,r0,0x0f01
```

```
ori r1,r1,0x0d4c
stw r2, 0x0000(r1)


# RCCR = 0000 0000
addis r2,r0,0x0000
ori r2,r2,0x0000
addis r1,r0,0x0f01
ori r1,r1,0x19c4
stw r2, 0x0000(r1)


# IDMA1_BASE = 1000h
addis r2,r0,0x0000
ori r2,r2,0x1000
addis r1,r0,0x0f01
ori r1,r1,0x87fe
sth r2, 0x0000(r1)


# base address for memory access at r1
addis r1,r0,0x0f01
ori r1,r1,0x1000


# BD start at 2000h
addis r2,r0,0x0000
ori r2,r2,0x2000
sth r2, 0x0000(r1)


# DCM
addis r2,r0,0x0000
ori r2,r2,0x0070
sth r2, 0x0002(r1)


# IBDPTR
addis r2,r0,0x0000
ori r2,r2,0x2000
sth r2, 0x0004(r1)
```

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```
# DPR_BUF
addis r2,r0,0x0000
ori r2,r2,0x4000
sth r2, 0x0006(r1)


#SS_MAX 0x0a
addis r2,r0,0x0000
ori r2,r2,0x0060
sth r2, 0x000a(r1)


# STS 0x0e
addis r2,r0,0x0000
ori r2,r2,0x0060
sth r2, 0x000e(r1)


# DTS 0x16
addis r2,r0,0x0000
ori r2,r2,0x0060
sth r2, 0x0016(r1)


# ISTATE 0x28
addis r2,r0,0x0000
ori r2,r2,0x0000
sth r2, 0x0028(r1)


# base address for memory access at r1
addis r1,r0,0x0f00
ori r1,r1,0x2000


# BD1
addis r2,r0,0x8868
ori r2,r2,0x1000
stw r2, 0x0000(r1)
```

```
# Data length

addis r2,r0,0x0000

ori r2,r2,0x022a

stw r2, 0x0004(r1)


# source buffer pointer

addis r2,r0,0x0100

ori r2,r2,0x0000

stw r2, 0x0008(r1)


# destination buffer pointer

addis r2,r0,0x0100

ori r2,r2,0x0100

stw r2, 0x000c(r1)


# base address for memory access at r1

addis r1,r0,0x0f00

ori r1,r1,0x4000


# START IDMA1

addis r2,r0,0x1e81

ori r2,r2,0x0009

addis r1,r0,0x0f01

ori r1,r1,0x19c0

stw r2, 0x0000(r1)
```

In summary, the basic steps to program GPCM, as outlined in the *MPC8260 PowerQUICC II™ Family Reference Manual*, are as follows:

1. For 60x bus, program SIUMCR[BCTLC] for $\overline{\text{BCTL0}}$ polarity.
2. Program ORx for $\overline{\text{CS}}$ and $\overline{\text{WE}}$ timing.
3. Program BRx[MS] to select GPCM and appropriate bus, BRx[PS] for port size, and so on.

Figure 1 shows a single-beat read access to the 60x bus.
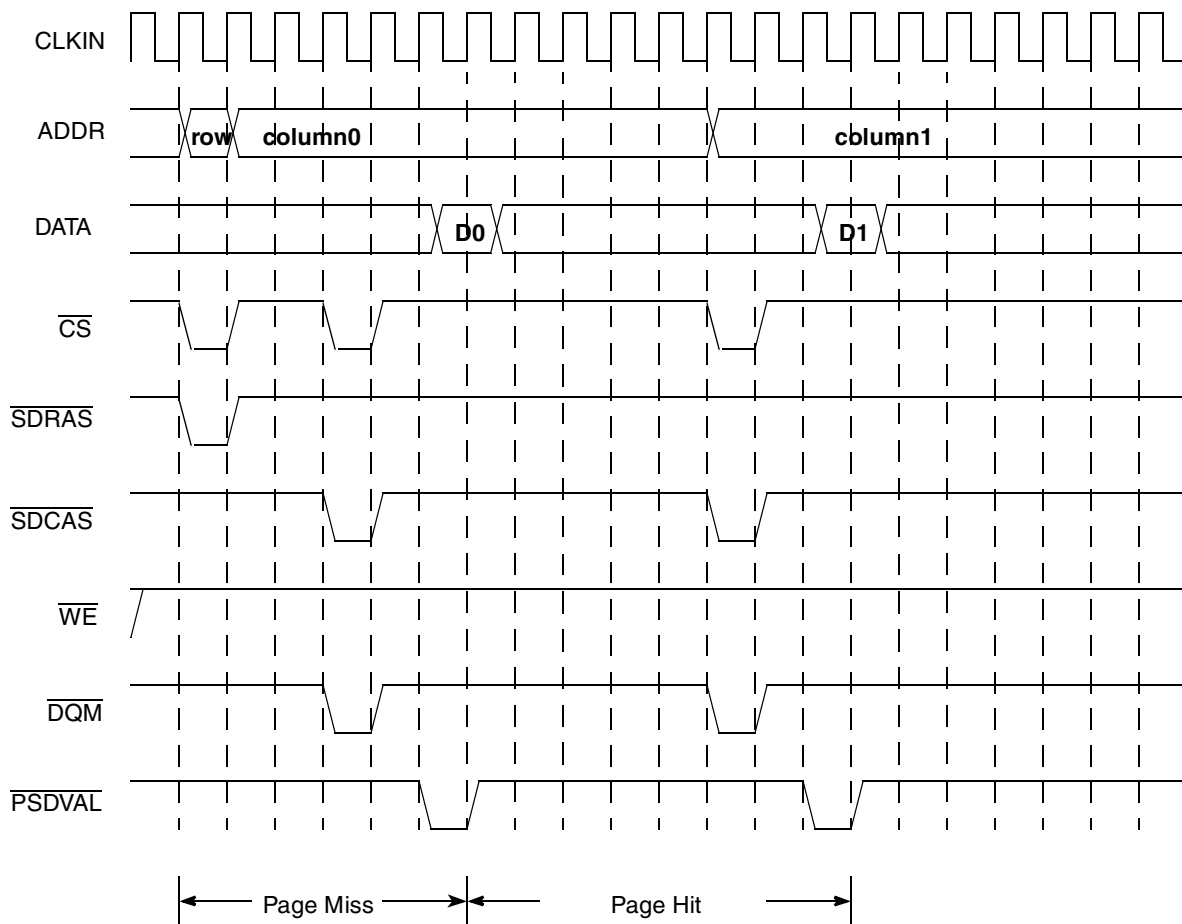
PSDMR[ACTTORW] = 011, PSDMR[CL] = 2

Figure 1. 60x Access in Single MPC8260 Mode, Single-Beat Read

Figure 2 shows a single-beat write access to the 60x bus.
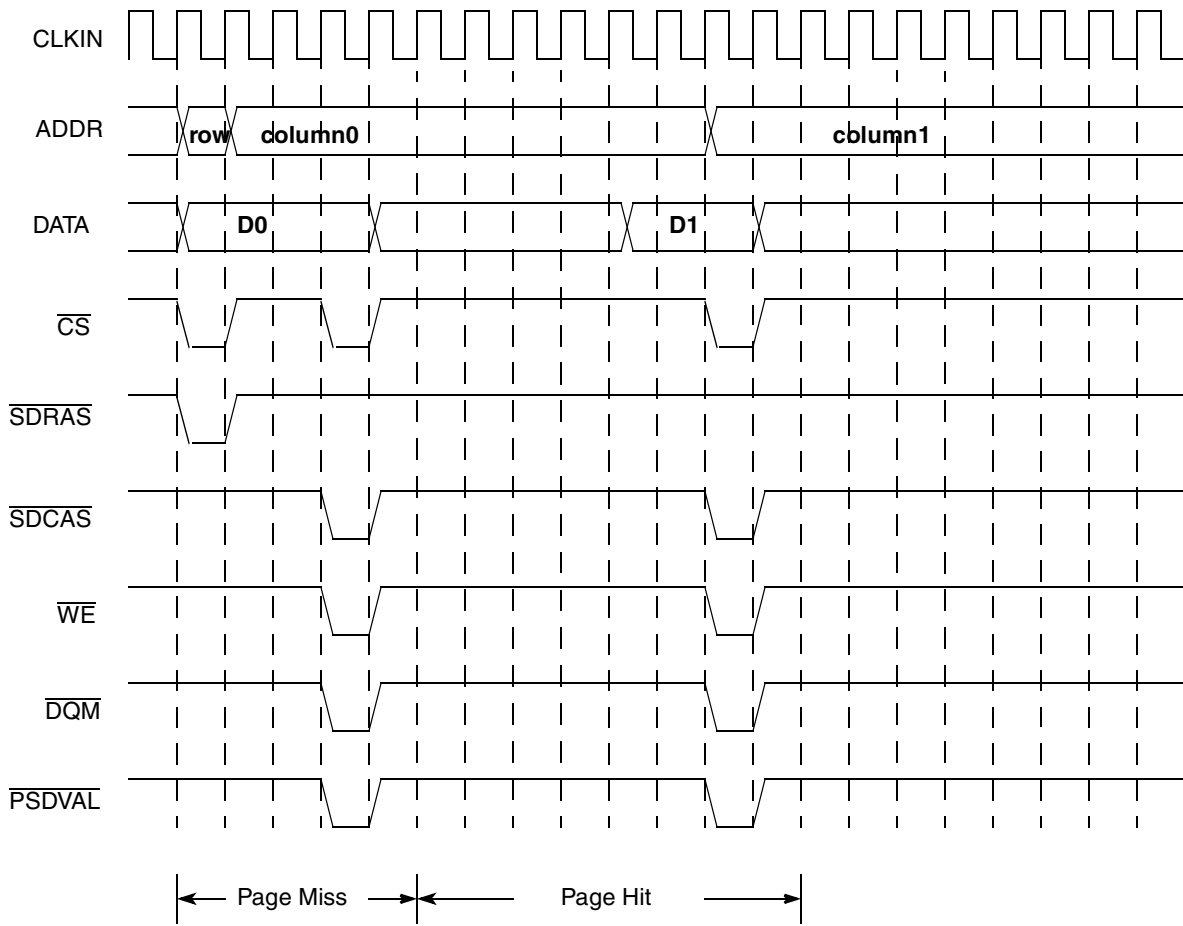
PSDMR[ACTTORW] = 011, PSDMR[CL] = 2

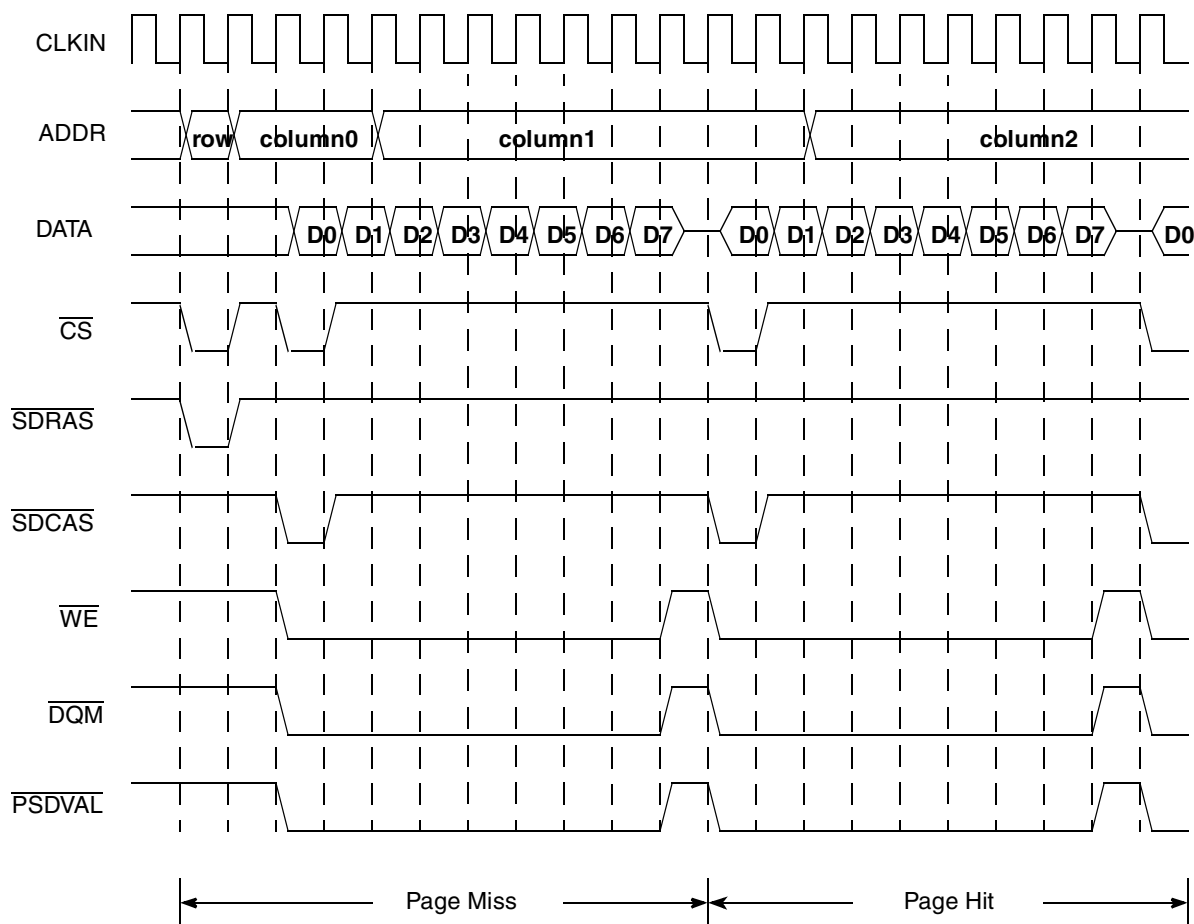**Figure 2. 60x Access in Single MPC8260 Mode, Single-Beat Write**

Figure 3 shows a burst read access to the 60x bus.
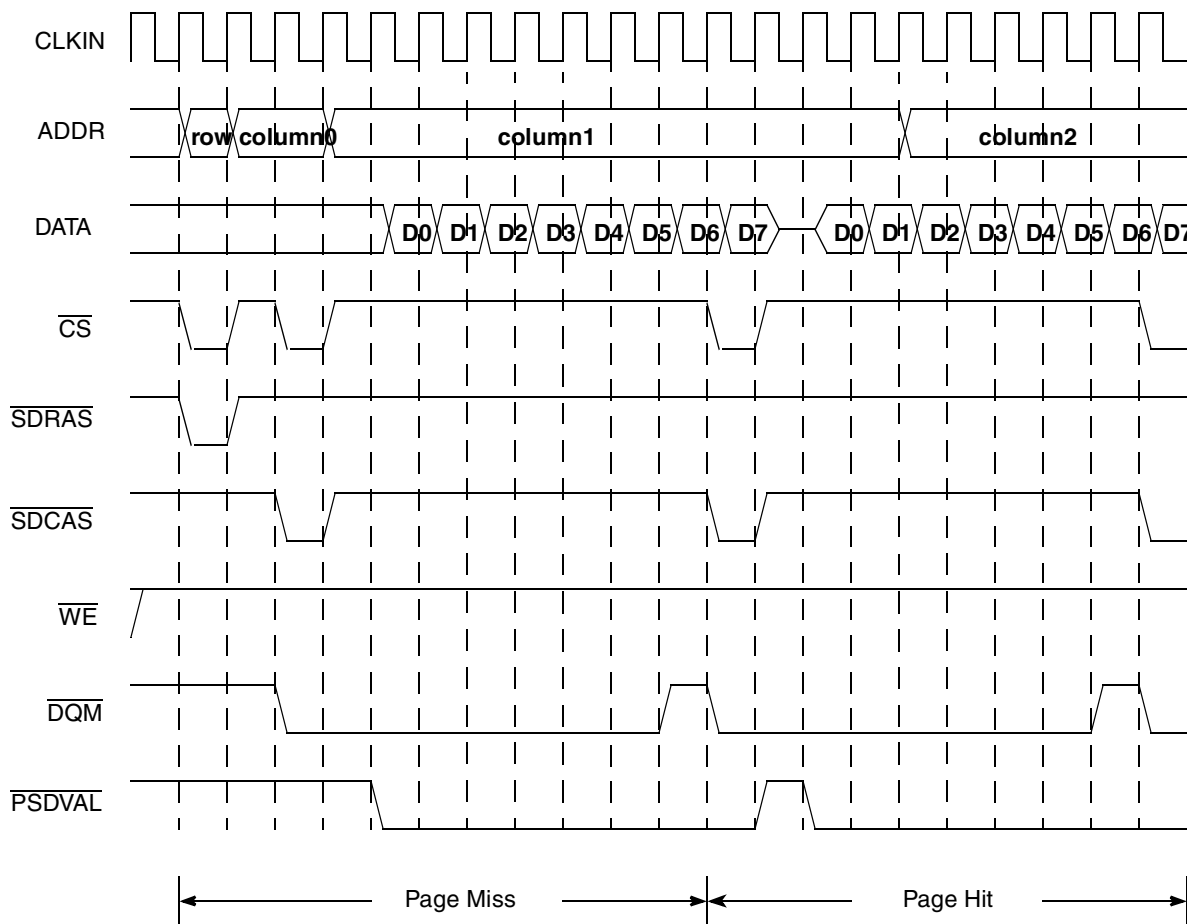
PSDMR[ACTTORW] = 010, PSDMR[CL] = 2, PSDMR[BL] = 1(Busrt Length = 8)

Figure 3. 60x Access in Single MPC8260 Mode, Port Size = 32, Burst Read (Burst Length = 8)

Figure 4 shows a burst write access to the 60x bus.

PSDMR[ACTTORW] = 010, PSDMR[CL] = 2, PSDMR[BL] = 1(Busrt Length = 8)

Figure 4. 60x Access in Single MPC8260 Mode, Port Size = 32, Burst Write (Burst Length = 8)

1.2   External Bus Mode (60x-Compatible)

To enter 60x-compatible bus mode, set the HRCW[EBM] bit during configuration. In this bus mode, the lower bits of the 60x address to memory are controlled by BADDR[27:31]. Note that BADDR[29:31] are multiplexed with other signals. The multiplexing is controlled by SIUMCR[L2CPC]. The BADDR[29:31] function is chosen when the L2CPC bits of hard reset configuration word are configured with a value of 10 during powerup or by programming this value directly to SIUMCR after the configuration.

Additional controls are available in 60x-compatible mode:

- ALE—External address latch enable
- PSDAMUX—External address multiplexing control (asserted=row, negated=column)
- BNKSEL[0–2]—Bank select address to allow internal bank interleaving

For an assembly language example, refer to the GPCM single MPC8260 mode example.

Note that for external bus mode, all the 60x bus signals are shown to illustrate the 60x bus nature of the access most clearly.

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Figure 5 shows a single read in 60x-compatible mode.
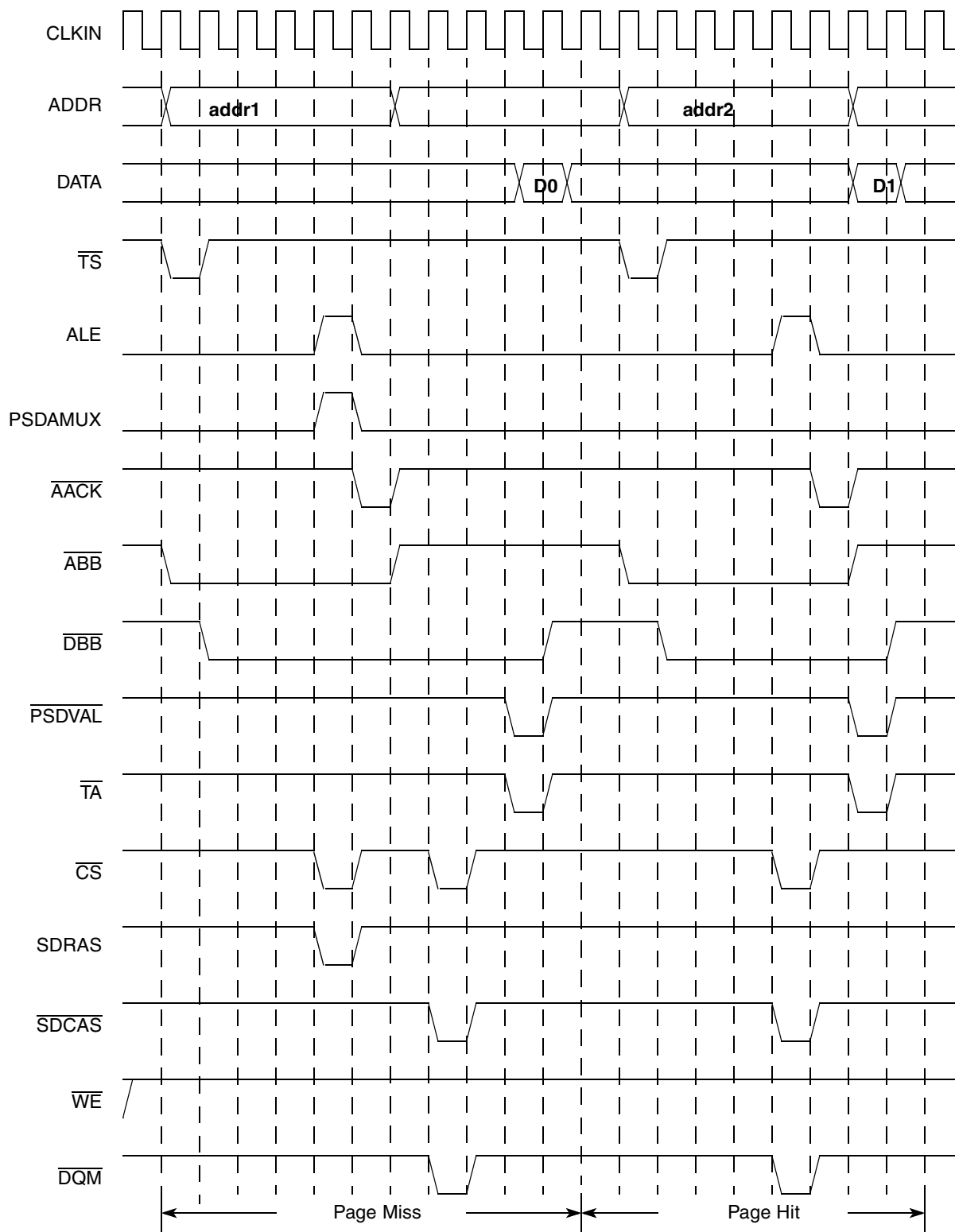
PSDMR[ACTTORW] = 011, PSDMR[CL] = 2

Figure 5. 60x Bus in 60x-Compatible Mode, Single Read

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Figure 6 shows a single-beat write in 60x-compatible mode.

PSDMR[ACTTORW] = 011, PSDMR[CL] = 2
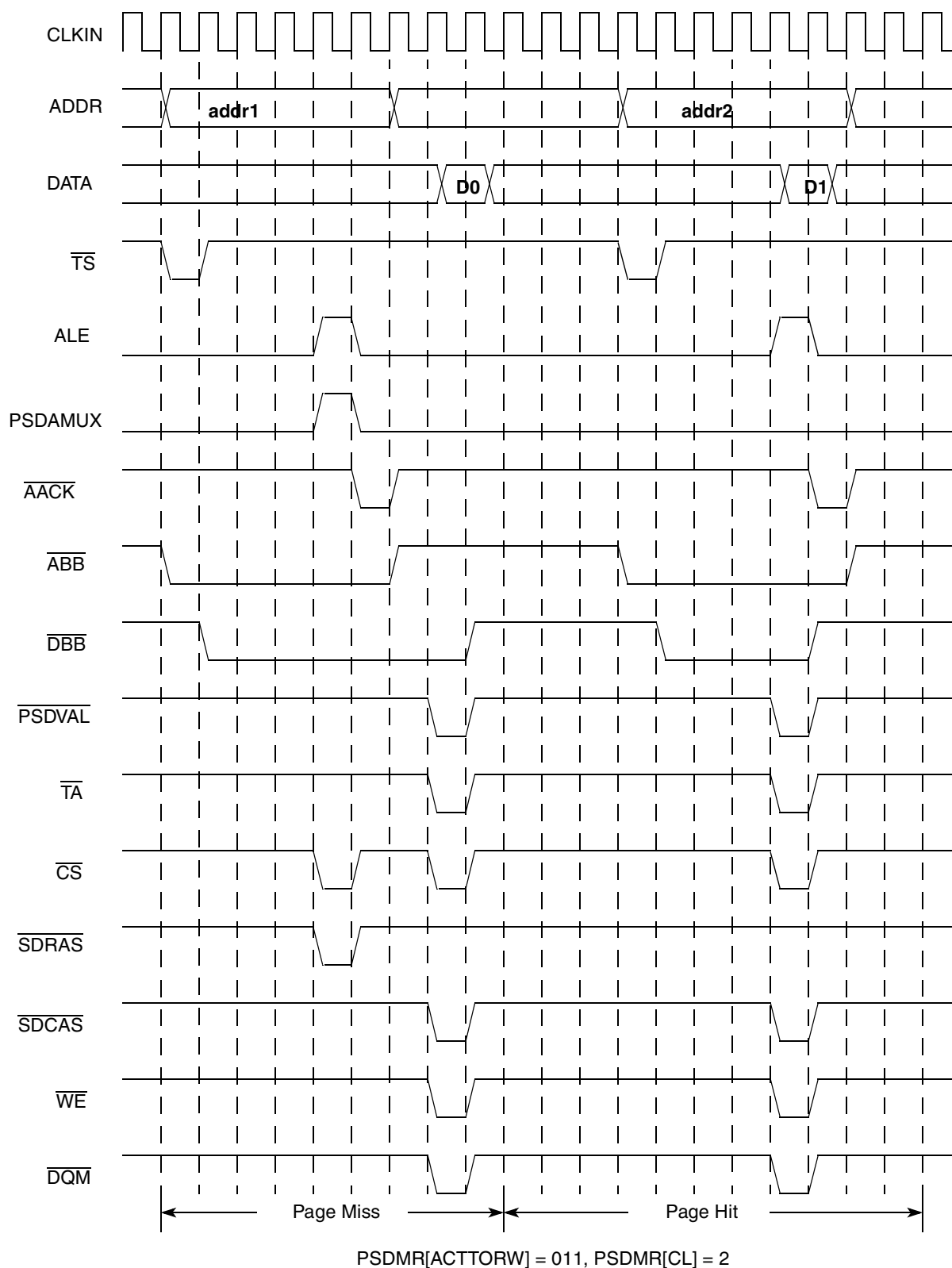
Figure 6. 60x Access in 60x-Compatible Mode, Single-Beat Write

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Figure 7 shows a burst read in 60x-compatible mode.

PSDMR[ACTTORW] = 011, PSDMR[CL] = 2
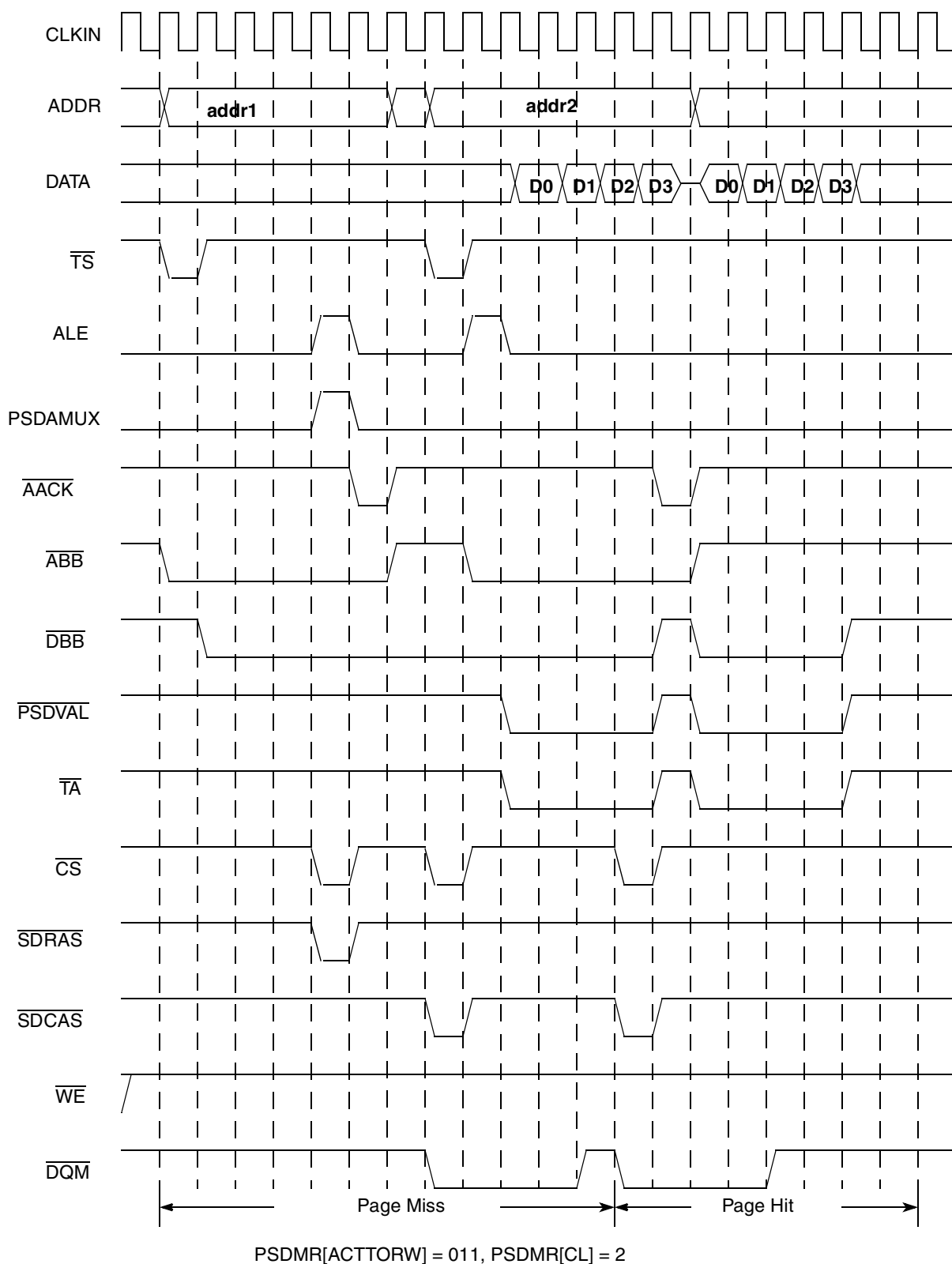
Figure 7. 60x Access in 60x-Compatible Mode, Burst Read (Burst Length=4, Port Size = 64)

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Figure 8 shows a burst write.

PSDMR[ACTTORW] = 011, PSDMR[CL] = 2
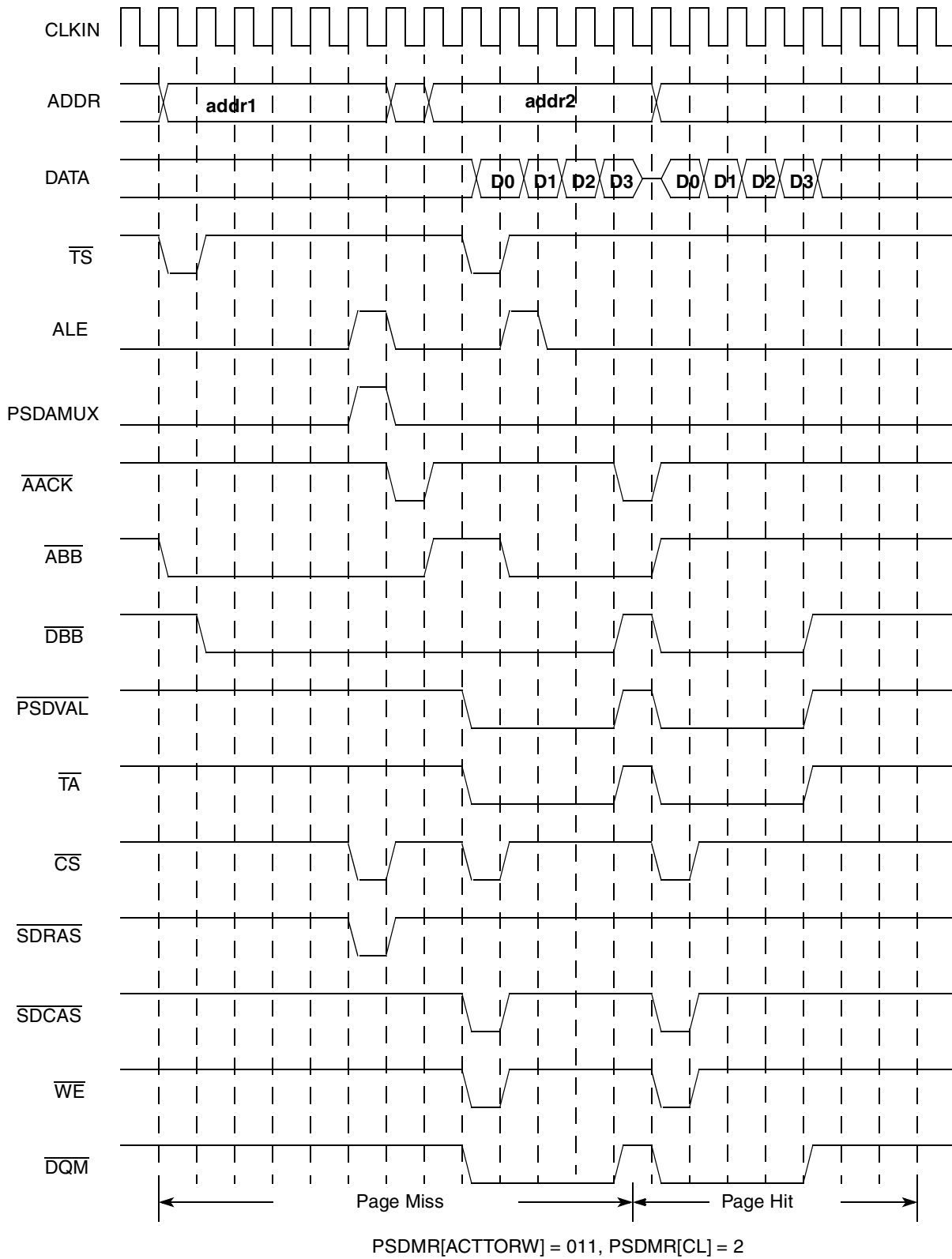
Figure 8. 60x Access in 60x-Compatible Mode, Burst Write (Burst Length = 4, Port Size = 64)

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2   Local Bus Access

The local bus access functions the same way for both single-MPC8260 mode and 60x-compatible mode. The local bus has its own signals:

- Local address bus
- Local data bus
- $\overline{\text{LSDRAS}}$
- $\overline{\text{LSDCAS}}$
- $\overline{\text{LWE}}$
- $\overline{\text{LDQM}}$

The local address pins are multiplexed with PCI signals. To select the local bus function of these pins, configure HRCW[L2CPC] to a value of 00 during configuration or program them with this value after configuration. Figure 9 shows a single-beat read local bus transaction.

LSDMR[ACTTORW] = 011, LSDMR[CL] = 2
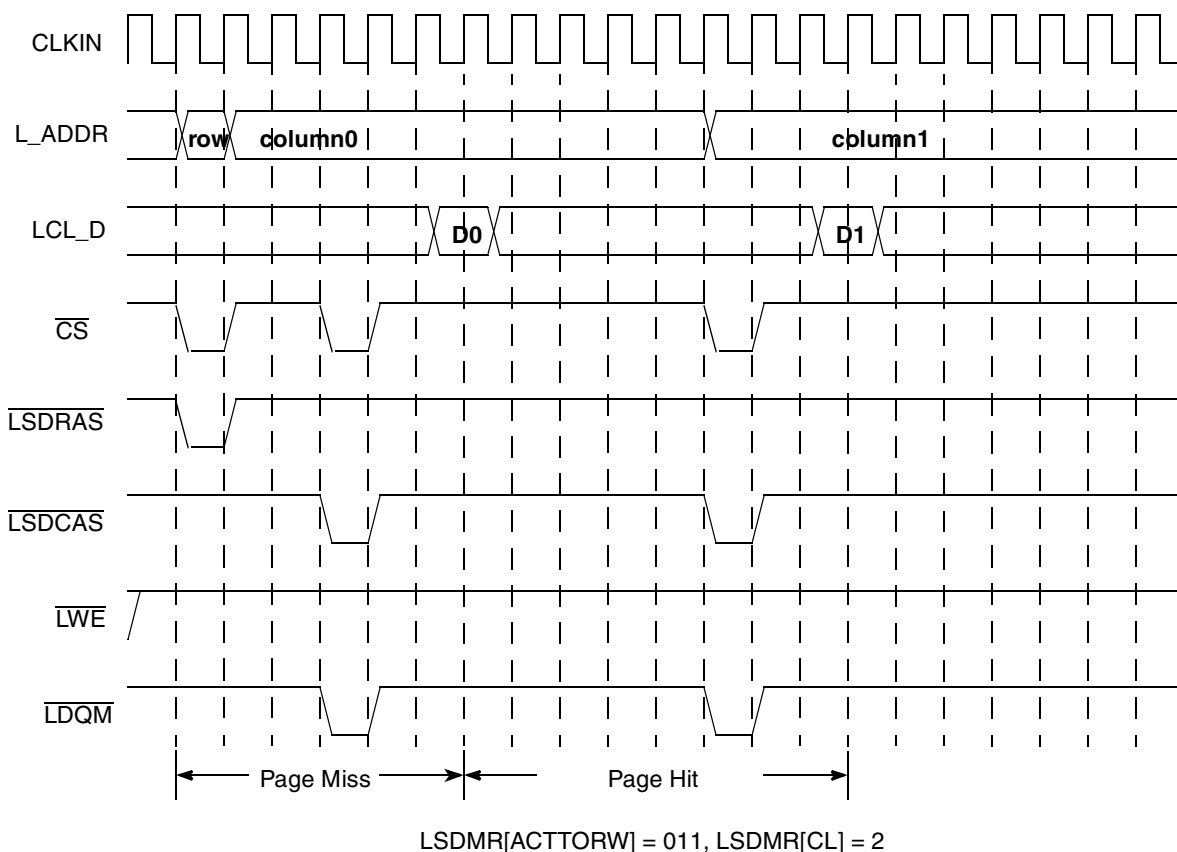
Figure 9. Local Bus Access, Single-Beat Read

Figure 10 shows a local bus single-beat write.

LSDMR[ACTTORW] = 011, LSDMR[CL] = 2
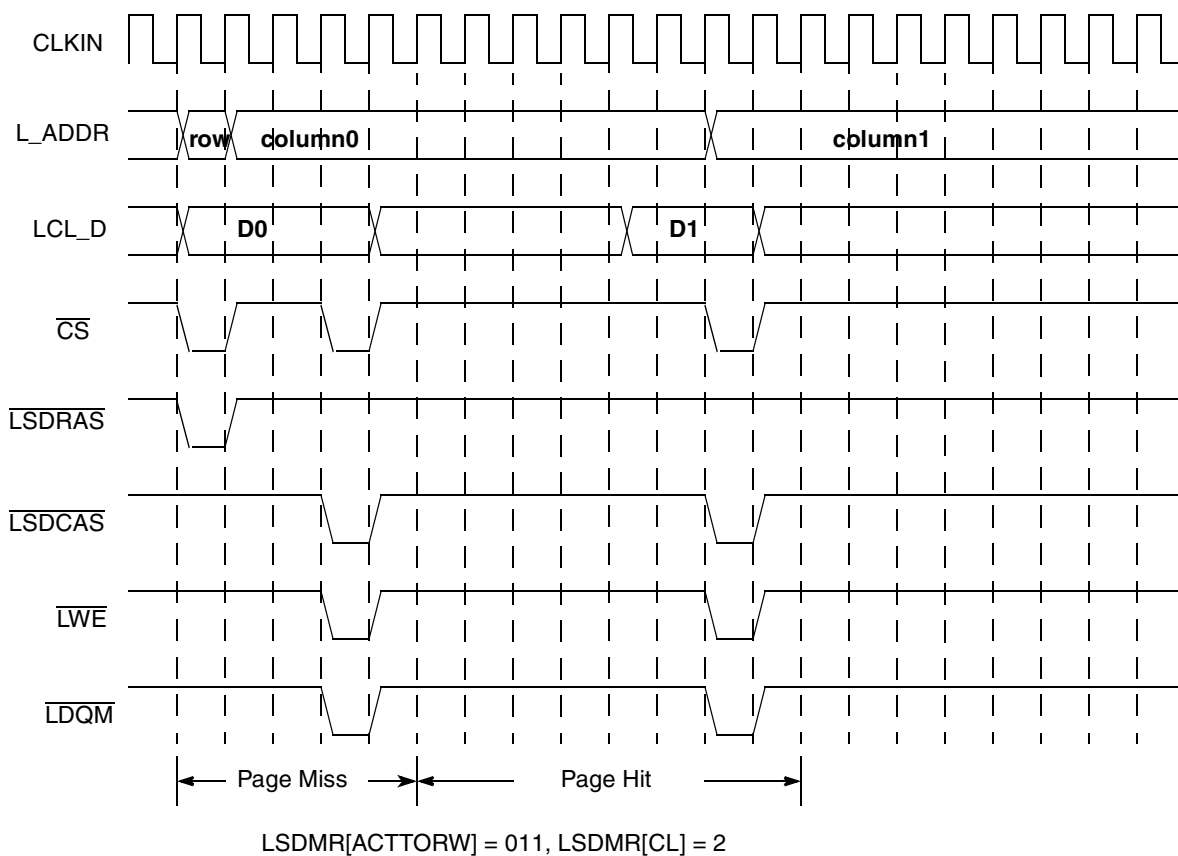
Figure 10. Local Bus Access, Single-Beat Write

Figure 11 shows a burst read on the local bus.

LSDMR[ACTTORW] = 010, LSDMR[CL] = 2, LSDMR[BL] = 1(Burst Length = 8)
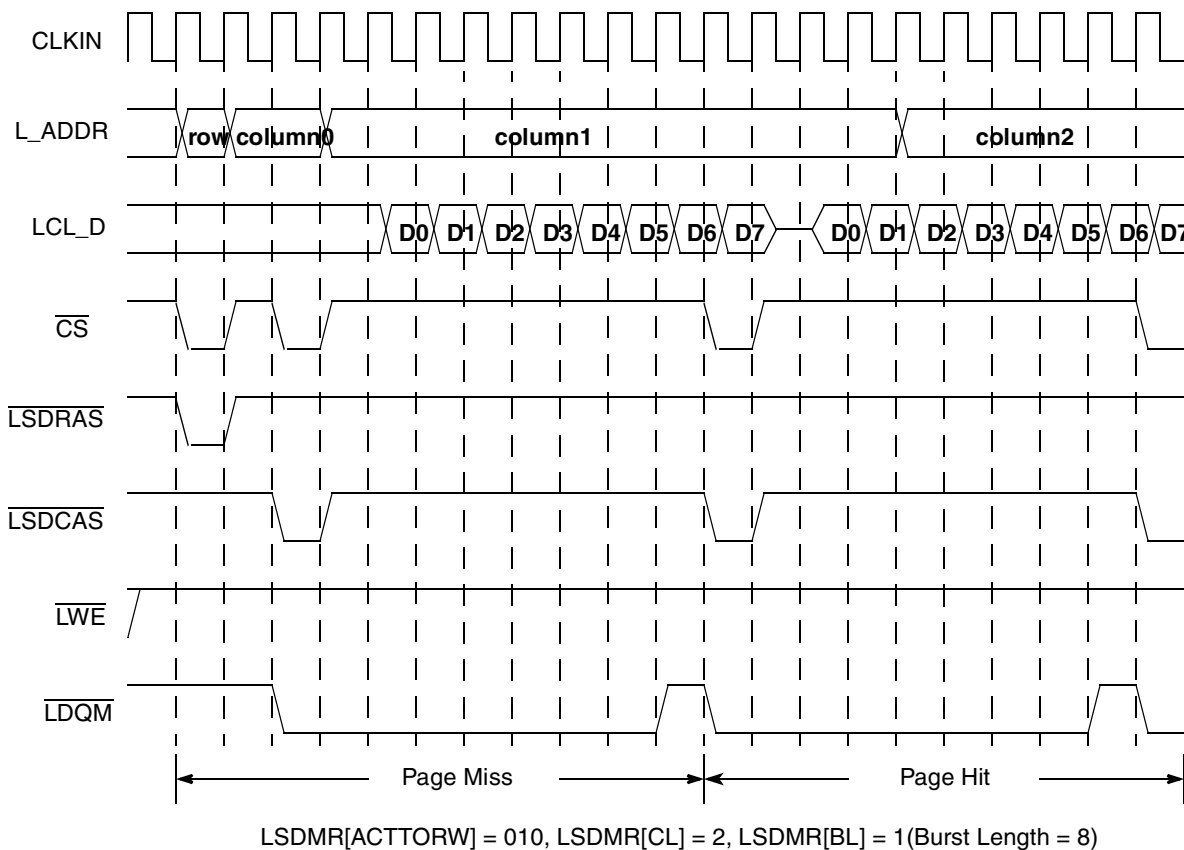
Figure 11. Local Bus Access, Burst Read (Burst Length = 8)

Figure 12 shows a burst write on the local bus.

LSDMR[ACTTORW] = 010, LSDMR[CL] = 2, LSDMR[BL] = 1(Burst Length = 8)
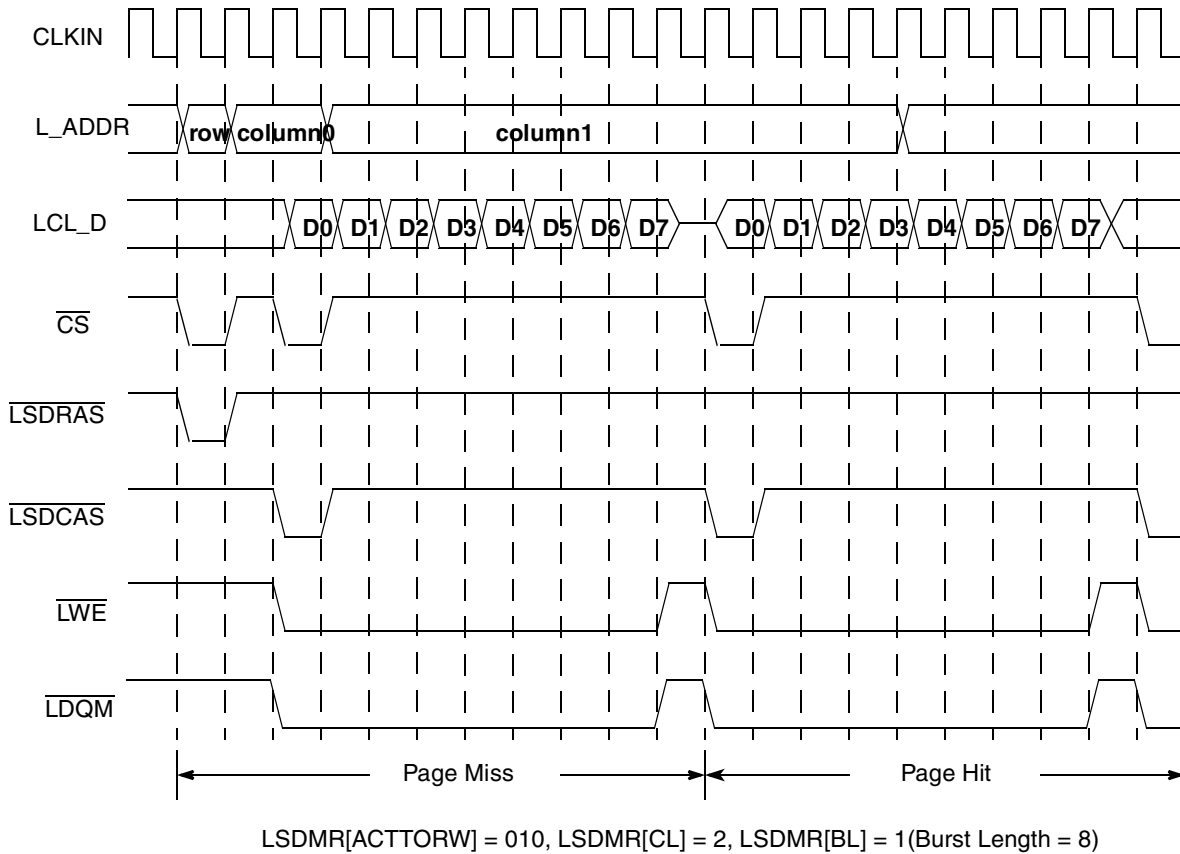
Figure 12. Local Bus Access, Burst Write (Burst Length = 8)

3 Read-Modify-Write Cycle

If the SDRAM is programmed to do read-modify-write parity checking or ECC correction and checking, every write access to memory that is less than the port size automatically causes a read-modify-write cycle. In Figure 13 and Figure 14, the read-modify-write cycle is caused by a 32-bit write to a 64-bit port. In Figure 15, the read-modify-write cycle is caused by a 16-bit write to a 32-bit port.

Figure 13 shows a 60x read-modify-write cycle in single-MPC8260 mode.
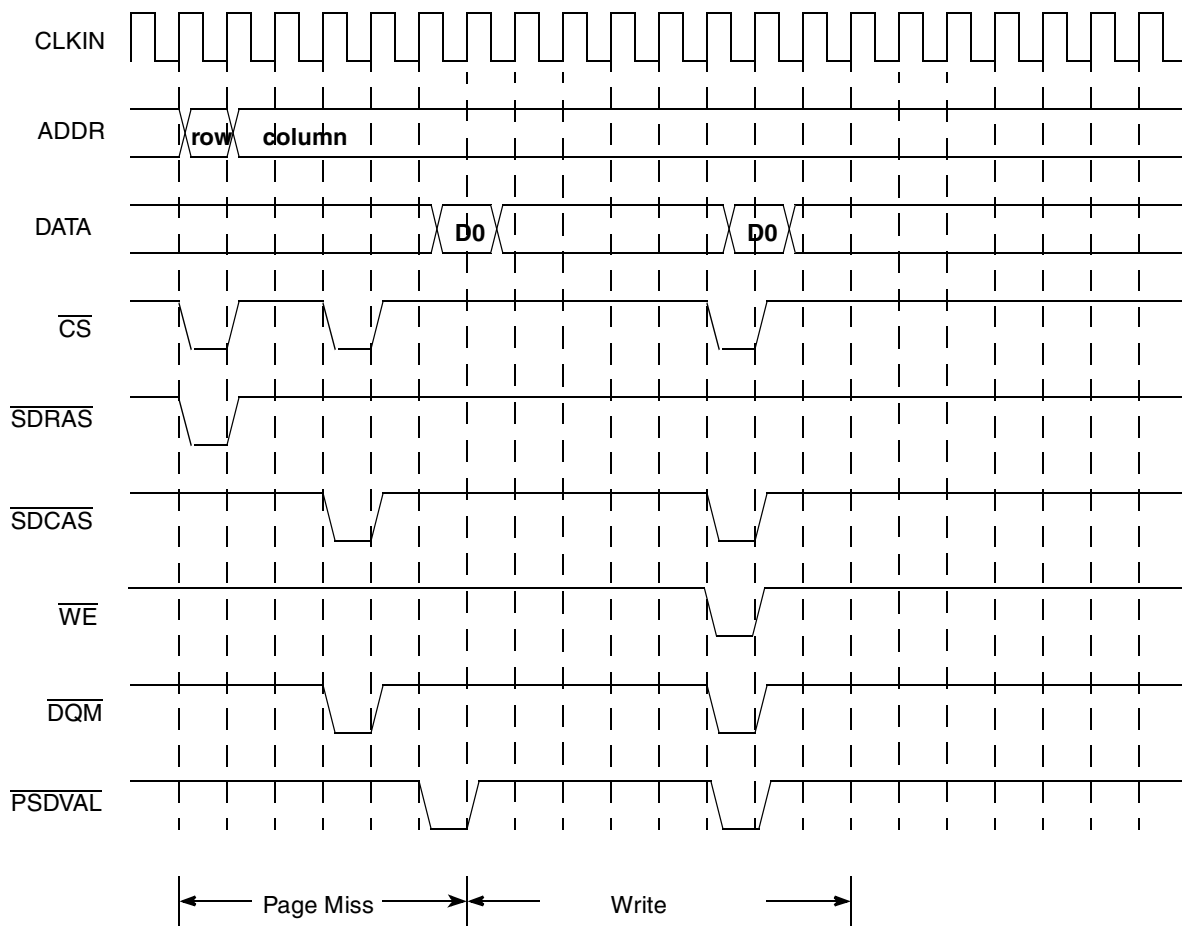
PSDMR[ACTTORW] = 011, PSDMR[CL] = 2

Figure 13. 60x Access in Single MPC8260 mode, Read-Modify-Write Cycle

Figure 14 shows a 60x read-modify-write cycle in 60x-compatible mode.

PSDMR[ACTTORW] = 011, PSDMR[CL] = 2
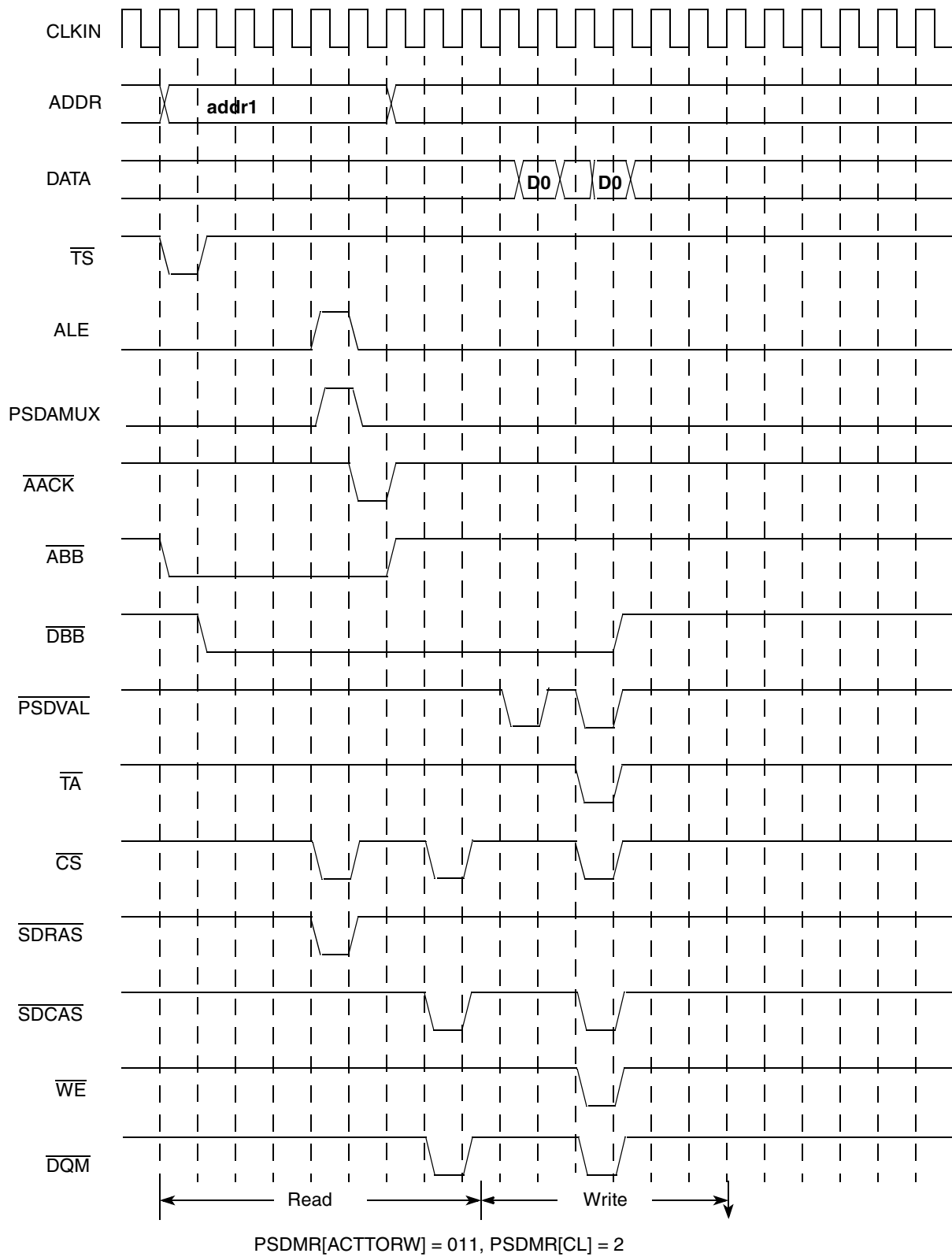
Figure 14. 60x Access in 60x-Compatible Mode, Read-Modify-Write Cycle

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Figure 15 shows a read-modify-write cycle on the local bus.

LSDMR[ACTTORW] = 011, LSDMR[CL] = 2
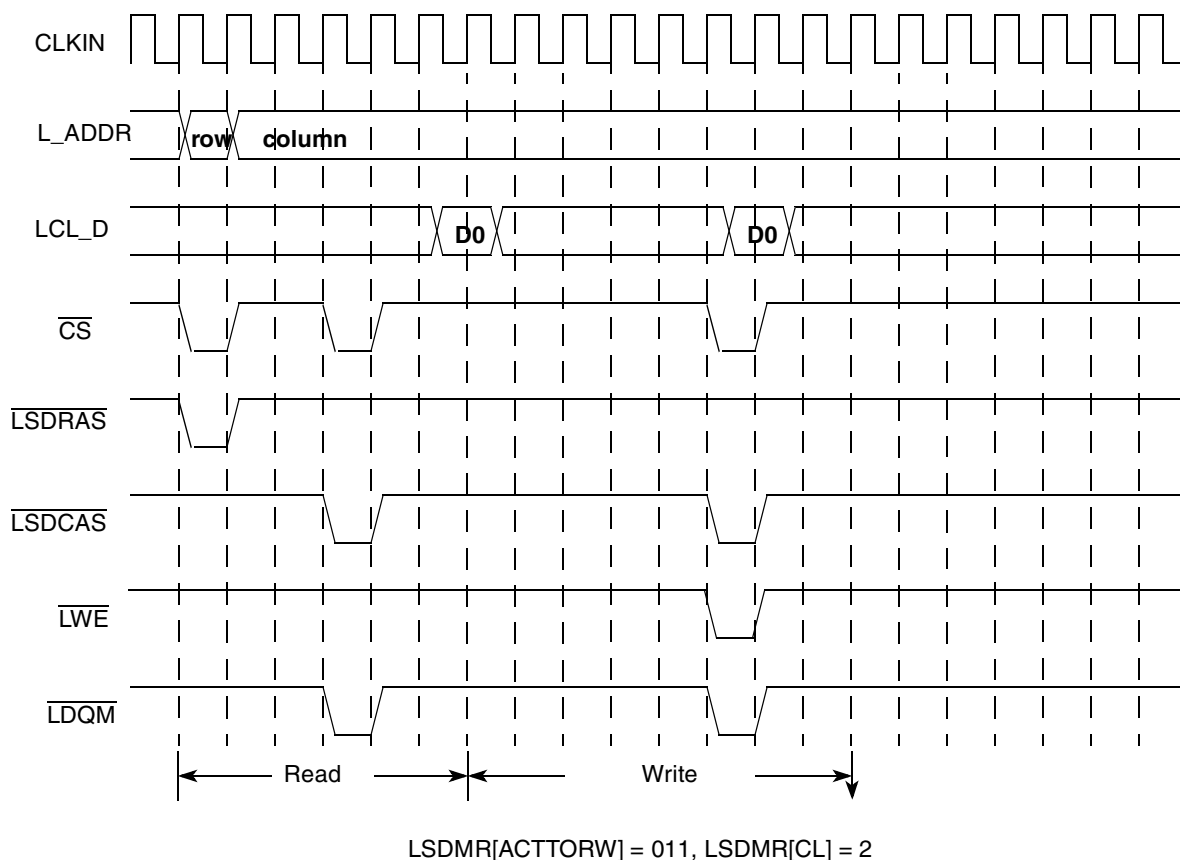
Figure 15. Local Bus Access, Read-Modify-Write Cycle

4 $\overline{\text{ARTRY}}$ Cycle

In 60x-compatible mode, the address transfer can be terminated with the requirement to retry if $\overline{\text{ARTRY}}$ is asserted during the address tenure and through the cycle following $\overline{\text{AACK}}$. The assertion causes the entire transaction (address and data tenure) to be rerun.

Figure 16 shows an $\overline{\text{ARTRY}}$ cycle in 60x-compatible mode.
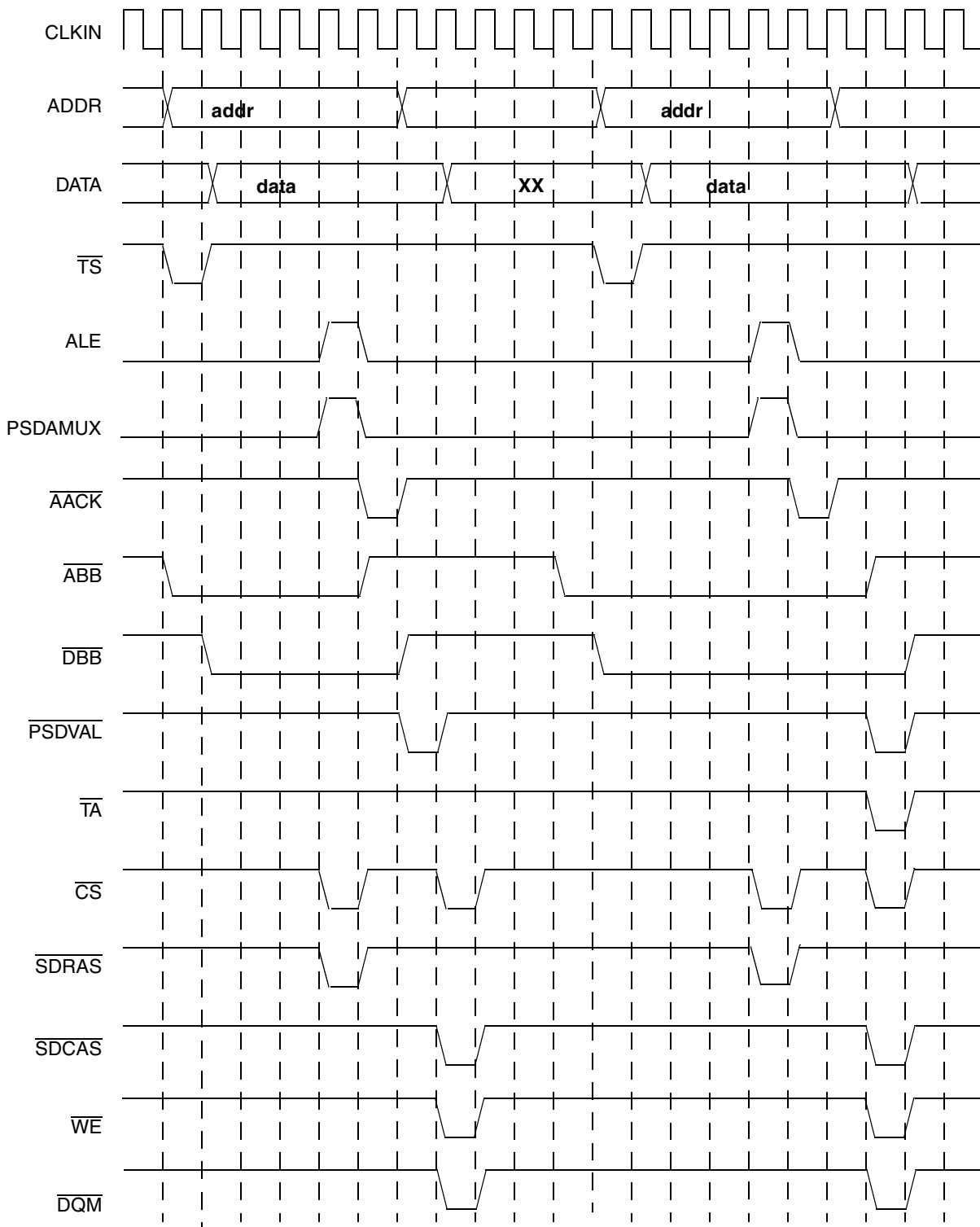
Figure 16. 60x Access in 60x-Compatible Mode, $\overline{\text{ARTRY}}$ Cycle

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