Order Number: AN2246
Rev 1.0, 11/2000

PowerPC™

Application Note

MPC8260 60x Bus Timing Diagram

Freescale NetComm, Austin

0.0 Introduction

All the timing diagrams are generated based on the simulations.

The timing diagrams are organized as followings:

1. External 60x Master Transactions
2. External 60x Slave Transactions.

freescale™ semiconductor

1. External 60x Master Transaction

1.1 External 60x Master Writes to Memory (GPCM) on 60x Bus

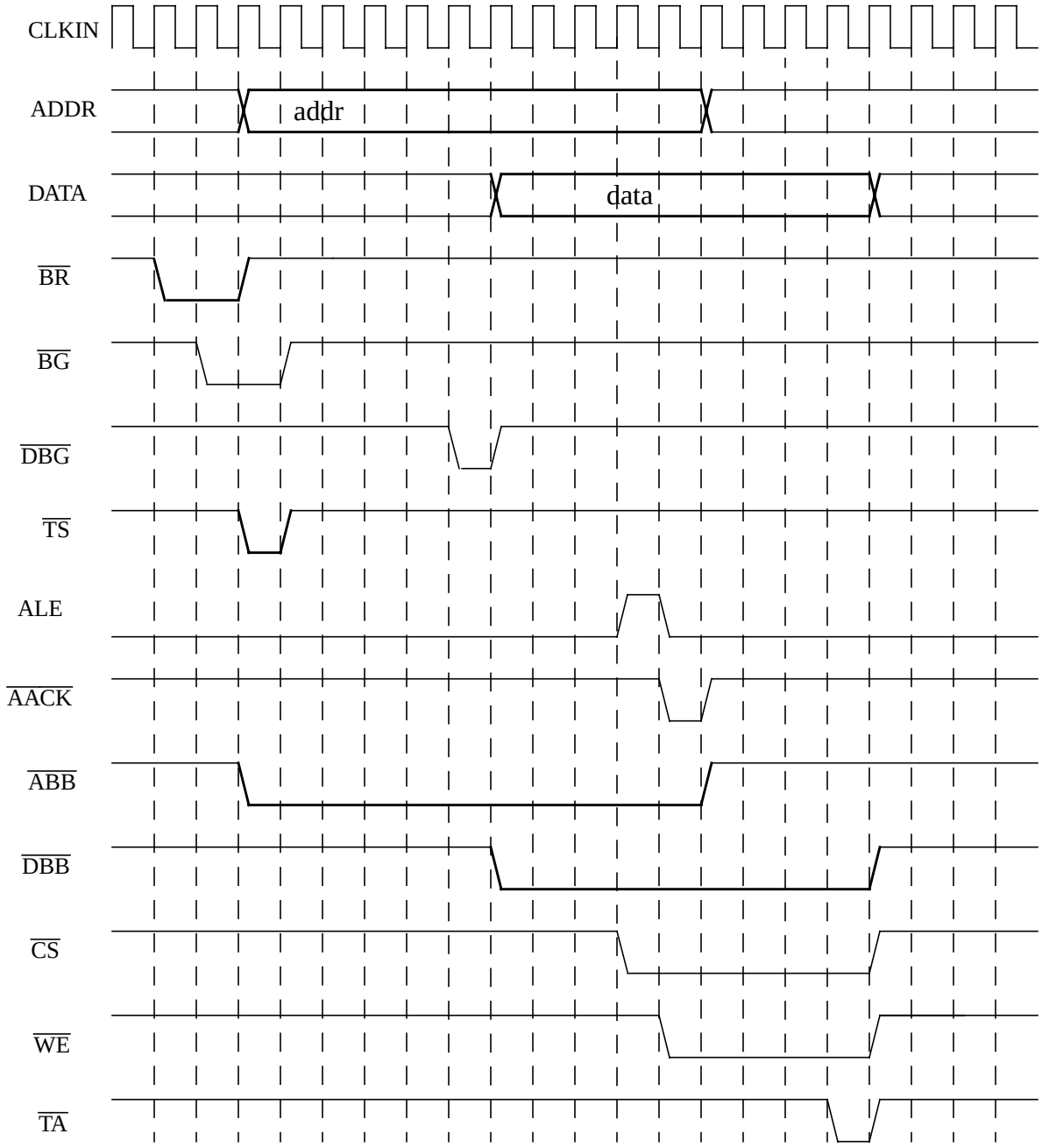

Figure 1 60x bus write to 60x memory

Notes: All the thick-lined signals are driven by external 60x master.

1.2 External 60x Master 60x Reads from Memory(GPCM) on 60x Bus

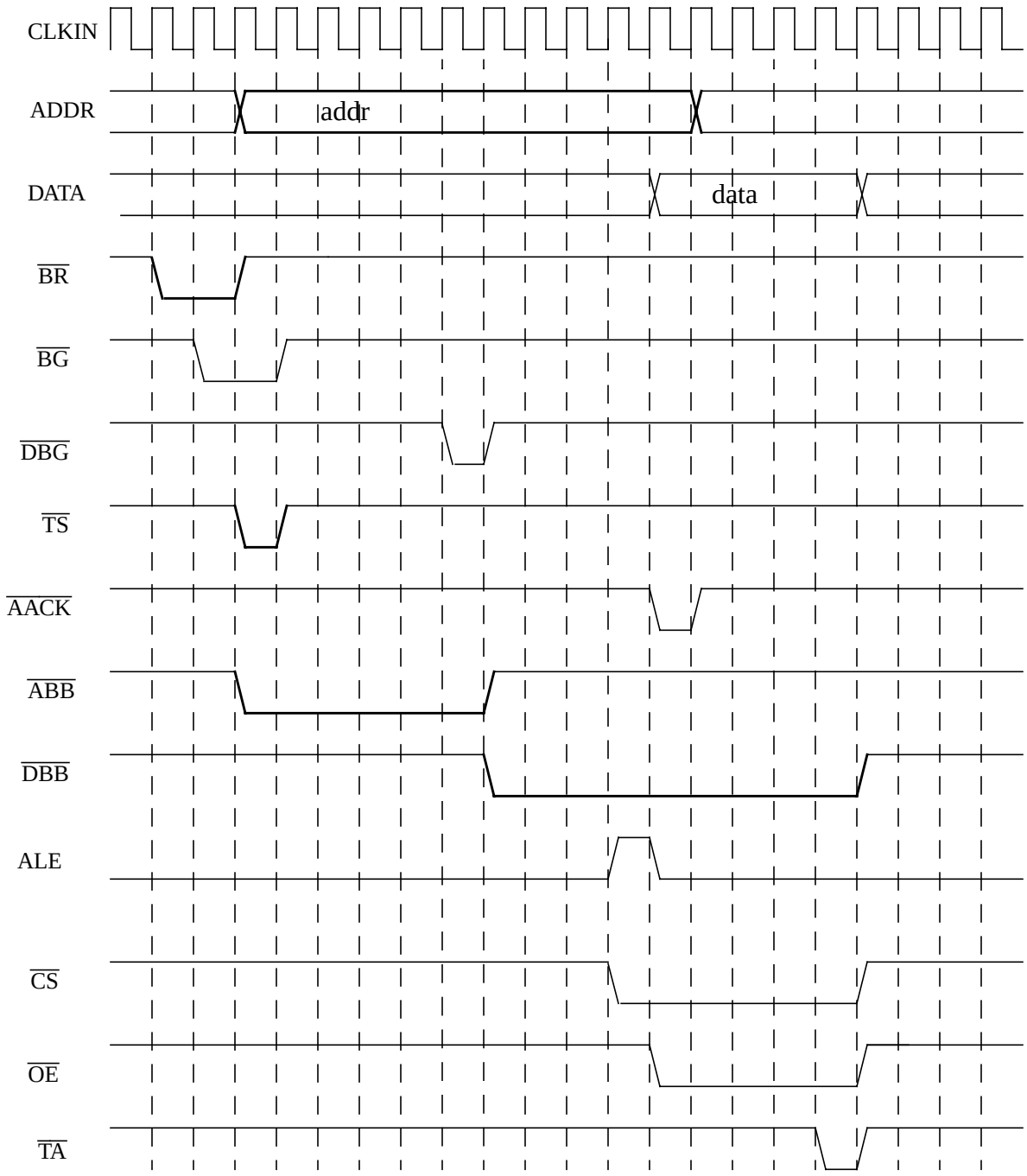

Figure 2 60x bus read from 60x memory (GPCM)

Notes: All the thick-lined signals are driven by external 60x master.

1.3 External 60x Master Reads from Internal dual-port RAM

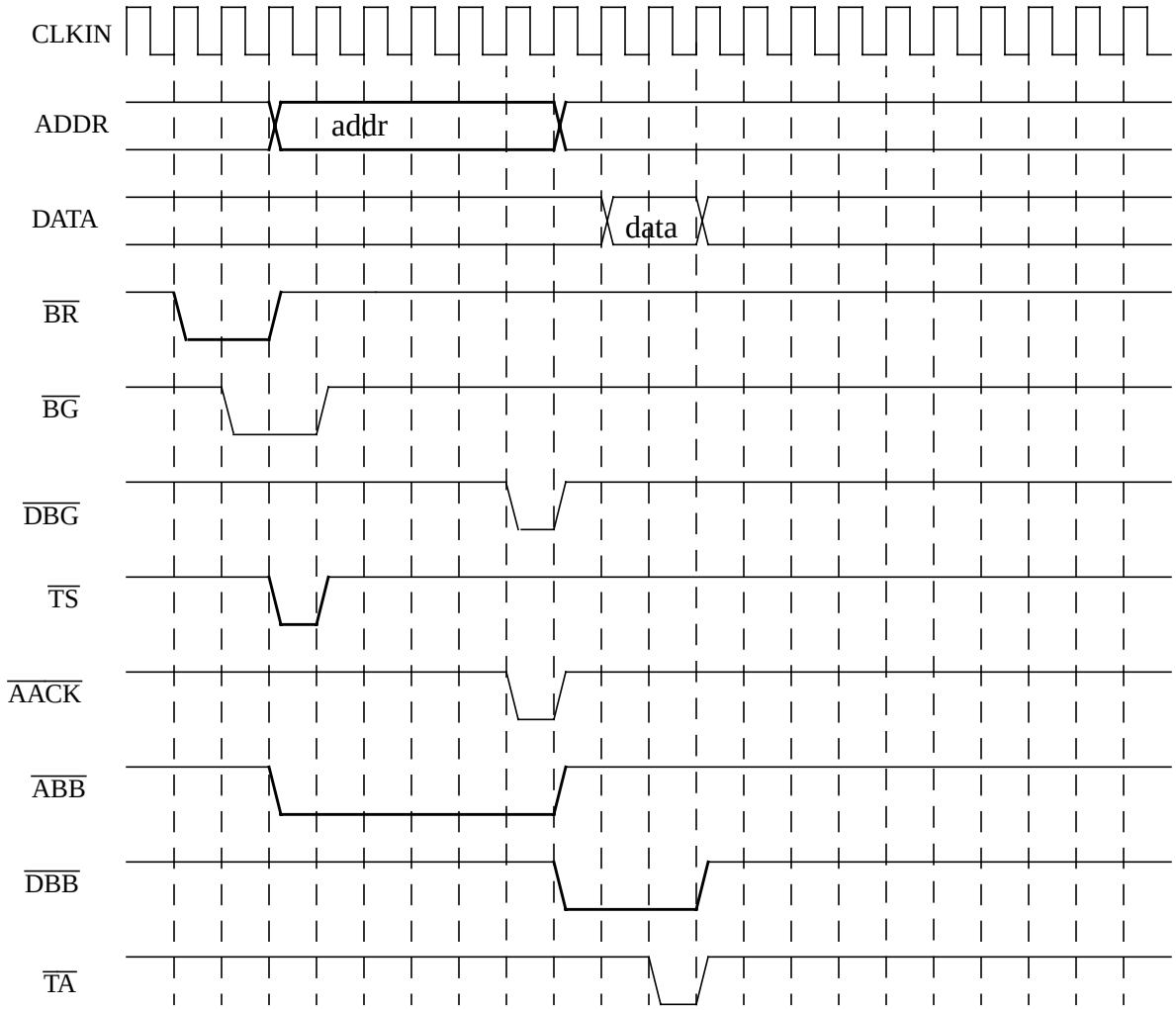

Figure 3 60x bus read from internal dual-port RAM

Notes: All the thick-lined signals are driven by external 60x master.

1.4 External 60x Master writes to internal dual-port RAM

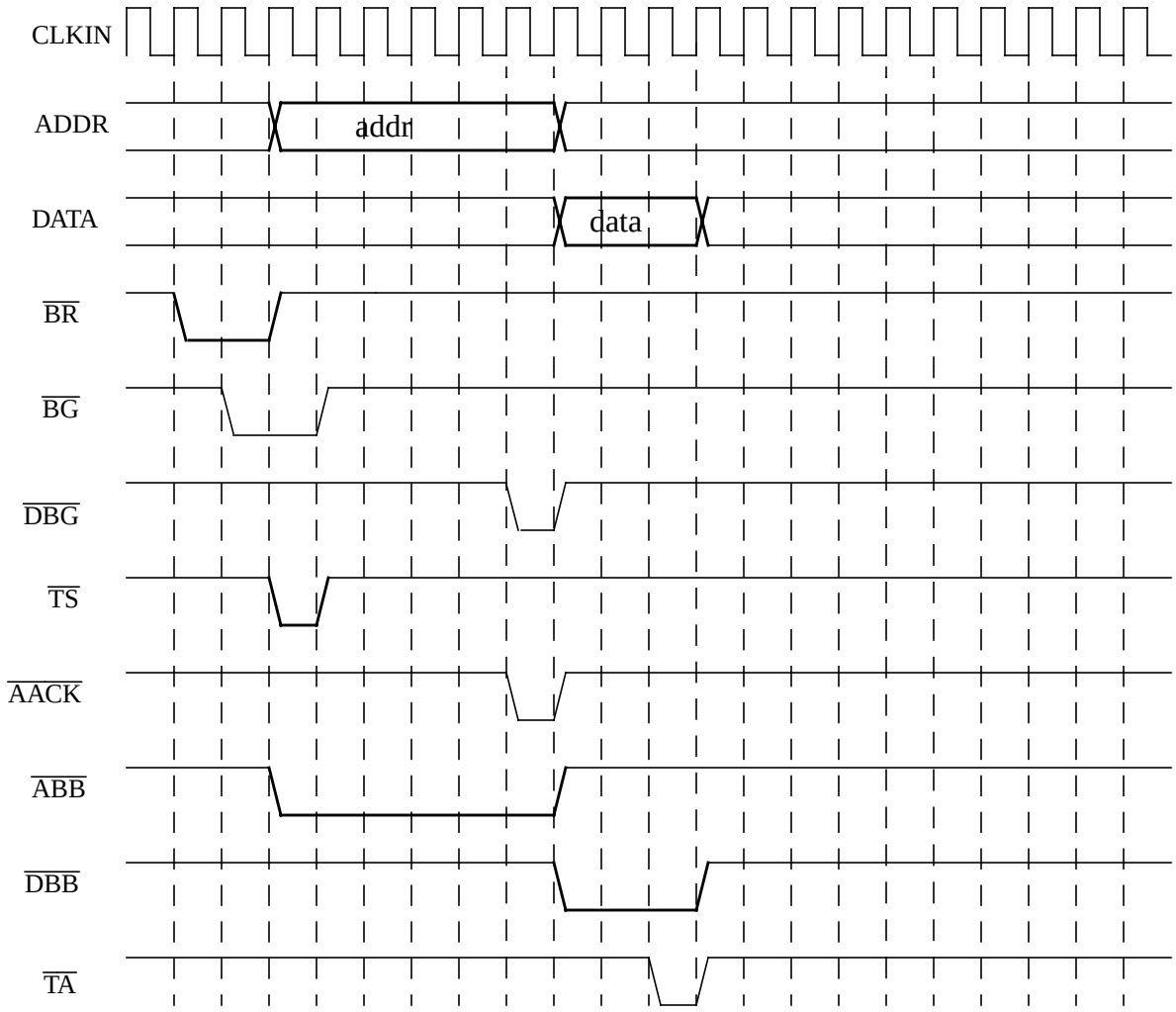

Figure 4 60x bus write to internal dual-port RAM

Notes: All the thick-lined signals are driven by external 60x master.

1.5 External 60x Master Writes to Memory (GPCM) on Local Bus

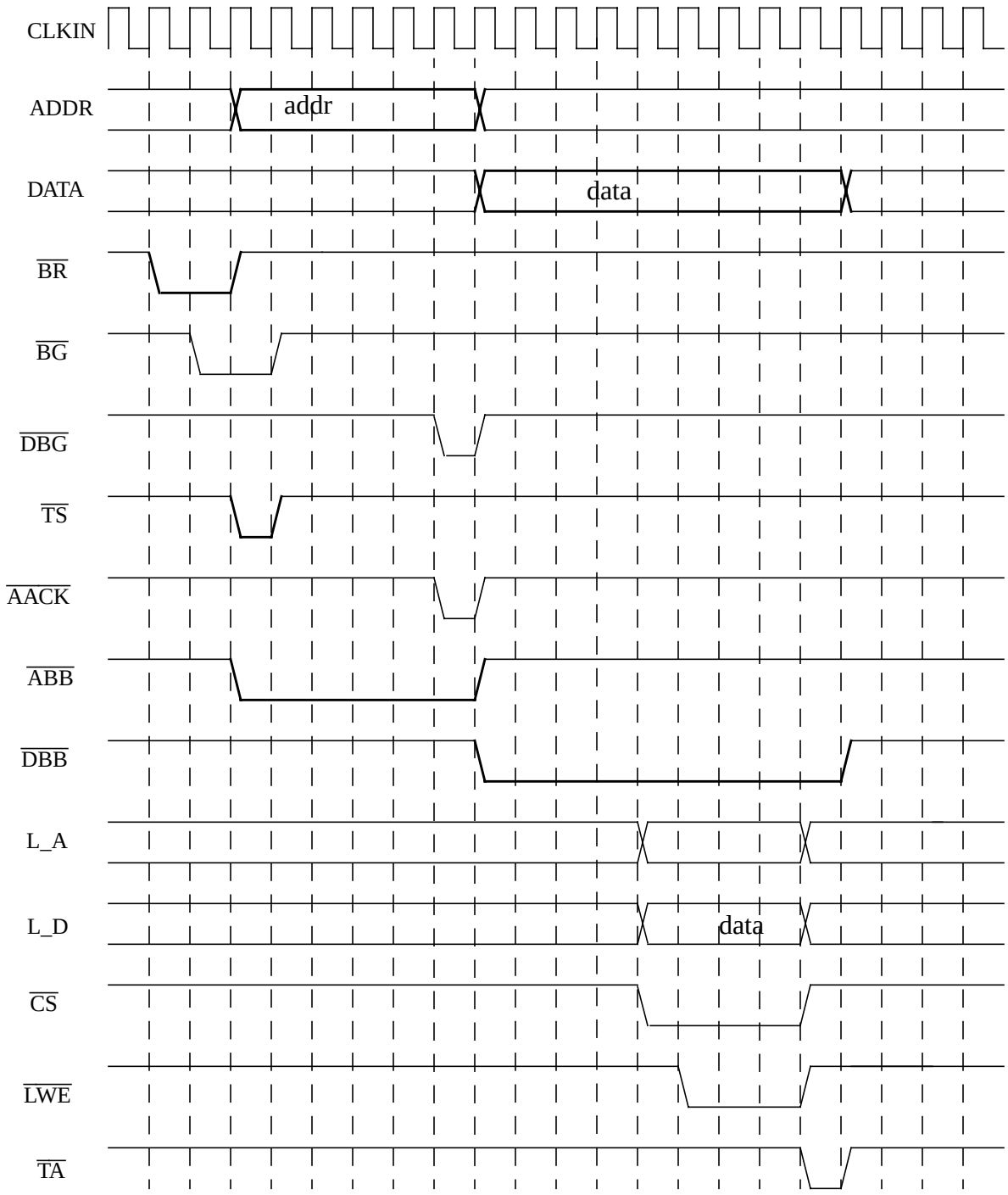

Figure 5 60x bus write to local bus

Notes: All the thick-lined signals are driven by external 60x master.

1.6 External 60x Master Reads from Memory(GPCM) on Local Bus

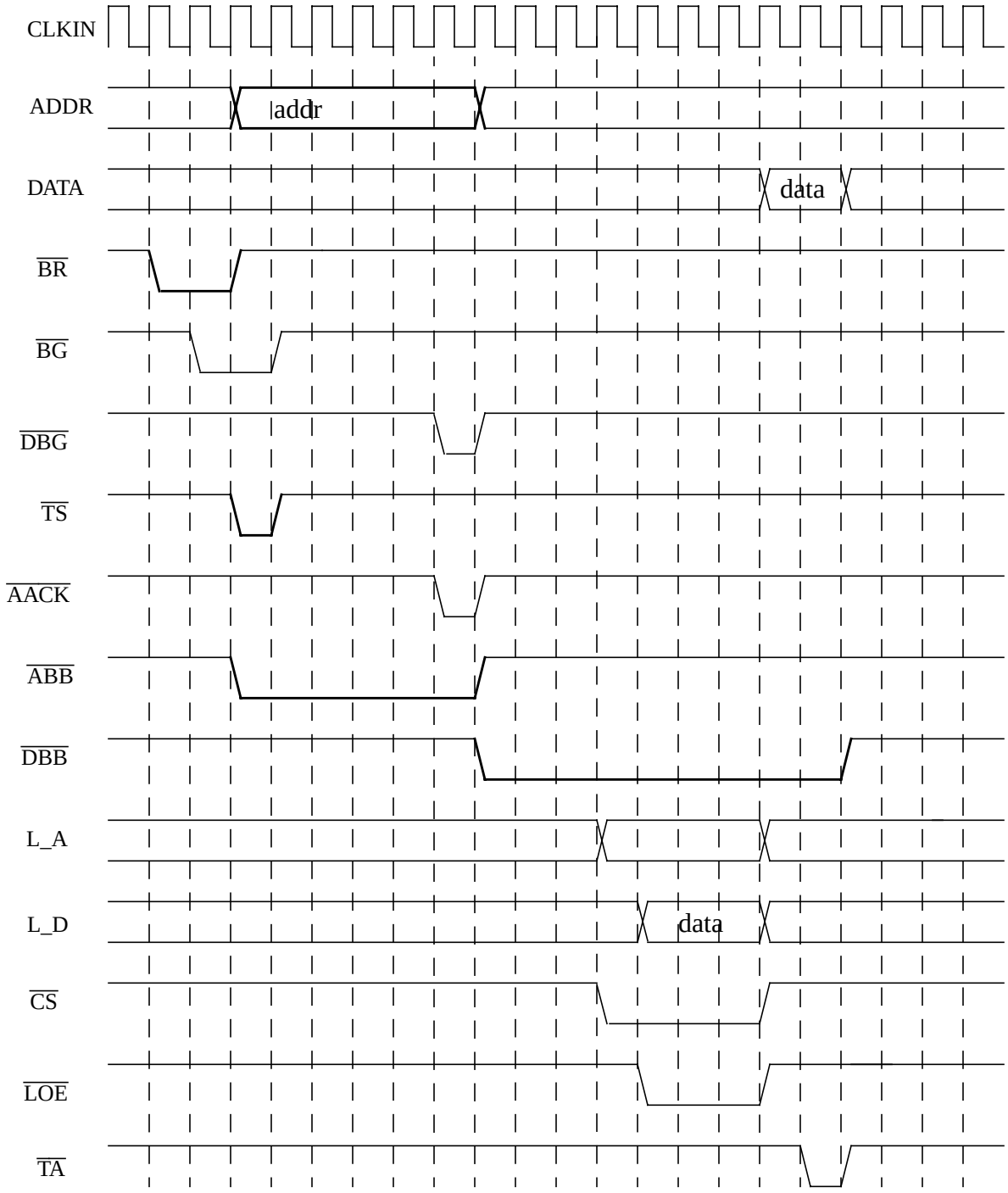

Figure 6 60x bus read from local bus

Notes: All the thick-lined signals are driven by external 60x master.

1.7 External 60x Master Writes to 60x Memory (GPCM) with Read-Modify-Write Cycle

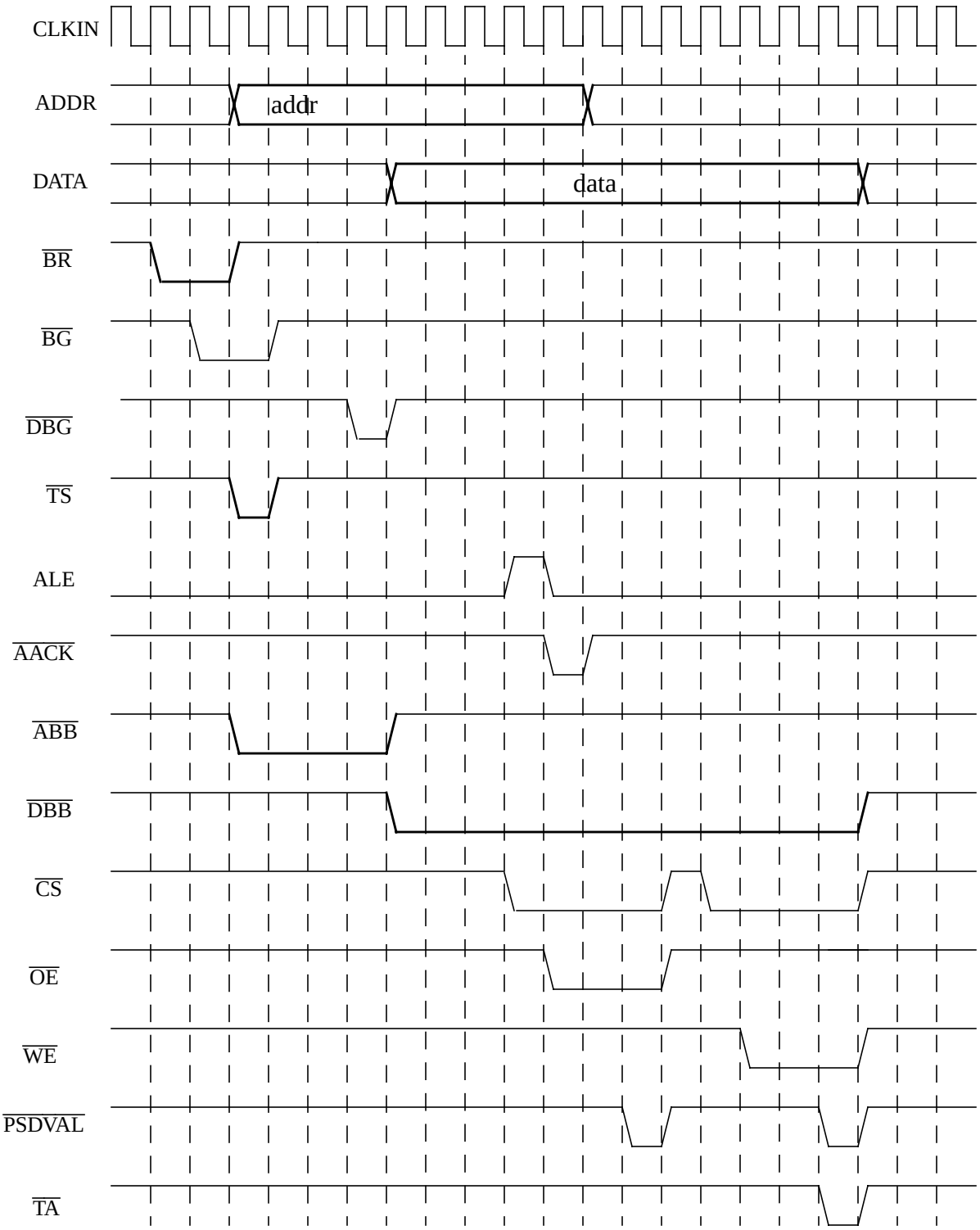

Figure 7 60x bus master write to 60x memory with Read-Modify-Write Cycle

Notes: All the thick-lined signals are driven by external 60x master.

1.8 External 60x Master Writes to Local Memory (GPCM) with Read-Modify-Write Cycle

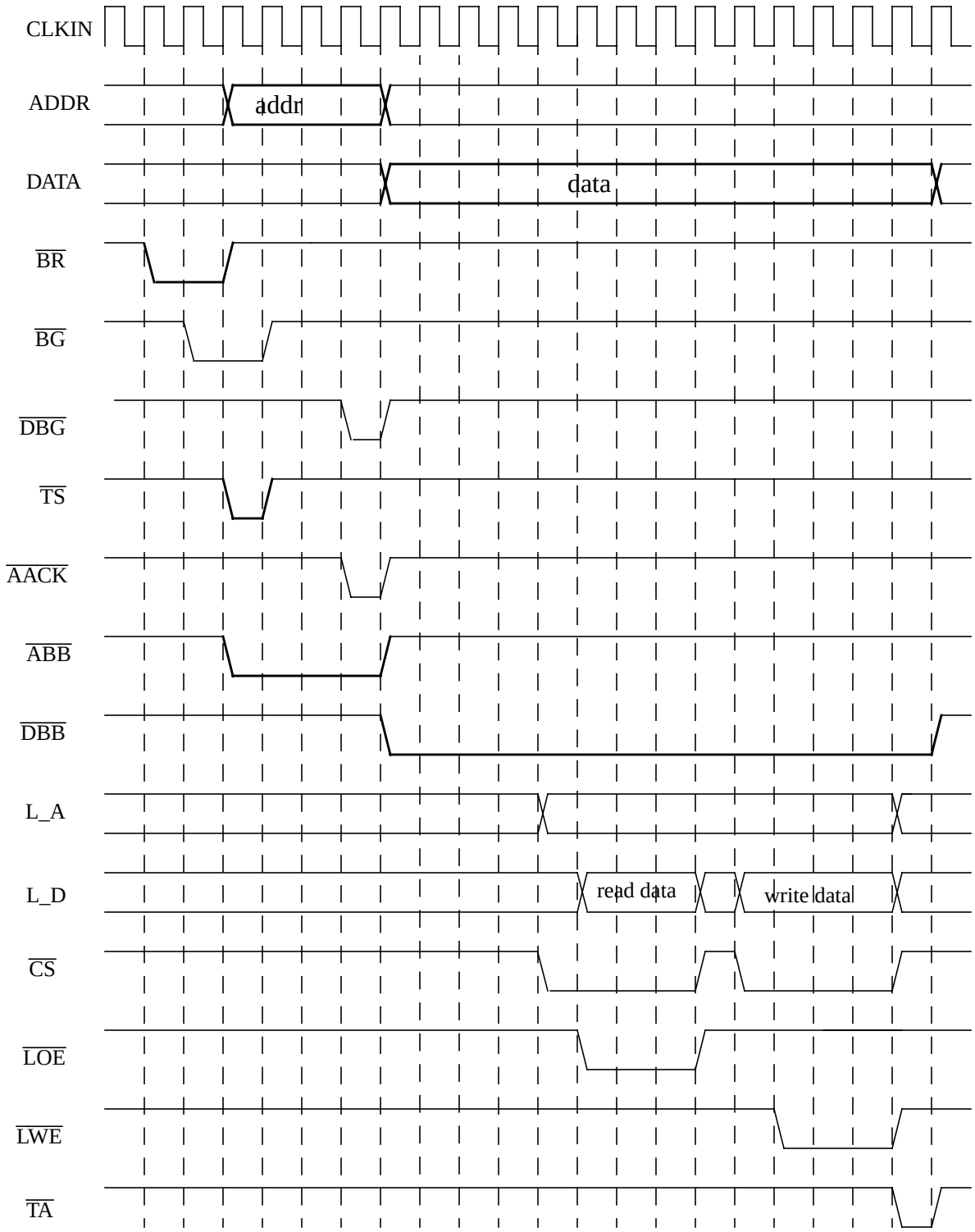

Figure 8 60x bus write to local bus with Read-Modify-Write Cycle

Notes: All the thick-lined signals are driven by external 60x master.

1.9 $\overline{\text{ARTRY}}$ Cycle during External 60x Master Access

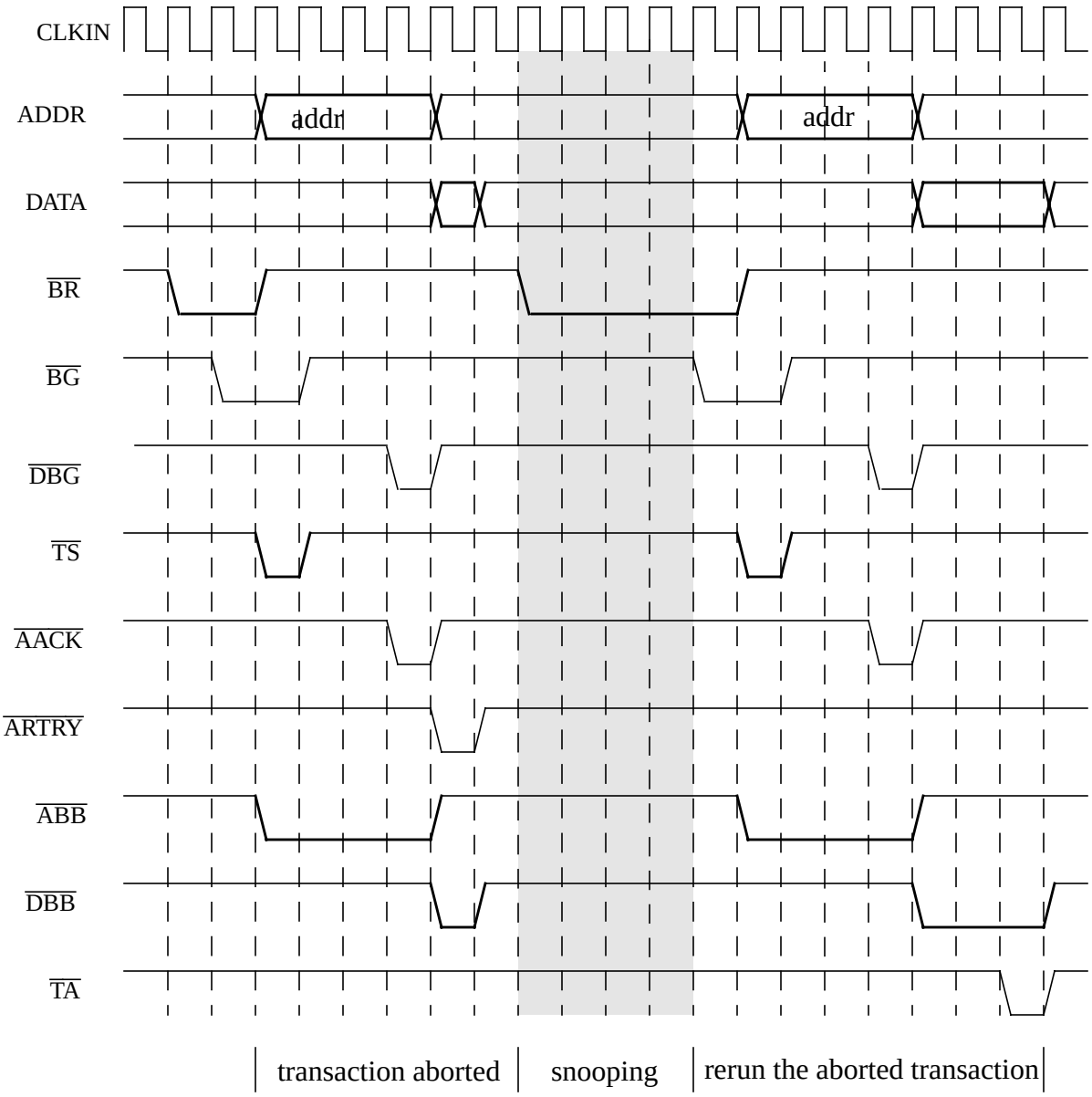

Figure 9 $\overline{\text{ARTRY}}$ cycle during external 60x master access

Notes: All the thick-lined signals are driven by external 60x master.

1.10 $\overline{\text{TEA}}$ Termination during External 60x Master Access

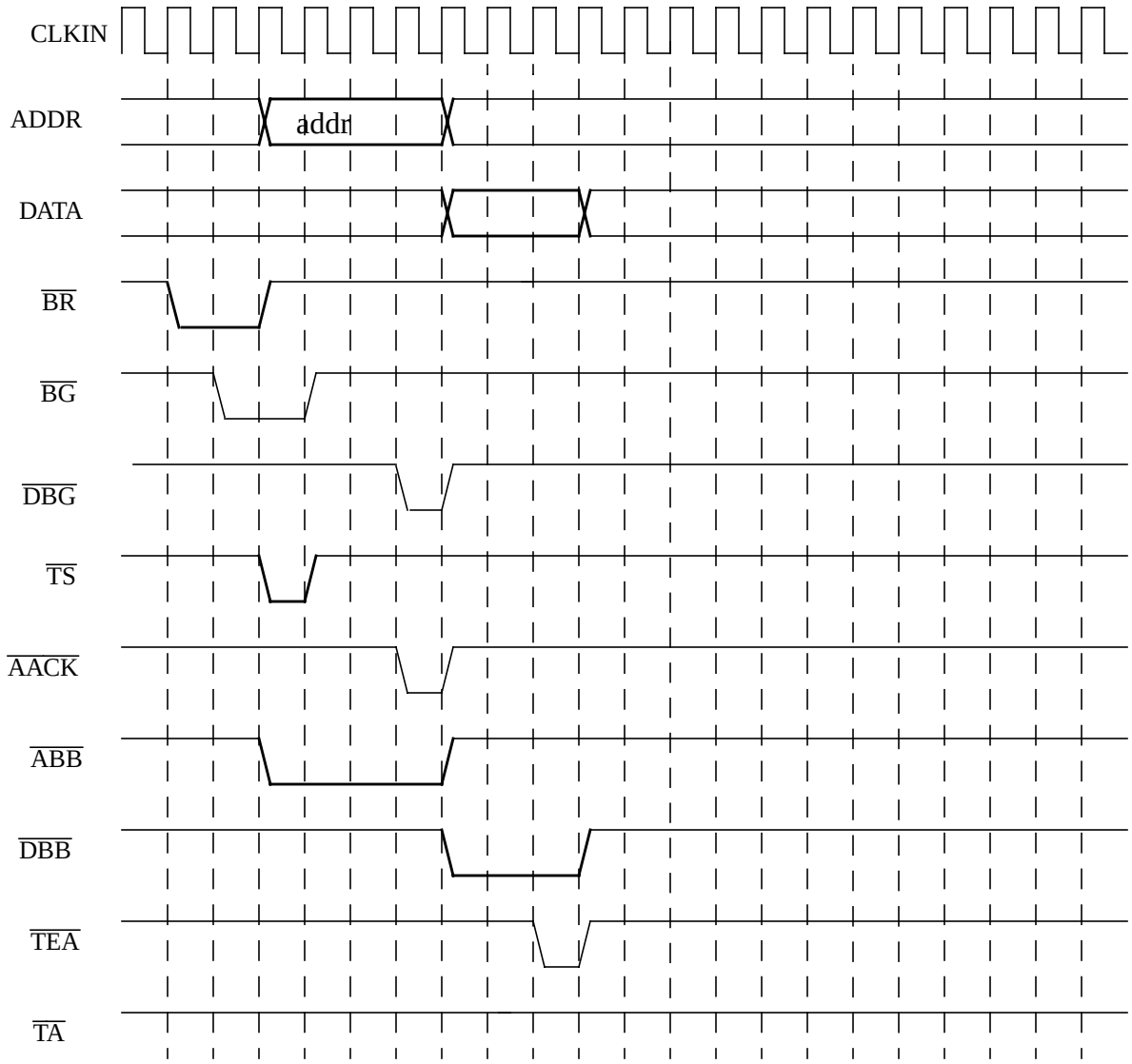

Figure 10 $\overline{\text{TEA}}$ termination during external 60x master access

All the thick-lined signals are driven by external 60x master.

Note:

If the external 60x master initiates a transaction not supported by MPC8260, the MPC8260 signals an error by asserting $\overline{\text{TEA}}$.

1.11 Pipeline Control -- Cycle with Pipeline

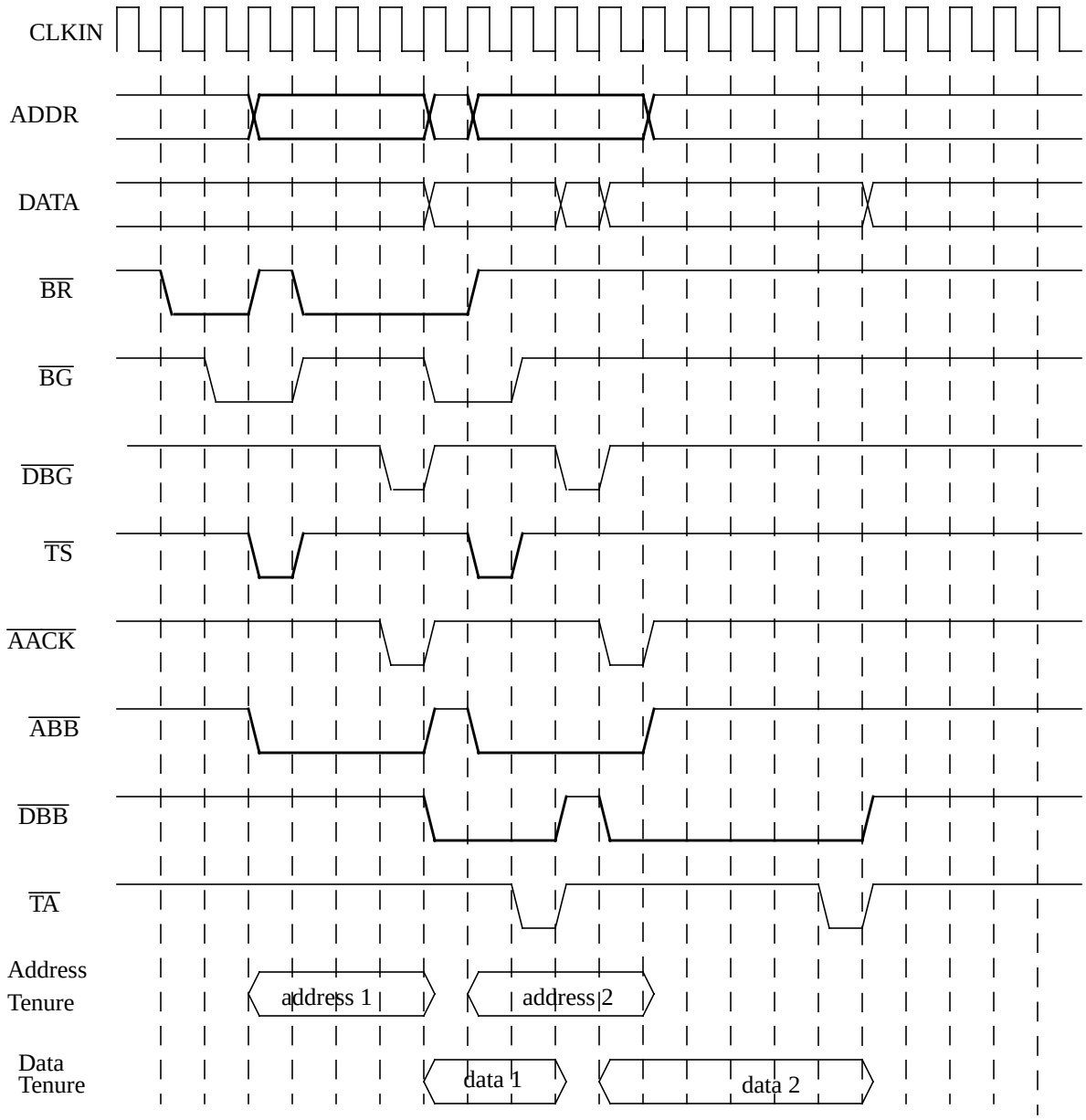

Figure 11. 60x Master Cycle with Pipeline

Note:

1. The pipeline depth is controlled by BCR[PLDP]:
   PLDP = 1: Depth is 0
   PLDP = 0: Depth is 1

2. With the pipeline depth equals to 1, the second address tenure starts before the end of the first data tenure.

1.12 Pipeline Control -- Cycle without Pipeline

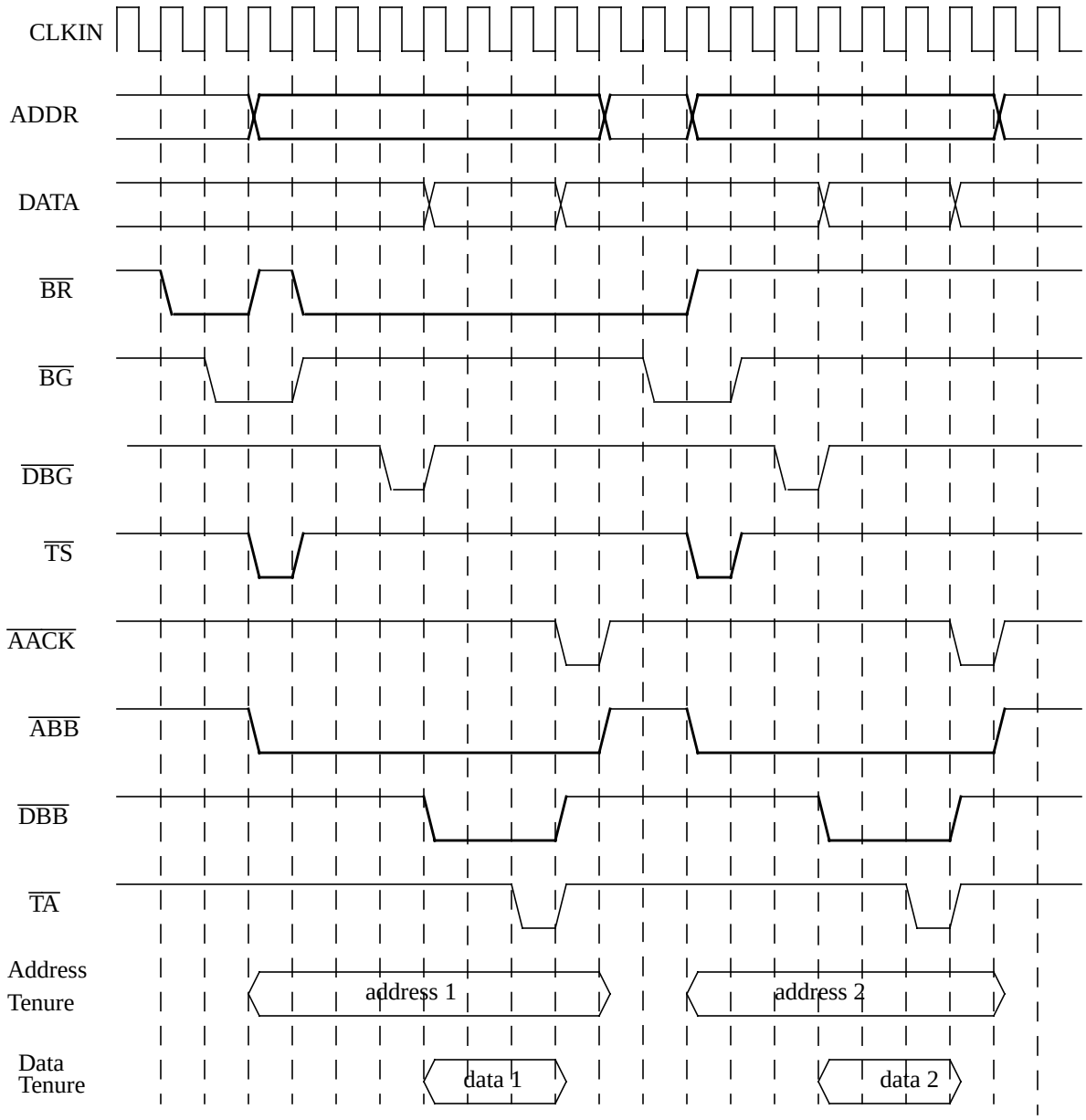

Figure 12. 60x Master Cycle without Pipeline

Note:

1. The pipeline depth is controlled by BCR[PLDP]:
   PLDP = 1: Depth is 0
   PLDP = 0: Depth is 1

2. With the pipeline depth equals to 0, the second address tenure starts after the end of the first bus tenure. Also for each bus transaction, the address tenure ends one cycle after its own data tenure finishes.

2. External Slave Transaction

2.1 Simple Read from 60x slave

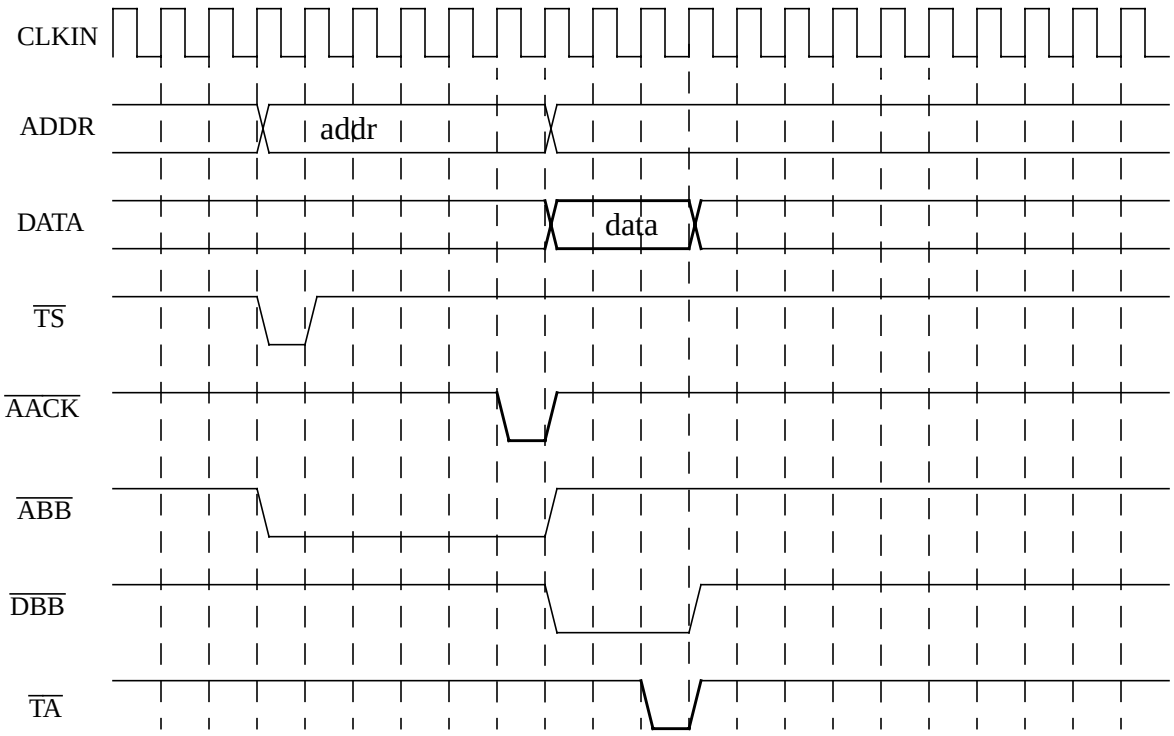

Figure 13 Simple read from 60x slave

Notes: All the thick-lined signals are driven by external 60x slave.

2.2 Simple Write to 60x slave

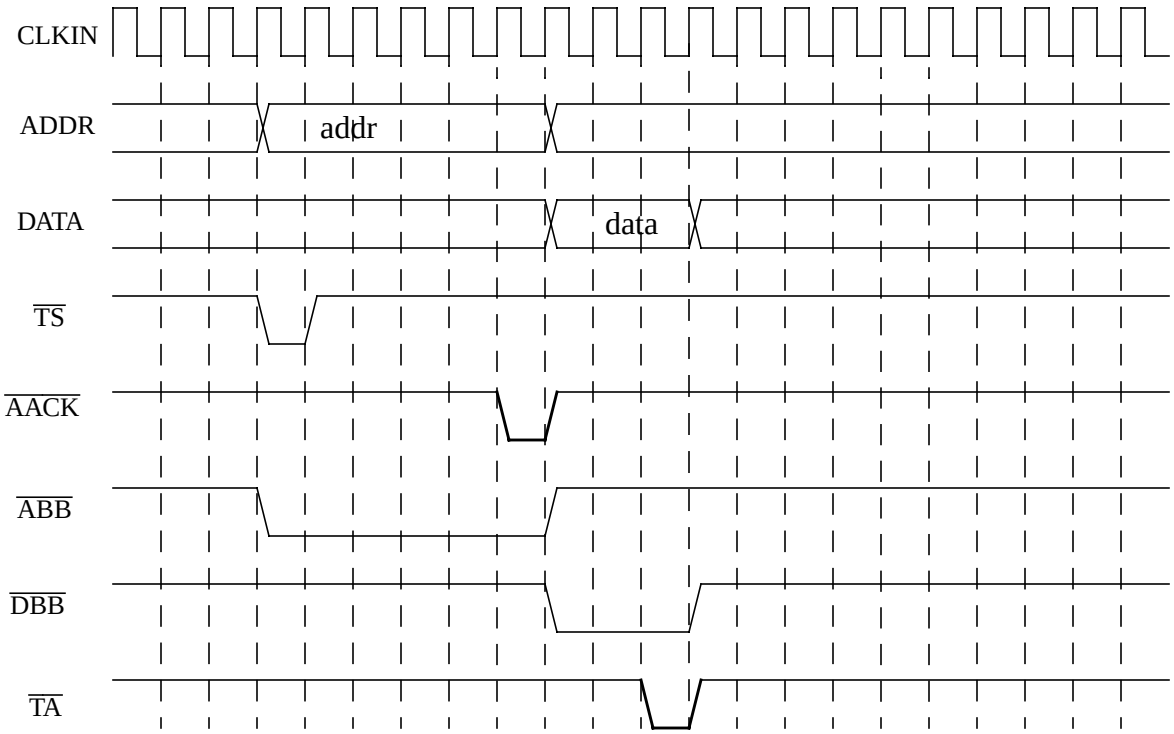

Figure 14 Simple write to 60x slave

Notes: All the thick-lined signals are driven by external 60x slave.

2.3 $\overline{\text{ARTRY}}$ Cycle during 60x Slave Transaction

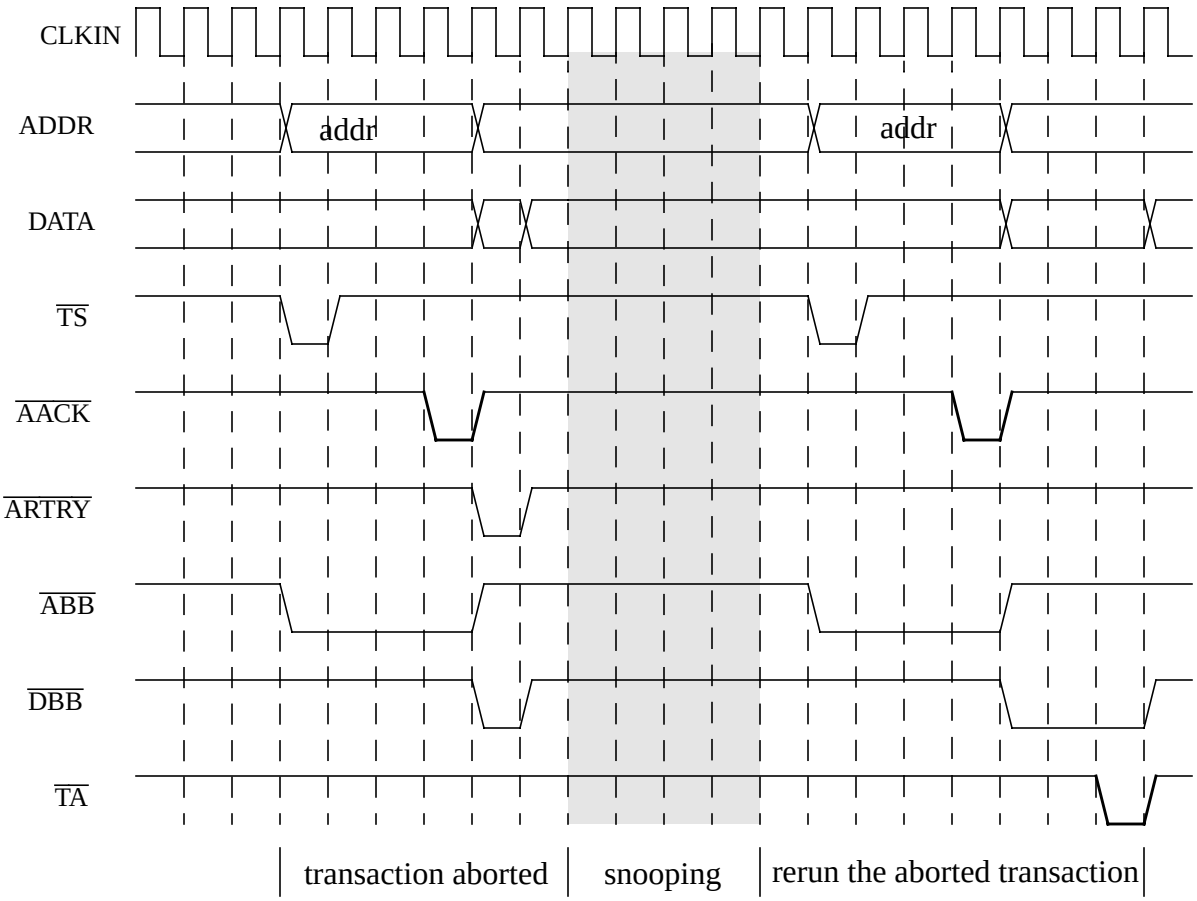

Figure 15 $\overline{\text{ARTRY}}$ cycle during 60x Slave Transaction

Notes: All the thick-lined signals are driven by external 60x slave.

2.4 $\overline{\text{TEA}}$ Termination during External 60x Slave Access

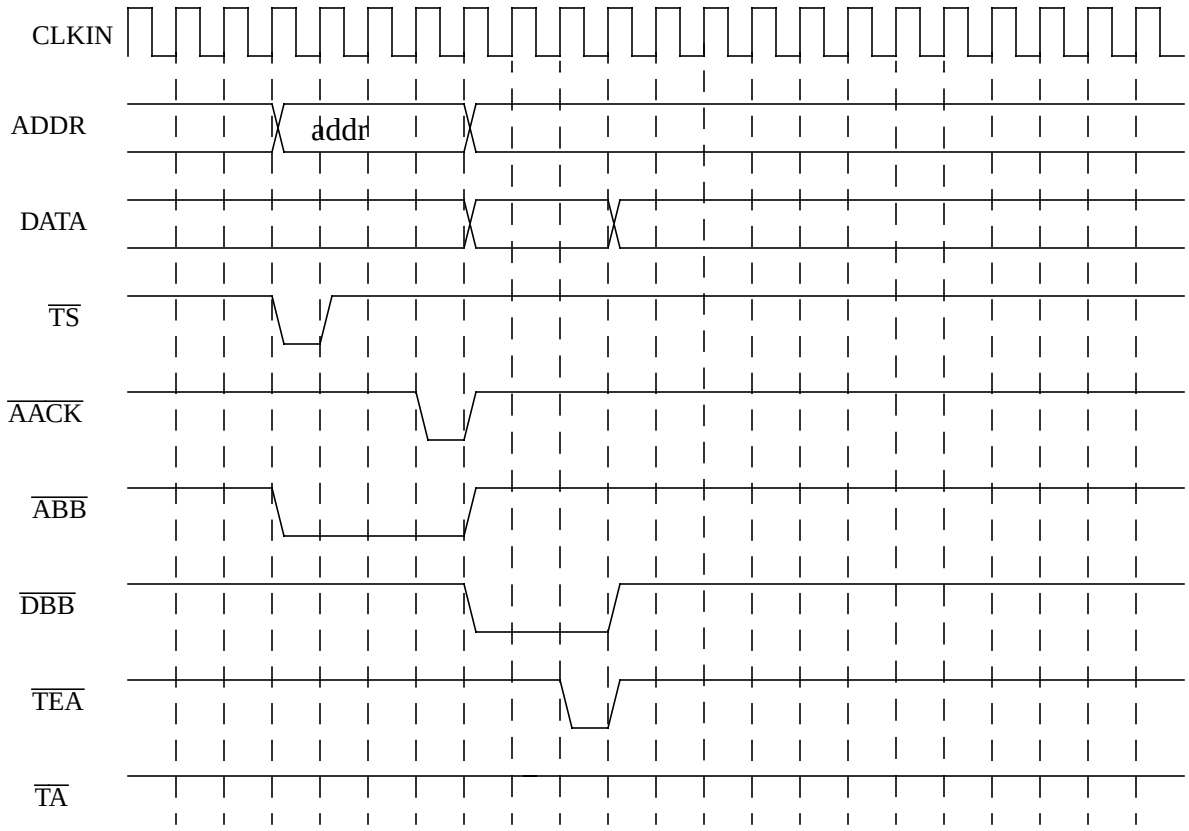

Figure 16 $\overline{\text{TEA}}$ termination during external 60x Slave access

Note:

If the external 60x slave detects a bus error, it may assert $\overline{\text{TEA}}$ to inform MPC8260 during data tenure.

2.5 Pipeline Control -- Cycle with Pipeline

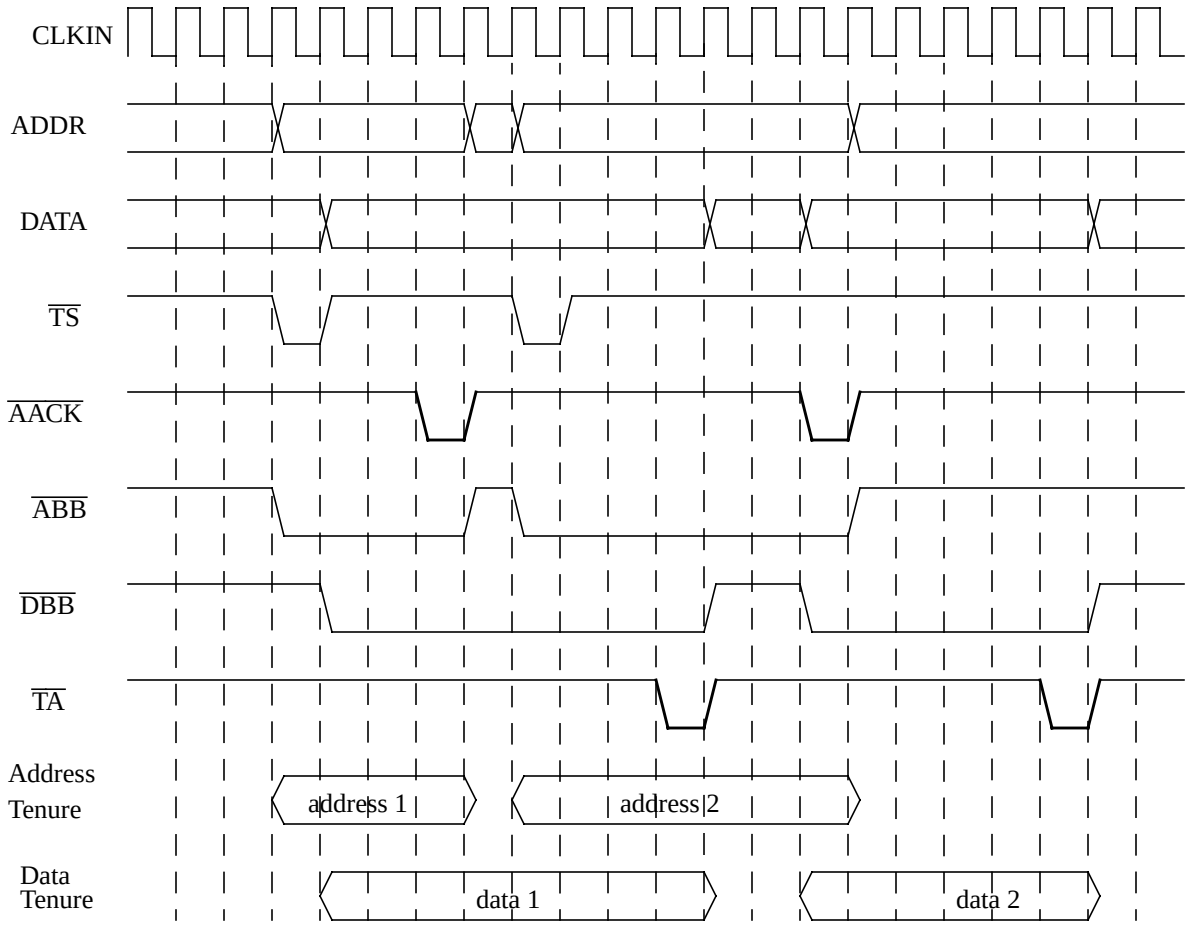

Figure 17 Cycle with Pipeline

Note:

1. The pipeline depth is controlled by BCR[PLDP]:

   PLDP = 1: Depth is 0
   PLDP = 0: Depth is 1

2. With the pipeline depth equals to 1, the second address tenure starts before the end of the first data tenure.

2.6 Pipeline Control -- Cycle without Pipeline

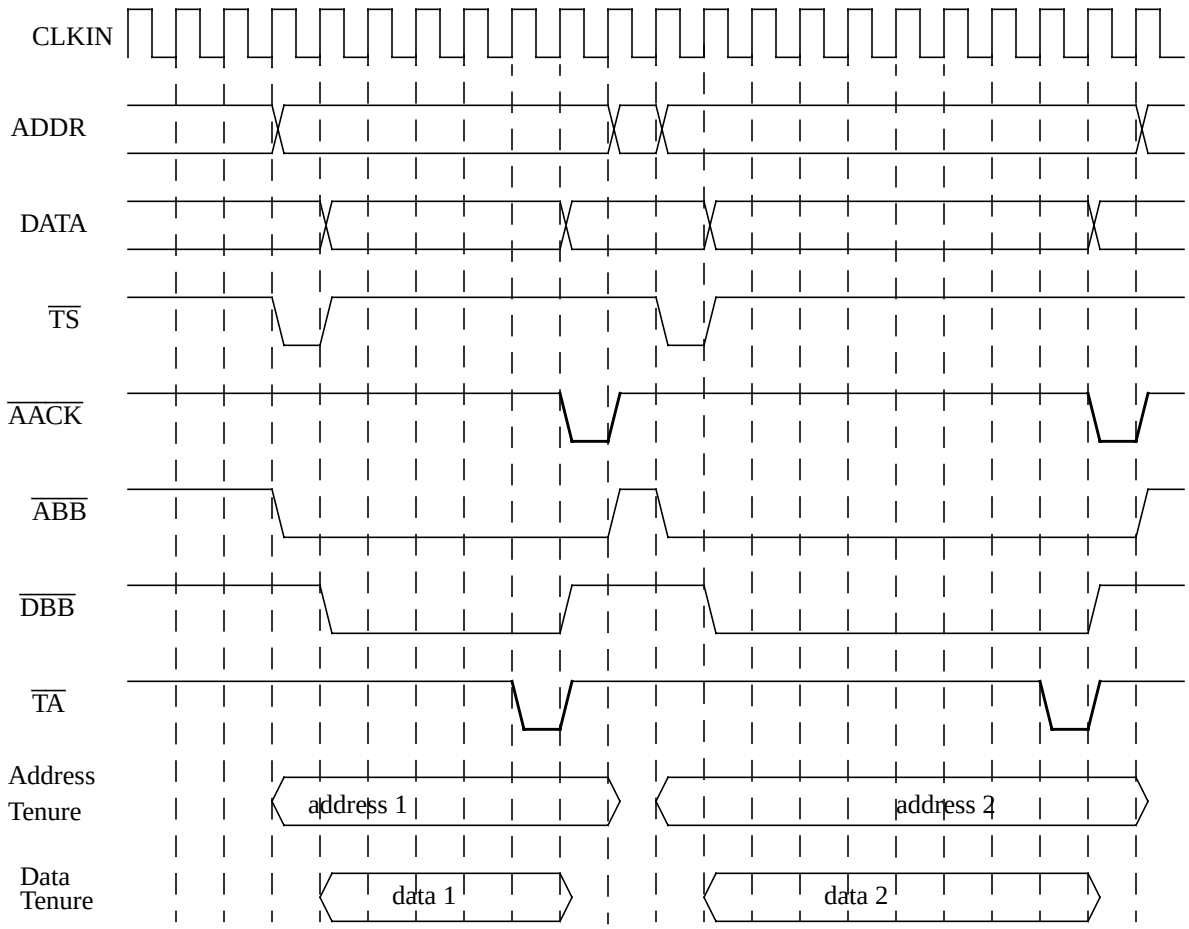

Figure 18 Cycle without Pipeline

Note:

1. The pipeline depth is controlled by BCR[PLDP]:

   PLDP = 1: Depth is 0
   PLDP = 0: Depth is 1

2. With the pipeline depth equals to 0, the second address tenure starts after the end of the first bus tenure. Also for each bus transaction, the address tenure ends one cycle after its own data tenure finishes.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com