AN2348
Rev. 1.5 9/2003

Migrating from the MPC860 to the MPC866 PowerQUICC™

This application note lists some of the design considerations that a customer must make when migrating from the MPC860/855T 'CDR2' family to the MPC866/859T 'HiP6W' family.

This application note covers the following topics:

1 Overview

The MPC866 family of processors is a member of the MPC8xx PowerQUICC™ family. The MPC866 family is a PowerPC™ derivative of Freescale's Quad Integrated Communications Controller (PowerQUICC). In addition to the standard MPC860 family capability, the MPC866/859T family of products provide the following "Enhanced SAR" (ESAR) features:

- Full AAL5, AAL2, and AAL0 support
- ATM Pace Controller (APC)
- Transmission Convergence (TC) sub-layer for E1/T1, xDSL and VBR, support
- Simultaneous Fast Ethernet (MII) and UTOPIA (ATM) operation
- Utopia MultiPHY Level II support
- Utopia port-to-port switching and a number of other key networking features

For more details, refer to the MPC866/859T Technical Summary.

Particular features make the MPC866 a very adaptable ATM ESAR controller that can be used for a variety of ATM applications:

- Line card controllers
- ATM to WAN interworking (frame relay, T1/E1 circuit emulation, xDSL applications)
- ATM25 applications
- Residential broadband network interface units (ATM-to-Ethernet)
- High performance set-top controller
- Bridging and routing applications

This application note describes the hardware and software design considerations when migrating from MPC860/855T to MPC866/859T. The MPC866 is the latest development of the MPC862/857T family of products. The MPC866/859T uses the HIP6W (0.18µm) technology, which enables the MPC866/859T to achieve higher performance with system frequencies up to 133 MHz.

The MPC866/859T family is designed to keep the same functionality as the MPC860/855T, including micro-code implementation. The MPC866 is an enhanced version of the MPC860SAR. Although the MPC866 is pin-compatible with both the MPC860 and MPC860SAR, a number of small but significant programming changes must be made to accommodate differences between the controllers.

The MPC859T is a low-cost derivative of the MPC866. It includes the same basic feature set, but only one serial communication controller (SCC) is available to the user. Before selecting the MPC859T as the host processor, carefully consider whether one SCC can provide enough performance for the target application.

The MPC866/859T PLL circuitry received a major design overhaul, that is, hardware and software need modification when changing from an 860/855T based design so that they support the high CPU frequency. Section 10, “Clocks and Power Control,” discusses the clocks and the DPLL operation.

This application note refers to the *MPC862 PowerQUICC™ User’s Manual*, the *MPC866 PowerQUICC™ Family User’s Manual*, and the *MPC860 PowerQUICC™ User’s Manual*.

2 System and External Bus Frequency Operation

The MPC866/859T Family operates at a maximum system frequency of 133 MHz and an external bus frequency of 66 MHz. Table 1 shows the maximum operating frequency operation and external bus frequency for both the MPC860/855T and MPC866/859T.

Table 1. Maximum Operating Frequency

	MPC860/855T		MPC866/859T		MPC859DSL	
	1:1 Mode	2:1 Mode	1:1 Mode	2:1 Mode	1:1 Mode	2:1 Mode
Maximum System Frequency Operation	66	80	66	133	66	66
Maximum External Bus Frequency Operation	66	40	66	66	66	33

To achieve the best performance, minimize the capacitive loading for the MPC866/859T external bus as much as possible. Freescale recommends connecting the SDRAM directly to the external bus while isolating and buffering slow access devices such as FLASH and DRAM on the external bus. Use devices such as data transceivers to help remove extra capacitance on the bus.

NOTE

New system frequencies are supported in MPC866. Be careful when reusing previous MPC860 drivers that use baud generator clocks (BRGCs). For example, BRG clock dividers should be readjusted to generate the desired baud when operating at frequencies higher than 80 MHz.

3 New PLL Implementation

The MPC866/859T implements a new Digital Phase Lock Loop (DPLL) block that eliminates the need for an XFC capacitor. The XFC pin is a No Connect (NC) on the MPC866/859T. The XFC pin is not connected internally. Table 2 lists the related pins for the PLL and clock block.

Table 2. DPLL Considerations

Pin Name	MPC860/855T	MPC866/859T
XFC	XFC Capacitor	No Connect
EXTCLK	EXTCLK	EXTCLK
XTAL	XTAL	XTAL
EXTAL	EXTAL	EXTAL
CLKOUT	CLKOUT	CLKOUT

The following list includes major changes in the clock and DPLL implementation:

- The input clock can be only a 10-MHz crystal at EXTAL/XTAL and 10 MHz or higher at EXTCLK.
- The power-on reset DPLL configuration default value has changed.
- The low-power and reset control register (PLPRCR) controls the system frequency. This register now has several different fields (MFN, MFD, MFI and PDF) for the frequency factor calculation. This register is not backwards-compatible with the MPC860/855T.

For more details on the clock and DPLL programming module, please refer to Section 10, “Clocks and Power Control” on page 9.

4 Power Voltage Structure

The MPC866 has two voltage levels for the power-supply connection. The internal logic and the DPLL block are fed by 1.8 V (V_{DDL} and V_{DDSYNC} respectively), while the I/O buffers are supplied by 3.3 V (V_{DDH}).

The keep alive power (KAPWR) power pin is not available on the MPC866/859T and was replaced as an additional V_{DDL} power pin.

Table 3 highlights the power supply voltage levels for each of the power pins.

Table 3. Power Supply Connection

Pin Name	MPC860	MPC866/859T
VDDH	3.3 V	3.3 V
VDDL	3.3 V	1.8 V

Table 3. Power Supply Connection

Pin Name	MPC860	MPC866/859T
VDDSYN	3.3 V	1.8 V
KAPWR	KAPWR	1.8 V
VSS	Ground	Ground
VSSSYN1	Ground	Ground
VSSSYN2	Ground	Ground

The organization of the power rails is shown in Figure 1. Note that the clock control and digital DPLL blocks are now powered by V_{DDL} on the MPC866/859T instead of V_{DDH} on the MPC860/855T. Also note that the low-power (sleep, doze, and power-down) modes are not supported.

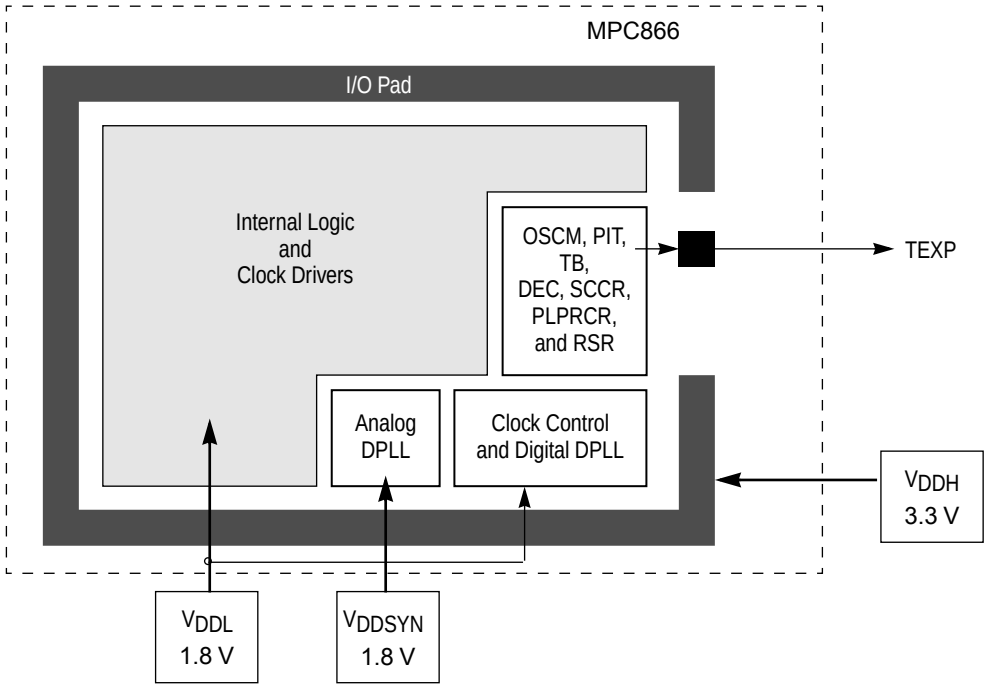


Figure 1. Organization of the Power Rails

5 Five-Volt Tolerant Pins

With the exception of the EXTAL and EXTCLK pins, the MPC860/855T pins are all 5-V tolerant. The MPC866/859T differs from the MPC860/855T concerning the pins that are 5-V tolerant. Table 4 lists all the pins on the MPC860/855T and MPC866/859T and states whether the pins are 5-V tolerant.

Table 4. List of the 5-V Tolerant Pins on the 860/855T and 866/859T

Pin Name	MPC860/855T 5-V Tolerant	MPC866/859T 5-V Tolerant
XTAL	No	No
EXTAL	No	No
EXTCLK	No	No
PB[14:31]	Yes	Yes
PA[0:15]	Yes	Yes
PC[4:15]	Yes	Yes
PD[3:15]	Yes	Yes
TDI	Yes	Yes
TDO	Yes	Yes
TCK	Yes	Yes
TRST	Yes	Yes
TMS	Yes	Yes
MII_MDIO	Yes	Yes
MII_TXEN	Yes	Yes
Remainder of 860/866 pins	Yes	No

6 Pinout Description

Figure 2 shows the MPC866/859T pinout. The following list notes the changes:

- All V_{DDL} pins and V_{DDSYNC} (shown in blue) were changed to 1.8-V pins on MPC866/859T.
- All V_{DDH} pins (shown in green) are still 3.3-V pins on MPC866/859T.
- Pin T2 (shown and labeled in red) was changed from XFC on the MPC860/855T to N/C on the MPC866/859T (see Table 5).
- Pin R1 (labeled in magenta) was changed from KAPWR on MPC860/855T to V_{DDL} on the MPC866/959T (see Table 5).
- All pins shown in brown are required for simultaneous operation of UTOPIA and MII operation on the MPC866/859T and are detailed in Table 6.
- All pins shown in orange are implemented in UTOPIA Multi-PHY operation on the MPC866/859T and are detailed in Table 7.

Table 5. Pin Changes from 860/855T Moving to 866/859T

Pin Name	Pin Number	MPC860/855T	MPC866/859T
XFC	T2	XFC	NC
KAPWR	R1	KAPWR	V_{DDL}

Table 6. Simultaneous MII and UTOPIA Pins

Pin No.	Pin Name	Pin No.	Pin Name
A3	CE2_A / MII-TXD3	U4	IP_A4 / UTPB_Aux4 / MII-RXCLK
B3	CE1_A / MII-TXD2	U5	IP_A5 / UTPB_Aux5 / MII-RX-ERR
K2	ALE_A / MII-TXD1	U15	PD[5] / REJECT2 / UTPB6 / MII-TXD3
L4	OP0 / MII-TXD0 / UtpClk_Aux	U16	PD[4] / REJECT3 / UTPB7/ MII-TXD2
R3	WAIT_A / SOC_Aux	U17	PD[15] / L1TSYNCA / UTPB0 / MII-RXD3
R16	PD[12] / L1RSYNCB / MII-MDC / UTPB3	V16	PD[6] / RTS4 / UTPB5 / MII-RXDV
T3	IP_A7 / UTPB_Aux7 / MII-RXDV	V17	PD[9] / RXD4 / UTPCLK / MII-TXD0
T4	IP_A1 / UTPB_Aux1 / MII-RXD2	V18	PD[13] / L1TSYNCB / UTPB2 / MII-RXD1
T5	IP_A0 / UTPB_Aux0 / MII-RXD3	V19	PD[14] / L1RSYNCA / UTPB1/ MII-RXD2
T6	IP_A6 / UTPB_Aux6 / MII-TX-ERR	W2	IP_A3 / UTPB_Aux3 / MII-RXD0
T16	PD[11] / RXD3 / MII-TX-ERR /RXENB	W17	PD[8] / TXD4 / MII-RX_CLK / MII-MDC
U3	IP_A2/IOIS16_A/UTPB_Aux2/MII-RXD1	W18	PD[10] / TXD3 / TXENB / MII-RXD0

Table 7. UTOPIA Level 2 Multi-PHY Pins

Pin No.	Pin Name	Pin No.	Pin Name
J16	PB[25]/SMTXD1/RXADDR3	L19	PB[22]/SMSYN2/SDACK2/TXADDR4
J18	PB[24]/SMRXD1/TXADDR3	N16	PB[16]/L1RQA/L1ST4/RXADDR0
K16	PB[21]/SMTXD2/L1CLKOB/TXADDR1	N17	PB[18]/L1ST2/RTS2/RXADDR4
K17	PB[23]/SMSYN1/SDACK1/TXADDR2	P18	PB[17]/L1RQB/L1ST3/RXADDR1
L16	PB[20]/SMRXD2/L1CLKOA/TXADDR0	U18	PB[14]/RSTRT1/RXADDR2

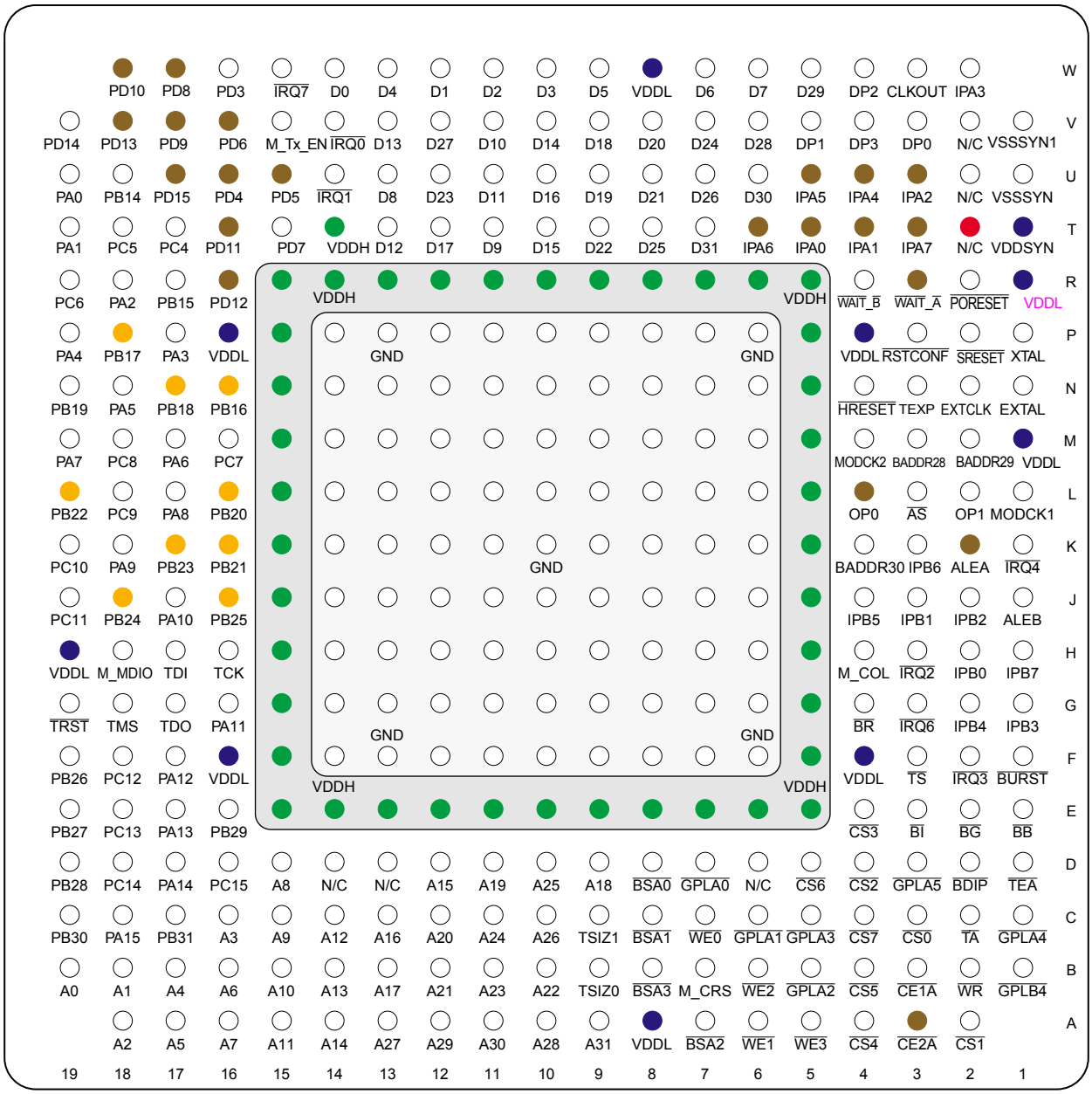


Figure 2. MPC866 Pinout

7 Microcode Status

Table 8 lists all the available protocols that can be implemented on the CPM ROM/RAM microcodes for the MPC860/855T and the MPC866/859T. The table also shows whether the patch is available as a RAM patch or is included in the ROM.

Table 8. MPC860/855T and MPC866/859T ROM-Based Microcodes

		MPC860/855T	MPC866/859T
	Mask (MOO #)	3K20A	3L90H
	Silicon revision	D.4	0.3
	Part No. IMMR[16:23]	0x05	0x08
	MSKNUM IMMR[24:31]	0x02	0x00
	ROM microcode revision no.	0x0000	0x0001
	Max microcode DPRAM space	8k	8k
SCC	Appletalk/Localtalk	Yes	Yes
	Asynchronous HDLA/IrdA	Yes	Yes
	AAL2	Yes (RAM) [1]	Yes
	ATM AAL0 & AAL5	Yes	Yes
	BISYNC	Yes	Yes
	Dynamic CLP and CNG marking	Yes (RAM) [1]	Yes
	Enhanced UBR	Yes (RAM) [1]	TBD
	Ethernet / IEEE 802.3	Yes	Yes
	HDLC	Yes	Yes
	Multi sub-channel [MSC]	Yes (RAM) [1]	TBD
	Port-to-port switching	Yes (RAM) [1]	Yes
	SS7	Yes (RAM) [1]	TBD
	Transparent	Yes	Yes
	UART	Yes	Yes
	RTP accelerator	Yes (RAM) [1]	TBD
SMC	GCI (ISDN)	Yes	Yes
	Transparent	Yes	Yes
	UART	Yes	Yes

[1] This microcode is RAM-based only.

8 Register Lock Mechanism

Except for the omission of the power-down feature, the operation of the register lock mechanism is unchanged.

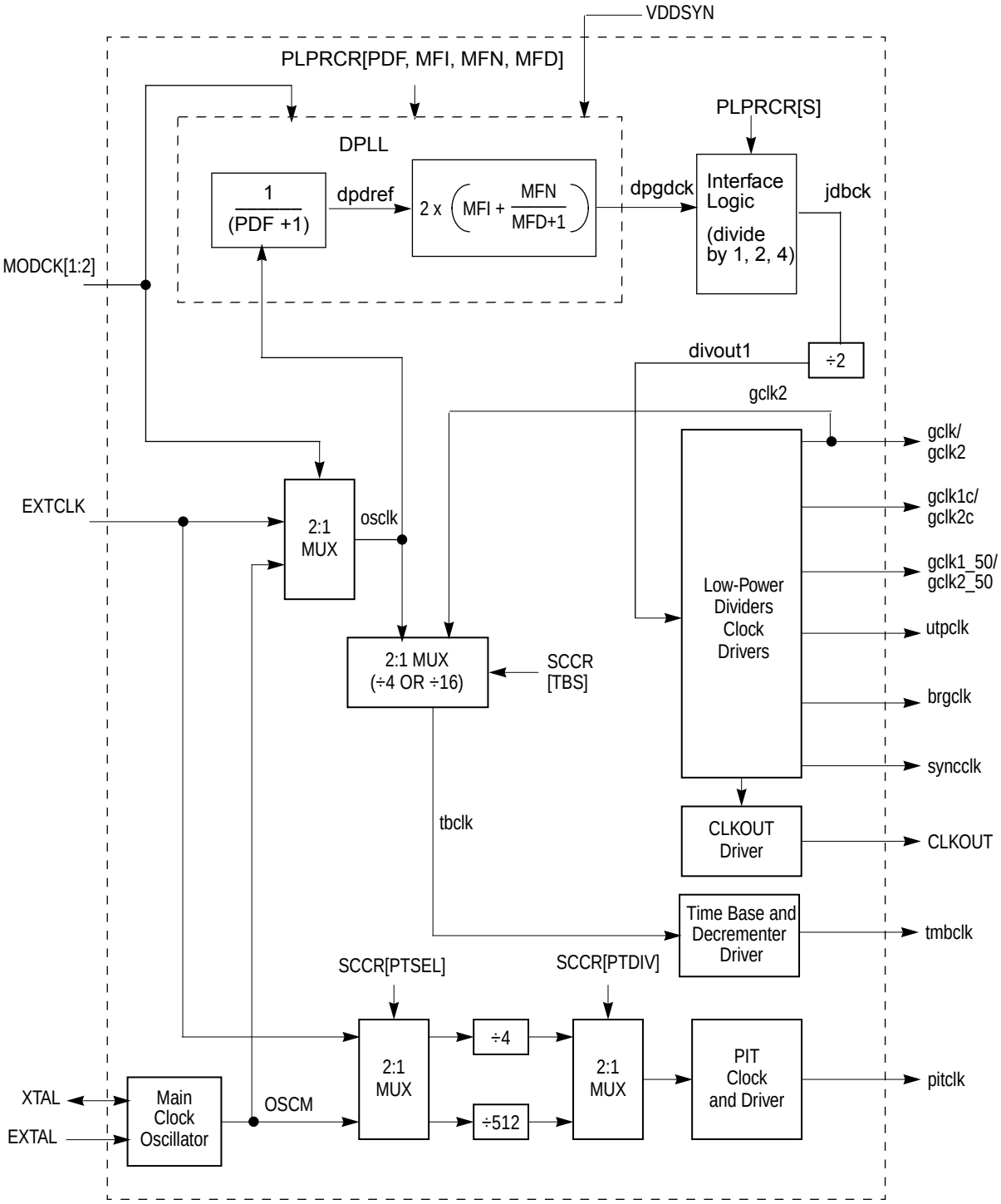
9 Development Boards

Freescale has developed an ADS board that accommodates the MPC8xx processors, including the MPC866/859 (see http://www.freescale.com/semiconductors for more information).

10 Clocks and Power Control

The MPC866 clock system provides many different clocking options for all on-chip and external devices. For its clock sources, the MPC866 contains PLL and crystal-oscillator support circuitry. The PLL circuitry can provide a high-frequency system clock from a low-frequency external source. Furthermore, to enable flexible power control, the MPC866 provides frequency divider options.

Figure 3 illustrates internal clock source and distribution that includes the DPLL and interface, clock dividers, drivers, and crystal oscillator.



Note that only CLKOUT is an actual external output; all other outputs are internal signals.

The real-time clock is not supported.

Figure 3. Clock Source and Distribution

10.1 Clock Module

The clock module consists of two external reference sources and a programmable PLL, arranged below in Figure 4.

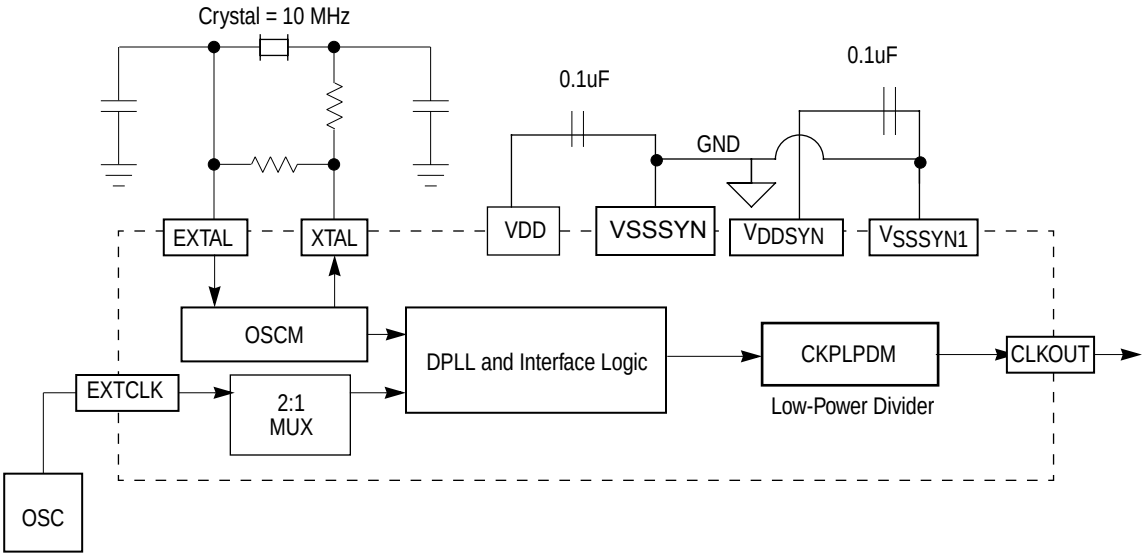


Figure 4. Clock Module Components

10.2 External Reference Clocks

The MPC866 has two input clock sources that are either provided at the EXTCLK pin or at the EXTAL and XTAL pins. These two clock sources can select to drive three internal clock signals (OSCLK, PITCLK, and TMBCLK). OSCLK provides the input clock to the PLL. PITCLK and TMBCLK provide dedicated clocks for special system timer circuitry, which includes the periodic interrupt timer (PIT), timebase (TB), and decrementer (DEC) in the SIU. These separate clock sources for the PIT, TB, and DEC enable these modules to continue counting at a fixed, user-defined rate regardless of system frequency.

The clock sources for OSCLK, PITCLK, and TMBCLK are selected at reset. The sources for PITCLK and TMBCLK can also be selected in software by manipulation of SCCR. See Section 10.3.1, “System Clock and Reset Control Register (SCCR).” For more information, see Section 10.2.2, “DPLL Reset Configuration,” and the *MPC866 PowerQUICC™ Family User’s Manual*, Section 14.3.2, “PIT Clock (PITCLK)” and Section 14.3.3, “Time Base and Decrementer Clock (TMBCLK).”

NOTE

It is possible to use both clock sources in a system so that each provides reference for different functions. If neither reference source is used, input should be grounded. Do not select the crystal oscillator circuit as OSCLK while also driving a high-frequency clock source on EXTCLK; noise from the EXTCLK clock source couples into the crystal oscillator circuit and might not allow the DPLL to lock. The converse, however, is allowable; EXTCLK can be selected as OSCLK while the crystal oscillator circuit supplies a separate frequency reference.

A typical configuration uses a canned oscillator with the EXTCLK input selected as OSCLK and a 10-MHz crystal at EXTAL and XTAL to provide PITCLK.

Four different PLL Modes that the MODCK pins define at reset determine the initial value of the PLPRCR register. Three of these modes require a 10-MHz input frequency, while the fourth mode can accept from 45 to 66 MHz. After reset, the PLPRCR can be programmed to achieve a different general system clock if the following requirements are met:

- OSCM is 10 MHz only (MODCK = 00 or 01).
- EXTCLK is 10 MHz (MODCK = 11).
- EXTCLK is 45 MHz to 66 MHz (MODCK = 10).

The input frequency requirements at reset are shown in Table 9.

Table 9. Input Frequency Requirements

MODCK[1-2]	Freq. In	PDF	MFI, MFN, MFD for DPGDCK
00, 01	OSCM = 10 MHz	0	160 MHz < OSCLK * 2 * (MFI + (MFN / (MFD+1))) < 320 MHz
11	EXTCLK = 10 MHz	0	160 MHz < OSCLK * 2 * (MFI + (MFN / (MFD+1))) < 320 MHz
10	45 MHz ≤ EXTCLK ≤ 66 MHz	10 MHz ≤ EXTCLK / (PDF+1) ≤ 32 MHz	160 MHz < OSCLK * 2 * (MFI + (MFN / (MFD+1))) / (PDF+1) < 320 MHz

10.2.1 DPLL and Interface

The DPLL in the MPC866 generates the overall system operating frequency in integer and non-multiples of the input clock frequency. CLKOUT synchronization is not guaranteed for non-integer multiples of OSCLK. If CLKOUT is an integer multiple of OSCLK/EXTCLK, the rising edge of EXTCLK is aligned (locked/synchronized) with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.

Digital implementation of frequency control and loop filtering functions in the design of the DPLL allows the following new features:

- Elimination of an on-board loop filter capacitor, minimization of internal capacitor value
- Selection of frequency and phase/frequency operation modes
- Improved noise immunity, eliminating additional supply and ground pins
- High-frequency resolution with a reduced lock time
- Reduced sensitivity to parameter variations that temperature and process cause

The main purpose of the DPLL is to generate a stable reference frequency by multiplying the frequency and eliminating the clock skew. The DPLL allows the processor to operate at a high internal clock frequency using a low-frequency clock input, providing two advantages. First, lower frequency clock input reduces the overall electromagnetic interference that the system generates. Second, the programmability of the oscillator enables the system to operate at a variety of frequencies with a single external clock source.

The DPLL reference clock (OSCLK) can be generated from either of the external clock sources described in Section 10.2, “External Reference Clocks.”

Inside the DPLL, the OSCLK is divided by the pre-division factor (PDF + 1) to generate a DPDREF clock. The frequency range of DPDREF is 10 to 32 MHz. This DPDREF clock is used farther inside the DPLL to generate the output clock of the DPLL, that is, DPGDCK (see Figure 3). The frequency range of DPGDCK

is 160 to 320 MHz. These frequency ranges must be maintained by both the reset configuration settings of the DPLL and interface and the final operating frequency of the DPLL and the interface.

The interface logic works in three modes, depending on divider selection input PLPRCR[S]. The formula for the output frequency of the DPLL and interface logic for each mode is given according to the following formula:

$$jdbck = 2 * \left(\frac{MFI + (MFN/(MFD+1))}{PDF + 1} \right) * OSCLK / 2^{S}$$

for S = 0, 1, or 2

NOTE

For synchronization between EXTCLK to CLKOUT, the total value by which the EXTCLK is multiplied must be an integer.

The total MF factor [MFI + (MFN/(MFD+1))] is an integer as a prerequisite.

Table 10 shows the DPLL parameters for some typical system frequencies during normal operation. The frequency after power-on reset is shown in Table 11. The multiplication factors (MF) shown are for the integer part (MFI), the numerator part (MFN), the denominator part minus 1(MFD), and the pre-division factor minus 1 (PDF) with their ranges listed in Table 10. The total MF value, MFI+(MFN/(MFD+1)), must be between 5 and 15.

Table 10. Typical System Frequency Generation

Input Frequency in MHz (f_{ref})	PDF	MFI	MFN [1]	MFD	dpgdck	PLPRCRS[10:11]	JDBCK	General System Frequency (MHz) [GCLK2] [2]
10	0	8	0	0	160	1	80	40
10	0	9	6	9	192	1	96	48
10	0	10	4	9	208	1	104	52
10	0	13	2	9	264	1	132	66
10	0	15	0	0	300	1	150	75
10	0	10	0	0	200	0	200	100
10	0	13	3	9	266	0	266	133
45	3	8	0	0	180	1	90	45
45	2	8	1	2	250	0	250	125
50	2	9	0	0	300	1	150	75
50	1	5	2	6	264	0	264	132
66	2	6	0	1	264	1	132	66
66	2	6	0	1	264	0	264	132

1 For MFN = 0, EXTCLK will be synchronized to CLKOUT.

2 Assuming DFNH = 0 and CSR = 0

The OSCLK can be supplied by either a crystal or an external clock oscillator. Crystals are typically much cheaper than clock oscillators; however, a clock oscillator has significant design advantages over a crystal circuit in that clock oscillators are easier to work with, resulting in faster design, debugging, and production.

10.2.2 DPLL Reset Configuration

While $\overline{\text{PORESET}}$ is asserted, the reset configuration of the DPLL is sampled on the MODCK[1-2] pins. The DPLL immediately begins to use the multiplication factor and pre-division factor values and external clock source for OSCLK determined by the sampled MODCK[1-2] pin and attempts to achieve lock. The MODCK[1-2] signals should be maintained steadily throughout $\overline{\text{PORESET}}$ assertion. The mode selection field and various factors are set as shown in Table 11. After $\overline{\text{PORESET}}$ is negated, the MODCK[1-2] values are internally latched, and the signals that are applied to MODCK[1-2] can be changed.

Table 11. Power-On Reset DPLL Configuration

MODCK[1-2]	Default at Power-On Reset		OSCLK (DPLL and Interface input)	General System Frequency (GCLK2)
	MFI[12-15]	PDF[27-30]		
00	8	0000	OSCM Freq	40 MHz (for OSCLK freq = 10 MHZ)
01	15	0000	OSCM Freq	75MHz (for OSCLK freq = 10 MHZ)
10 [1]	6	0010	EXTCLK Freq	1:1 Mode (The allowable frequencies on EXTCLK are 45 MHz to 66 MHz)
11	15	0000	EXTCLK Freq	75 MHz (for EXTCLK freq = 10 MHZ)
Note: Note: S = 1, MFN = 0, MFD = 1 for all of the reset con gur ations. **Note:** The general system clock[GCLK2] is jdbck divided by 2. **Note:** divout1 is jdbck divided by 2.				

[1] For Revision 0.x of the MPC866, MFI = 8 and PDF = 0011 binary

NOTE

Under no condition should the voltage on MODCK1 and MODCK2 exceed the power supply voltage V_{DDH} applied to the part.

At power-on reset, before the PLL achieves lock, the MPC866 does not generate any internal or external clocks, which can cause higher than normal static current during the short period of stabilization.

10.3 Clock and Power Control Registers

The following sections describe the clock and power control registers.

10.3.1 System Clock and Reset Control Register (SCCR)

The DPLL has a 32-bit control register, the system clock, and reset control register (SCCR), shown in Figure 5, which are memory-mapped into the MPC866 SIU's register map.

	0	1 2	3 5	6	7	8	9	10	11 12	13 14	15
Field	—	COM	—	TBS	PTDIV	PTSEL	CRQEN	—	—	EBDF	—
HRESET	—	#	0	#	#	#	0	0	0	†	0
POR	0	0	0	0	*	*	0	0	0	†	0
R/W	R/W										
Addr	(IMMR&0XFFFF0000) + 280										

	16	17 18	19 20	21 23	24 26	27 29	30 31
Field	—	DFSYNC	DFBRG	DFNL	DFNH	DFUTP	DFAUTP
HRESET	0						
POR	0						
R/W	R/W						
Addr	(IMMR&0XFFFF0000) + 282						

Note: HRESET is hard reset and POR is power-on reset.

The eld is unde ned
—The eld is unaff ected.
* PTDIV depends on the combination of MODCK1 and MODCK2. PTSEL depends on MODCK1. See Table 12 for more information.
† This eld is set according to the def ault of the hard reset con gur ation word.

Figure 5. System Clock and Reset Control Register (SCCR)

This register is effected by HRESET but is not affected by SRESET. Table 12 describes SCCR fields.

Table 12. SCCR Field Descriptions

Bits	Name	Description
0	—	Reserved, should be cleared
1–2	COM	Clock output module. This eld controls the output b uffer of the CLKOUT pin. When both bits are set, the CLKOUT pin is held in the high state. These bits can be dynamically changed without generating spikes on the CLKOUT pin. If the CLKOUT pin is not connected to external circuits, clock output should be disabled to minimize noise and power dissipation. The COM eld is cleared by hard reset. 00 Clock output enabled full-strength buffer 01 Reserved 10 Reserved 11 Clock output disabled
3–5	—	Reserved, should be cleared
6	TBS	Timebase source. Determines the clock source that drives the timebase and decrementer. 0 Timebase frequency source is the OSCLK divided by 4 or 16. 1 Timebase frequency source is GCLK2 divided by 16.
7	PTDIV	Periodic interrupt timer clock divide. Determines if the clock, the crystal oscillator, or main clock oscillator to the periodic interrupt timer is divided by 4 or 512. At power-on reset, this bit is cleared if the MODCK1 and MODCK2 signals are low. 0 The clock is divided by 4. 1 The clock is divided by 512.

Table 12. SCCR Field Descriptions (continued)

Bits	Name	Description
8	PTSEL	Periodic interrupt timer select. Selects the crystal oscillator or main clock oscillator as the input source to PITCLK. At power-on reset, it re ects the v alue of MODCK1. 0 OSCM (crystal oscillator) is selected. 1 EXTCLK is selected.
9	CRQEN	CPM request enable. Cleared by power-on or hard reset. In low-power modes, speci es if the general system clock returns to high frequency while the CP is active. 0 The system remains in low frequency even if the communication processor module is active. 1 The system switches to high frequency when the communication processor module is active.
10	—	Reserved, should be cleared
11–12	—	Reserved, should be cleared
13–14	EBDF	External bus division factor. This eld de nes the frequency division f actor between GCLKx and GCLKx_50. CLKOUT is similar to GCLK2_50. The GCLKx_50 is used by the bus interface and memory controller to interface with an external system. This eld is initializ ed during hard reset using the hard reset con gur ation word in the *MPC866 PowerQUICC™ Family User's Manual,* Section 11.3.1.1, "Hard Reset Con gur ation Word." 00 CLKOUT is GCLK2 divided by 1. 01 CLKOUT is GCLK2 divided by 2. 10 Reserved 11 Reserved
15–16	—	Reserved, should be cleared
17–18	DFSYNC	Division factor for the SYNCCLK. This eld sets the div out1, where divout1 is equivalent to JDBCK divided by 2, frequency division factor for the SYNCCLK signal. Changing the value of this eld does not result in a loss-of-lock condition. This eld is cleared b y a power-on or hard reset. 00 Divide by 1 (normal operation). 01 Divide by 4. 10 Divide by 16. 11 Divide by 64.
19–20	DFBRG	Division factor of the BRGCLK. This eld sets the div out1, where divout1 is equivalent to JDBCK divided by 2, frequency division factor for the BRGCLK signal. Changing the value of this eld does not result in a loss-of-lock condition. This eld is cleared b y a power-on or hard reset. 00 Divide by 1 (normal operation). 01 Divide by 4. 10 Divide by 16. 11 Divide by 64.
21–23	DFNL	Division factor low frequency. Sets the divout1, where divout1 is equivalent to JDBCK divided by 2, frequency division factor for general system clocks to be used in low-power mode. In low-power mode, the MPC866 automatically switches to the DFNL frequency. To select the DFNL frequency, load this eld with the divide v alue and set the CSRC bit. A loss-of-lock condition does not occur when changing the value of this eld. This eld is cleared b y a power-on or hard reset. 000 Divide by 2. 001 Divide by 4. 010 Divide by 8. 011 Divide by 16. 100 Divide by 32. 101 Divide by 64. 110 Reserved 111 Divide by 256.

Table 12. SCCR Field Descriptions (continued)

Bits	Name	Description
24–26	DFNH	Division factor high frequency. Sets the divout1, where divout1 is equivalent to JDBCK divided by 2, frequency division factor for general system clocks to be used in normal mode. In normal mode, the MPC866 automatically switches to the DFNH frequency. To select the DFNH frequency, load this eld with the divide v alue and clear CSRC. A loss-of-lock condition does not occur when this eld is changed. This eld is cleared b y a power-on or hard reset. 000 Divide by 1. 001 Divide by 2. 010 Divide by 4. 011 Divide by 8. 100 Divide by 16. 101 Divide by 32. 110 Divide by 64. 111 Reserved
27–29	DFUTP	UTOPIA clock dividers; see the *MPC866 PowerQUICC™ Family User's Manual*, Section 41.2, "UTOPIA Mode Registers."
30–31	DFAUTP	

10.3.2 PLL and Reset Control Register (PLPRCR)

The 32-bit system PLL and reset control register (PLPRCR) shown in Figure 6 controls the system frequency and low-power mode operation.

	0	4	5	9	10	11	12	15
Field	MFN		MFD		S		MFI	
HRESET	—		—		—	—	—	
POR	0000		00001		0	1	*	
R/W	R/W							
Addr	(IMMR&0xFFFF0000) + 284							

	16	17	18	19	20	21	22	23	24	25	26	27	30	31
Field	—	TEXPS	—	—	—	CSRC	–		CSR	—	FIOPD	PDF		DBRMO
HRESET	—	1	0	0	0	0	0		—	—	—	0000		0
POR	0	1	0	0	0	0	0		0	0	0	*		0
R/W	R/W													
Addr	(IMMR&0xFFFF0000) + 286													

Notes: HRESET is hard reset and POR is power-on reset. * POR depends on the combination of MODCK1 and MODCK2. See Table 13 for more information.

Figure 6. PLL and Reset Control Register (PLPRCR)

HRESET and SRESET affect this register. Table 13 describes PLPRCR bits.

Table 13. PLPRCR Field Descriptions

Bits	Name	Description
0–4	MFN	Numerator of the fractional part of the multiplication factor in the formula for the output frequency of the DPLL and Interface. The range of values for the MFN is 0 to 31. The numerator of the fractional part of the multiplication factor (MFN) must be less than the denominator of the fractional part of the multiplication factor (MFD+1). [1] If the numerator is larger than the denominator, the output clock frequency will differ from the desired frequency. If the numerator is zero, then the circuit for fractional division is disabled to save power. See Section 10.2.1, “DPLL and Interface”
5–9	MFD	Denominator minus 1 of the fractional part of the multiplication factor in the formula for the output frequency of the DPLL and Interface.The range of values for the MFD is 1 to 31. The denominator of the fractional part of the multiplication factor(MFD+1) must be greater than the numerator of the fractional part of the multiplication factor MFN. [1] If the numerator is larger than the denominator, the output clock frequency will differ from the desired frequency. If the numerator is zero, then the circuit for fractional division is disabled to save power. See Section 10.2.1, “DPLL and Interface”
10–11	S	Selection Bits for the Divider after the Double Clock (fdck) 00 Divide By 1 01 Divide By 2 10 Divide By 4 11 = Reserved. See Section 10.2.1, “DPLL and Interface”
12–15	MFI	Integer part of the multiplication factor in the formula for the output frequency of the DPLL and Interface. The range of values for the MFI is 5 to 15. [1] If the MFI is less than 5, the DPLL will use 5. See Section 10.2.1, “DPLL and Interface”
16	—	Reserved
17	TEXPS	Timer expired status. Internal status bit set when the periodic timer expires, the timebase clock alarm sets, the decrementer interrupt occurs, or the system resets. This bit is cleared by writing a 1; writing a zero has no effect. 0 TEXP is negated. 1 TEXP is asserted.
18	—	Reserved, should be cleared
19	—	Reserved, should be cleared
20	—	Reserved, should be cleared
21	CSRC	Clock source. Speci es whether DFNH or DFNL gener ates the general system clock. Cleared by hard reset. 0 The general system clock is generated by the DFNH eld. 1 The general system clock is generated by the DFNL eld.
22–23	—	Reserved, should be cleared
24	CSR	Checkstop reset enable. Enables an automatic reset when the processor enters checkstop mode. If the processor enters debug mode at reset, then reset is not generated automatically; refer to Table 14. See the *MPC866 PowerQUICC™ Family User’s Manual*, Section 45.5.2.2, “Debug Enable Register (DER).”
25	—	Reserved, should be cleared

Table 13. PLPRCR Field Descriptions (continued)

Bits	Name	Description
27-30	PDF	Pre-division factor minus 1 in the formula for the output frequency of the DPLL and interface. The range of values for the PDF is 0 to 15. Refer to Section 10.2.1, “DPLL and Interface.”
31	DBRMO	DPLL BRM order bit 0 First order (should be used when fractional part, MFN/MFD, in undivisible form is greater than 1/10) 1 Second order (should be used when fractional part, MFN/MFD, in undivisible form is less than 1/10) This bit is ignored if the MFN is 0.

[1] The total multiplication factor, including both the integer and fractional parts, must be between 5 to 15.

Table 14 describes PLPRCR[CSR] and DER[CHSTPE] bit combinations.

Table 14. PLPRCR[CSR] and DER[CHSTPE] Bit Combinations

PLPRCR[CSR]	DER[CHSTPE]	Checkstop Mode	Result
0	0	No	—
0	0	Yes	—
0	1	No	—
0	1	Yes	Enter debug mode
1	0	No	—
1	0	Yes	Automatic reset
1	1	No	—
1	1	Yes	Enter debug mode

11 ATM Operational Differences

To highlight some of the operational differences between the 860 and the 866 ESAR functions, the reception and transmission of a typical ATM cell will be discussed for both processors.

11.1 ATM Cell Reception – 860 (SAR)

1. Cell is received from the transmission line by means of the UTOPIA interface and put into FIFO. When the RxClav signal (receive cell available) is asserted by the PHY, the SAR receives a cell from that PHY.
2. Read cell header. In SAR mode, the UTOPIA is controlled by microcode that uses registers that are 4 bytes long. When the RxClav is sent to the CPM, the cell is read in to the processor four bytes at a time.
3. Address look-up. Match the header to get the correct channel number.
4. Get parameters from memory.
5. Read data from PHY UTOPIA interface to the CPM, which involves calculating the cyclic redundancy check (CRC) and sending out the relevant address to the DMA for memory access.

6. The relevant parameters in memory (buffer descriptor pointers, CRC counters and so on) are updated.

11.2 ATM Cell Reception – 866 (ESAR)

1. Cell is received from the transmission line using the UTOPIA interface and put into FIFO. When the RxClav signal (Receive Cell Available) is found to be asserted by the PHY, the ESAR will receive a cell from that PHY.
2. Read cell header. In 866 ESAR, there is a UTOPIA hardware block that reads the entire cell into an internal 2 cell FIFO in a minimal amount of time. Hence, when the RxClav is sent to the CPM, the cell (n bytes) is read in to the processor within (n) clock cycles.
3. Address look-up. Match the header to get the correct channel number.
4. Get parameters from memory.
5. Read data from PHY UTOPIA interface to the CPM, which involves calculating the CRC and also sending out the relevant address to the DMA for memory access.
6. The relevant parameters in memory (buffer descriptor pointers, counters, and so on) are updated.

The most noticeable difference between the 860 SAR and 866 ESAR modes of operation is the actual implementation of how the UTOPIA interface reads the whole cell into the CPM during cell reception. On the 860, the microcode controls the UTOPIA interface. However, the 866 has a cell FIFO that the UTOPIA hardware block implements, and is independent from any microcode. This added 866 ESAR functionality requires some additional processing overhead, although reading a cell takes a significantly shorter period of time on 866 compared to 860.

For example, when the 860 SAR reads a complete ATM cell of 53 bytes, it takes between 300 – 500 CPM clock cycles, depending on available bandwidth. The 866 ESAR, on the other hand, requires around 15-20% fewer clock cycles and is much more efficient in terms of speed and utilized bandwidth.

11.3 ATM Cell Transmission – 860 (SAR) / 866 (ESAR)

The user-defined APC scheduler controls this process (assuming that the IAQ bit is not set). The PHY asserts the TxClav signal (transmit cell available) when space is available in the PHY. If the APC is ready to transmit and space is available in the FIFOs, the cell is transmitted.

1. If a cell is available (TxClav is asserted) and the APC scheduler is ready to transmit, the channel number is read from the APC transmit queue.
2. Read channel parameters – buffer descriptors, counters, and so on.
3. Transmit header. If the cell that will be transmitted is an AAL5 cell, the information resides in connection tables and parameter RAM. If the cell to be transmitted is an AAL0 cell, the information resides in memory.
4. Transmit payload, which includes direct memory access (DMA) from the buffers with optional CRC.
5. Update parameters – parameter table entries.

12 Programming Considerations

To take advantage of new features on the 866 device, consider a number of significant programming items:

- SCC Parameter RAM. Page 4 of this memory area contains all of the necessary connection tables, buffer descriptors, and data buffers that the 866 operation requires. This section of memory **MUST** be cleared during the initialization sequence before any 866 operation. If it is not cleared, the 866 may not operate or may operate unpredictably.
- To enable backwards-compatibility that performs 860SAR functionality using 866 silicon, *all* ESAR bits must be cleared through the ESAR register set to reduce the complexity of the internal microcode. The ESAR bits in registers SRSTATE, STSTATE, APCST should all be cleared. Similarly, if 866 ESAR functionality is required, these bits should be set in all of the above registers.
- The 866 ESAR device allows the user to program or modify any memory location on-the-fly without conflicting with the current CPM process. It is only possible to do this action using the WRITE_TO_MEMORY command. Attempting to modify any memory location without using this command causes system CPM failure. (Adding or removing internal channels and modifying the APC period can also be changed on-the-fly in both 860 SAR and 866 ESAR modes.)
- Avoid writing non-zero values to the 32-bit location IMMR+0x3CB8 on the 866 even for non-ATM applications unless Freescale specifically requires it.. The 866 reserves this location for internal CPM usage.

13 866 ESAR Mode - Internal Resource Conflicts

When operating an ATM application in 866 ESAR mode, internal resource conflicts can cause the MPC866 to lose some functionality. The following subsections detail potential restrictions and conflicts that can arise.

13.1 Parameter RAM Conflicts

Because the 866 ESAR mode requires additional memory, be aware of the potential conflicts that can occur in parameter RAM. If operating in serial ATM mode on SCC1-4 or UTOPIA on SCC4, other peripherals can lose their parameter RAM. The serial ATM parameters of SCC1 extend into the I2C parameter RAM. Similarly, the parameter RAM for SCC2/SPI, SCC3/SMC1, and SCC4/SMC2/PIP are affected in the same manner.

To relocate the parameter RAM for the SMCs, I2C, and SPI controllers to a non-conflicting location, use RAM-based microcode patches. These microcode patches are available on the Freescale MPC860 web-site. (On MPC866 the relocation of the I2C/SPI does not require a RAM microcode patch. The device contains the relocatable I2C/SPI functionality and works as described in the pdf for the RAM-loadable microcode of previous revisions.)

13.2 IDMA2 Conflicts

Use IDMA2 only in level-sensitive mode when ATM is enabled. To achieve this mode, set the RCCR[DR1M] bit.

13.3 UTOPIA Conflicts

The UTOPIA interface is implemented using the hardware of IDMA1 and the parameter RAM page of SCC4. Therefore, the following situations occur if the UTOPIA port is used:

- SCC4 is unavailable because parameter RAM page 4 is lost.
- IDMA1 is unavailable. (The DREQ0 signal is lost, and the IDMA1 event and mask registers IDSR1 and IDMR1 are used for UTOPIA events.)
- Ethernet CAM support for SCC2, SCC3, and SCC4 is unavailable (because REJECT2, REJECT3, and REJECT4 are lost).
- Parallel interface port (PIP) is unavailable (because the PIP handshake signals are lost).

Furthermore, the UTOPIA interface can be made to operate in either UTOPIA split bus mode of operation or using mixed bus mode operation. Depending on initial register programming, specific port pin functions are available or unavailable. In 866/859 ESAR multi-PHY mode, the following situations occur:

- In UTOPIA split bus mode, PCMCIA port A and the Fast Ethernet controller's (FEC) MII signals are unavailable. However in UTOPIA mixed bus mode, the MII signals or the PCMCIA port A signals are still available on the PCMCIA port A pins.
- The PHY address signals conflict with the signals of both SMCs. However, when a PHY address signal is not activated, the pin's other signal functions become available. For example, if only eight PHYs are used in a UTOPIA master application, the SMC1 data signals are still available.

14 Register Comparison Between 860SAR & 866 (ESAR)

The spreadsheets and information that are shown in Figure 7 and Table 15 through Table 16 detail the differences between 860SAR and 866ESAR throughout the register set of the MPC8XX:

Connection Tables – SAR vs. ESAR

Receive Function Code & Status Register

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field				BO		FC			EXT	ACP	EC*	SNC*	ESAR	MCF	SER	MPHY*

ESAR	Must also be set to enable ESAR functionality
MCR	Enable management cell Iter
* Available only in SCC4 UTOPIA mode, otherwise written as 0	

Transmit Function Code & Status Register

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field				BO		FC			EXT		EC*	SNC*	ESAR		SER	MPHY*

ESAR	Must also be set to enable ESAR functionality
* Available only in SCC4 UTOPIA mode, otherwise written as 0	

APC Status Register

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field		CSER		NSER		*			**				ESAR	DIS	PL2***	MHY

ESAR	Must also be set to enable ESAR functionality
*	Was NMPHY on SAR, now bits [2..6] in MPHY status register on ESAR
**	Was CMPHY on SAR, now bits [10..14] in MPHY status register on ESAR
**	Used only if ESAR is not set for backwards-compatibility with the MPC860SAR

MPHY Status Register

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field			NMPHY								CMPHY					

NMPHY	Number of Multiple PHYs
CMPHY	Current Multiple PHYs

CPM Command Register

Figure 7. Differences in the Register Set Between the MPC860 and the MPC866

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	RST	ATM OPCODE			OPCODE = 1111				CH_NUM					OPCODE 2		FLG

ATM OPCODE	111 = ATM ESAR Write to Memory Command or internal command (see OPCODE 2) 00 = RESERVED, normal ATM OPCODES apply when 00 is written to these two bits 01 = ACTIVATE PM - to activate PM session on the channel number speci ed b y the COMM_CH eld. * 10 = DEACTIVATE PM - To deactivate PM session on the channel number speci ed b y the COMM_CH eld. * 11 =RESERVED
OPCODE 2	OPCODE 2 commands are only valid when ATM OPCODE=111

ESAR APC Status Register (From APC Parameter RAM)

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	APCOM	*	LAST	*								EQ	ESAR	DIS	*	MPHY

*	Reserved
APCOM	APC table overrun event mask for this APC level.
LAST	This priority level is the last APC level for the speci c PHY#.
EQ	APC table and PTP queue of this speci c le vel have equal priority. The APC mechanism schedules cells to be transmitted evenly from the two utilities. This bit is valid only if the DIS bit is NOT set.
ESAR	Selects the new features of ESAR or allows backwards-compatibility with the older SAR functionality. To enable ESAR functionality, all bits must be programmed to the desired value throughout the ESAR register set.
DIS	APC table is disabled at this level. PTP queue is still serviced. All lower levels down to LAST are still serviced.
MPHY	All M-PHY bits (throughout the ESAR register set) should be set to desired values when working with multi-PHY.

Utopia Mode Event Register

Base	0	1	2	3	4	5	6	7	-	-	-	-	-	-	-	
Field				SYNC	IQOV	GINT	GUN	GOV								

GUN	Global transmitter underrun in UTOPIA's tx cell FIFO.
GOV	Global receiver underrun in UTOPIA's rx cell FIFO

Figure 7. Differences in the Register Set Between the MPC860 and the MPC866

Interrupt Queue Entry

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	V	W		CNG					APCO		TQF	UN	RXF	BSY	TXB	RXB

	TQF	Transmit queue full - this bit is valid in case that an APC bypass command was issued and the transmit queue is full, indicating that the APC bypass command was not performed. This bit is valid only for AAL0 PTP channels where ITQ option is set.

Performance Monitoring

Section 38.3 of the User Manual covers this new feature for ESAR. Correct configuration is achieved by programming table 38-2.

Connection Tables - SAR vs. ESAR

Receive Connection Table - RCT

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	FHNT	PM							HEC	CLP	CNG/ NCRC	INF	CNGI/ PTP	CDIS	AAL	

CT_Offset + 0	PM	Performance monitoring
	NCRC	No CRC (AAL0 only) / Congestion (AAL5 only)
	PTP	Port-to-port cell switching / Congestion interrupt (AAL5 only)
CT_Offset + 2	RBALEN	
CT_Offset + 4	RCRC	
CT_Offset + 6		
CT_Offset + 8	RB_PTR	
CT_Offset + A		
CT_Offset + C	RTMLEN	
CT_Offset + E	RBD_PTR	
CT_Offset + 10	RBASE	
CT_Offset + 12	TSTAMP	

Figure 7. Differences in the Register Set Between the MPC860 and the MPC866

CT_Offset + 14	AAL 2	IMASK
	AAL 2	Indicates this VC is an AAL2 channel. Must initialize prior to setting !
CT_Offset + 16	FT	NIM | | | RPMT | | |
	FT	Filter type
	NIM	Non-intrusive monitoring
	RPMT	Receive performance monitoring table number
CT_Offset + 18 to CT_Offset + 1F	Reserved	

Port-to-Port Specific Receive Connection Table - PTP RCT

When PTP function is used, a new RCT must be defined called PTP RCT. It is a specific RCT which must be initialized as page 2-15. All of the fields are new.

Transmit Connection Table - TCT

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field		PM							PC			INF	CR10	CDIS	AAL	

CT_Offset + 20	PM	Performance Monitoring
CT_Offset + 22	TBALEN	
CT_Offset + 24	TCRC	
CT_Offset + 26		
CT_Offset + 28	TB_PTR	
CT_Offset + 2A		
CT_Offset + 2C	TTMLEN	
CT_Offset + 2E	TBD_PTR	
CT_Offset + 30	TBASE	

Figure 7. Differences in the Register Set Between the MPC860 and the MPC866

CT_Offset + 32					TPMT		AVCF	ACT	
	TPMT	Transmit performance monitoring table number							
	AVCF	Auto VC off							
	ACT	Active status							
CT_Offset + 34	CHEAD								
CT_Offset + 36									
CT_Offset + 38	APCL								
CT_Offset + 3A	APCPR								
CT_Offset + 3C	OUT	BNR	TSER	APCP					
	BNR	Buffer not ready (Internal Use)							
	TSER	Traf c ser vice type							
	APCP	APCP <= 4094 instead of 32766 in SAR							
CT_Offset + 3E	APCPF								

Transmit Connection Table Extensions TCTE

**Located at TCTEBASE programmed in Parameter RAM, the TCTE are located in DPRAM.
They support VBR channels to hold additional parameters for traffic shaping.**

Buffer Descriptors - SAR vs. ESAR

Receive Buffer Descriptor

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	E		W	I	L	F/ OAM	CM	FMC	HEC	CLP	CNG	ABT			LN	CR

Offset + 0	F/OAM	F (AAL5) First in frame. (AAL0) Operation and maintenance cell indication.
	FMC	Forward monitoring cell received + BRC elds added

Figure 7. Differences in the Register Set Between the MPC860 and the MPC866

Offset + 2	DATA LENGTH / CHANNEL CODE
	Number of bytes written into BD's data buffer (AAL5) / Channel number when AAL0 buffers + MCF bit set
Offset + 4	Rx data buffer pointer
Offset + 8	CPCS-UU+CPI
Offset + A	RESERVED
Offset + C	CELL HEADER EXPANSION 1
Offset + 10	CELL HEADER EXPANSION 2
Offset + 14	CELL HEADER EXPANSION 3

Transmit Buffer Descriptor

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	R		W	I	L	OAM	CM							ICNG	RH	ICLP

Offset + 0	OAM	User Cell / Non User Cell
	ICNG	Invert CNG bit (AAL5 only)
	RH	Replace header (AAL5 only)
	ICLP	Invert CLP bit (AAL5 only)
Offset + 2	Data Length	
Offset + 4	Tx Data Buffer Pointer	
Offset + 8	CPCS-UU+CPI / HEADER_L	
	HEADER_L	Lower half word of the replacement header
Offset + A	Reserved / HEADER_H	
	HEADER_H	Upper half word of the replacement header
Offset + C	CELL HEADER EXPANSION 1	
Offset + 10	CELL HEADER EXPANSION 2	
Offset + 14	CELL HEADER EXPANSION 3	

Figure 7. Differences in the Register Set Between the MPC860 and the MPC866

Table 15. Parameter RAM Mapping - SAR vs. ESAR

Serial and Utopia Interface Parameter RAM Map				
Offset from SCC Base	**Name**	**Description**	**SAR Function**	**ESAR Function**
0x00	RBDBASE	Base pointer for receive BDs		
0x04	SRFCR/SRSTATE	SAR receive function code and receive status	SRFCR/SRSTAE[12] does not exist SRFCR/SRSTAE[13]= DIS Disable Utopia receive process	SRFCR/SRSTAE[12]= ESAR bit Enable ESAR functions SRFCR/SRSTAE[13]= MCF Enable management cell lter
0x06	MRBLR	Maximum receive buffer length		
0x08	RSTATE	SCC internal receive state parameters		
0x0C	Reserved			
0x10	R_CNT	Receive internal byte counter		
0x12	STFCR/STSTATE		STFCR/STSTATE[9] = TQF Transmit Queue Full in 850SAR STFCR/STSTATE[9] = Reserved in 860SAR until Rev C1 STFCR/STSTATE[9] = TQF Transmit Queue Full in 860SAR in Rev D STFCR/STSTATE[11] = PBF Port B Flag STFCR/STSTATE[12] = Reserved	850 ESAR doesn't exist STFCR/STSTATE[9] = Reserved STFCR/STSTATE[9] = Reserved STFCR/STSTATE[11] = Reserved STFCR/STSTATE[12] = ESAR Enable ESAR functions
0x14	TBDBASE	Base pointer for transmit BDs		
0x18	TSTATE	SCC internal transmit state parameters		
0x1C	COMM_CH	Command channel		
0x1E	STCHNUM	Current transmit channel number		
0x20	T_CNT	Transmit internal byte counter		
0x22	CTBASE	Connection table base address		
0x24	ECTBASE	External connection table base address		
0x28	INTBASE	Interrupt base pointer		
0x2C	INTPTR	Pointer to interrupt queue		
0x30	C-MASK	Constant mask for CRC32		
0x34	SRCHNUM	Current receive channel number		
0x36	INT_CNT	Interrupt counter		
0x38	INT_ICNT	Interrupt initial value		
0x3A	TSTA	Time stamp timer address		

Table 15. Parameter RAM Mapping - SAR vs. ESAR (continued)

0x3C	OLDLEN	Transmitter temporary length		
0x3E	SMRBLR	SAR maximum receive buffer length register		
0x40	EHEAD	Empty cell header		
0x44	EPAYLOAD	Empty cell payload		
0x48	TQBASE	Transmit queue base pointer		TQBASE: Reserved in MPHY mode
0x4A	TQEND	Transmit queue end pointer		TQEND: Reserved in MPHY mode
0x4C	TQAPTR	Transmit queue APC pointer		TQAPT: Reserved in MPHY mode
0x4E	TQTPTR	Transmit queue transmitter pointer		TQTPTR: Reserved in MPHY mode
0x50	APCST	APC status Number of multiple PHY Current Multi PHY Utopia Level 2 MPHY Priority table Level 2	 APCST[5-7] = NMPHY APCST[8-10] = CMPHY APCST[12] = Reserved APCST[14] = PL2	 APCST[5-7] = Reserved Reserved if ESAR bit in APCST = 1 APCST[8-10] = Reserved Reserved if ESAR bit in APCST = 1 APCST[12] = ESAR APCST[14] = PL2 Reserved if ESAR bit in APCST = 1
0x52	APCPTR	APC parameter pointer		MPHY master: Points to MPHY pointing table
0x54	AM1	Address match parameter		
0x56	AM2	Address match parameter		
0x58	AM3	Address match parameter		
0x5A	AM4	Address match parameter		
0x5C	AM5	Address match parameter		
0x5E	ECSIZE	Expanded cell size/unassigned cell data		ECSIZE: new con gur ation
0x60	APCT_REAL	APC 32 bit counter		Used internally by the APC for VBR traf c. Must be initialized to zero.
0x64	R_PTR	Receiver internal data pointer		
0x68	RTEMP	Receiver temporary data storage		
0x6C	T_PTR	Transmit internal data pointer		
0x70	TTEMP	Transmitter temporary data storage		
0x74 to 0x7F	Reserved			

ESAR Parameters				
Offset from SCC Base	**Name**	**Description**	**SAR Function**	**ESAR Function**

Table 15. Parameter RAM Mapping - SAR vs. ESAR (continued)

0x80	FMCTIMESTMP	OAM performance monitoring time stamp counter address	Nonexistent	
0x84	FMCTEMPLATE	OAM performance monitoring - FMC template pointer	Nonexistent	
0X88	PMPTR	OAM performance monitoring table pointer	Nonexistent	
0x8A	PMCCHANNEL	Temporary storage containing pmchannel number	Nonexistent	
0x8C	Reserved		Nonexistent	
0x90	MPHYST	MultiPHY status	Nonexistent	
0x92	TCTEBASE	Internal TCT extension base	Nonexistent	
0x94	ETCTEBASE	External TCT Extension Base pointer	Nonexistent	
0x98	COMM_CH2	Second host command channel / MSB = 0x0000	Nonexistent	
0x9C	STATBASE	Statistics table base pointer	Nonexistent	
0x9C to 0xBF	Reserved			

Serial Interface Parameter RAM Map				
Offset from SCC Base	**Name**	**Description**	**SAR Function**	**ESAR Function**
0xC0	ALPHA	Receiver delineation alpha/delta counters		
0xC2	DELTA	Receiver delineation alpha/delta counters		
0xC4	RSTUFF	Receive data stuf ng location		
0xC8	SHUFFLESTATE	Receiver data shuf ing state		
0xCA	RHECTEMP	Receiver temporary HEC storage area		
0xCC	THECTEMP	Transmitter temporary HEC storage area		

Table 15. Parameter RAM Mapping - SAR vs. ESAR (continued)

0xCE	ASTATUS	Cell synchronization status register		
0xD0	HEC_ERR	HEC error counter		
0xD2	Reserved			
0xD4	RSCRAM	Receiver scrambling storage		
0xD8	RSCRAM1	Receiver scrambling storage		
0xDC	TSCRAM	Transmitter scrambling storage		
0xE0	TSCRAM1	Transmitter scrambling storage		
0xE4	RCRC	Receiver temporary CRC		
0xE8	TCRC	Transmitter temporary CRC		
0xEC	RCHAN	Receiver current channel		
0xF0	TCHAN	Transmitter current channel		
0xF4 to 0xFF	Reserved			

APC Parameter RAM Map				
Offset from SCC Base	**Name**	**Description**	**SAR Function**	**ESAR Function**
0x00	APCT_BASE1	APC table rst pr iority base pointer		
0x02	APCT_END1	First APC table length		
0x04	APCT_PTR1	First APC pointer		
0x06	APCT_SPTR1	First APC priority service pointer		
0x08	ETQBASE	Enhanced Transmit Queue base pointer		

Table 16. Parameter RAM Mapping - SAR vs. ESAR

0x0A	ETQEND	Enhanced Transmit Queue end pointer		
0x0C	ETQAPTR	Enhanced Transmit Queue APC pointer		
0x0E	ETQTPTR	Enhanced Transmit Queue transmitter pointer		
0x10	APC_MI	APC - Maximum iteration		
0x12	NCITS	Number of cells in time slot		
0x14	APCNT	APC - N timer		
0x16		Reserved		
0x18	EAPCST	APC status of the rst priority service		
0x1A	PTP COUNTER	First priority PTP queue length		
0x1C	PTP_TxCH	First priority PTP channel		
0x1E		Reserved		
(n * 0x20) + 0x0	APCT_BASEn	APC table—N'th priority table base pointer		
(n * 0x20) + 0x2	APCT_ENDn	N'th table —Length		
(n * 0x20) + 0x4	APCT_PTRn	N'th APC table pointer		
(n * 0x20) + 0x6	APCT_SPTRn	N'th table APC service pointer		
(n * 0x20) + 0x8 -> +0x17		Reserved		
(n * 0x20) + 0x18	EAPCSTn	APC status of the N'th priority service		
(n * 0x20) + 0x1C	PTP_COUNTERn	N'th priority PTP queue length.		
(n * 0x20) + 0x1E		Reserved		

15 Document Revision History

Table 17 shows the history of revisions and changes to this document.

Table 17. Revision History

Revision Number	Changes
0.0	Initial release
1.1	• Updates incorporated in document • Nontechnical reformatting changes
1.4	• Updates incorporated in document • Nontechnical reformatting changes
1.5	• Minimum Extclk frequency is now 45 MHz • In Table 10, two rows that said 40 MHz were changed to 45 MHz and parameters were updated • Light edit done

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How to Reach Us:

Home Page:
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USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
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