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Migrating from the MPC857T to the MPC885

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This document contains information that is useful when migrating from the MPC857T to the MPC885. Refer to the *MPC885 PowerQUICC™ Family Reference Manual* and *MPC885/MPC880 Hardware Specifications* (for MPC885), and the *MPC862 PowerQUICC™ Family Users Manual* and *MPC862/857T/857DSL Hardware Specifications* (for MPC857T) for more detailed information.

Contents

1 Overview

The need for embedded security and an additional Fast Ethernet channel makes the transition from an MPC857T to an MPC885 a logical progression. Both processors contain the same embedded PowerPC™ architecture-based core and system interface unit (SIU) to ease software migration.

The MPC885 has twice the internal L1 cache as the MPC857T for a total of 8 Kbytes for data and 8 Kbytes for instructions. The MPC885 has a faster core and faster bus speed than the MPC857T. The MPC885 incorporates four 16-bit timers that can be cascaded into two 32-bit timers.

The MPC885 incorporates two Fast Ethernet channels instead of one and has a similar communications processor module (CPM). However, the variety of serial channels has changed. While both the MPC857T and the MPC885 feature UTOPIA, the MPC885

can support full duplex UTOPIA and Fast Ethernet simultaneously. The MPC885 also has a USB controller and an on-chip security processor that can perform encryption on the serial channels and TDM interface.

2 Feature Comparison

The MPC857T and MPC885 communications microprocessors incorporate many types of communications engines to accommodate different system requirements. The following sections discuss hardware and protocol features of both microprocessors.

2.1 Hardware Features

Table 1 compares the MPC857T and the MPC885 hardware features.

Table 1. Hardware Features Comparison

Feature	MPC857T	MPC885
Core frequency (max)	100 MHz	133 MHz
Bus frequency (max)	66 MHz	80 MHz
I and D cache	4K	8K
FEC	1	2
Security	No	Yes
USB 1.1	No	Yes
Time slot assigner (TSA)	Yes	Yes
SPI	1	1
SMC	2	2
SCC	1	3
PCMCIA	Yes	Yes

2.2 Protocol Features

Table 2 compares the MPC857T and the MPC885 protocol features.

Table 2. Protocol Feature Comparison

Protocol	MPC857T	MPC885
10/100 Fast Ethernet	1	2
10BT Ethernet	Yes	Yes
HDLC/SDLC	Yes	Yes
UART	Yes	Yes
Transparent	Yes	Yes

3 The MPC885

The MPC885 PowerQUICC™ device is a 0.18-µm version of the MPC860 PowerQUICC family of communications microprocessors. Unlike the MPC857T, the MPC885 has a core voltage of 1.8 V and an I/O voltage of 3.3 V, with 5-V input compatibility (on some I/O pins). The MPC885 supports a maximum core speed of 133 MHz and a maximum external bus speed of 80 MHz (in 1:1 mode).

The MPC885 incorporates the same embedded MPC8XX processor core and similar CPM and SIU. The MPC885 also supports an on-chip security engine and two 10/100 Fast Ethernet controller modules. The CPM supports USB 1.1, three SCCs (SCC2, SCC3, and SCC4), two SMCs (SMC1 and SMC2), SPI, and I^2C. The SCCs can support IEEE 802.3 Ethernet, ATM, HDLC/SDLC, UART, and transparent protocols.

Figure 1 shows the MPC885 block diagram.

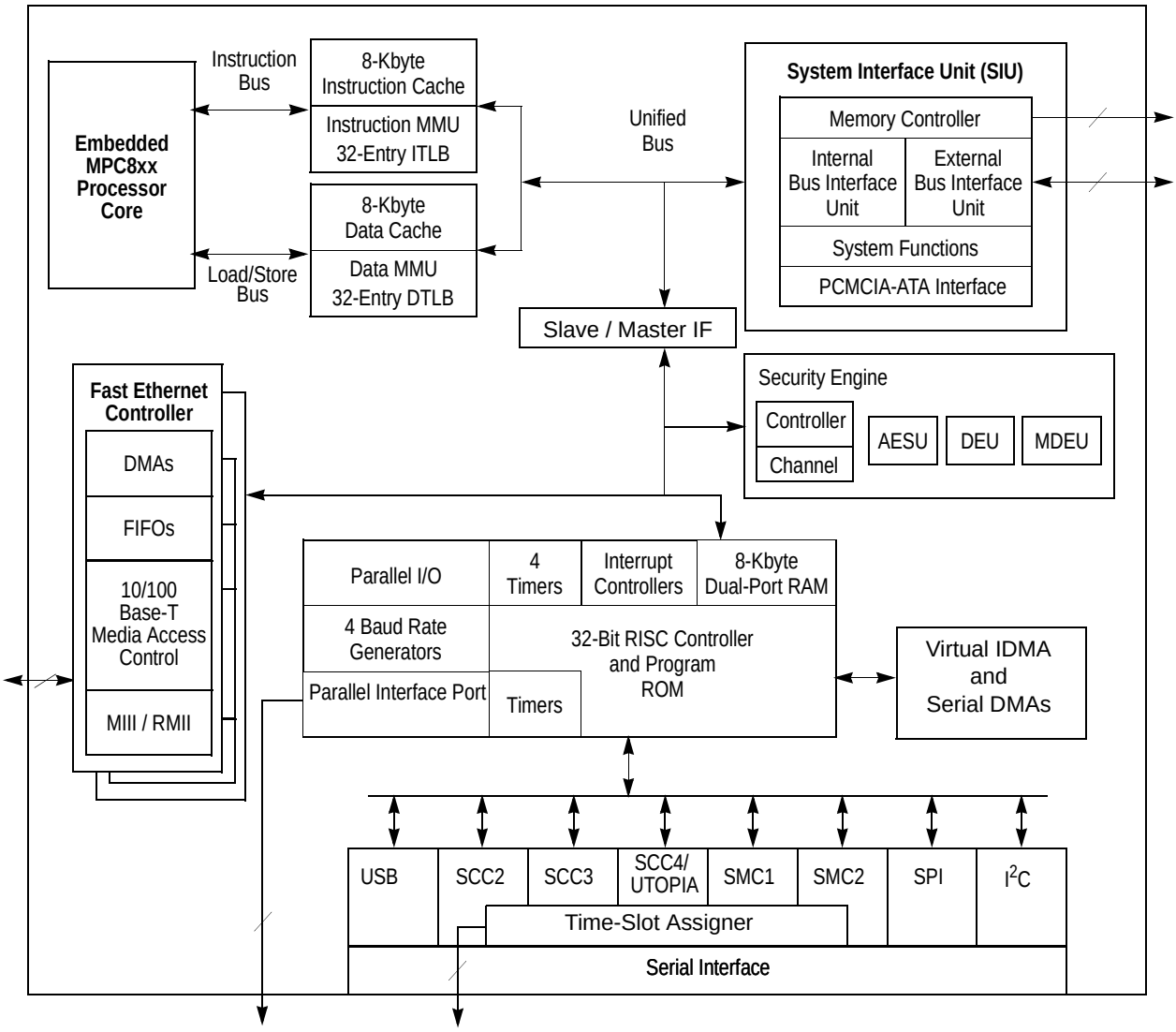


Figure 1. MPC885 Block Diagram

4 The MPC857T

The MPC857T PowerQUICC device is a 0.32-µm version of the MPC8XX PowerQUICC family of communications microprocessors. The MPC857T has a core voltage of 3.3 V and an I/O voltage of 3.3 V, with 5-V compatibility. The MPC857T supports a maximum core speed of 100 MHz and a maximum external bus speed of 66 MHz.

The MPC857T incorporates the same embedded processor core and similar CPM and SIU as the MPC8XX family. The MPC857T features one 10/100 Fast Ethernet controller module. The CPM supports one SCC (SCC1), two SMCs (SMC1 and SMC2), SPI and I^2C. The SCC can support 802.3 Ethernet, ATM, HDLC/SDLC, UART, and transparent protocols.

Figure 2 shows the MPC857T block diagram.

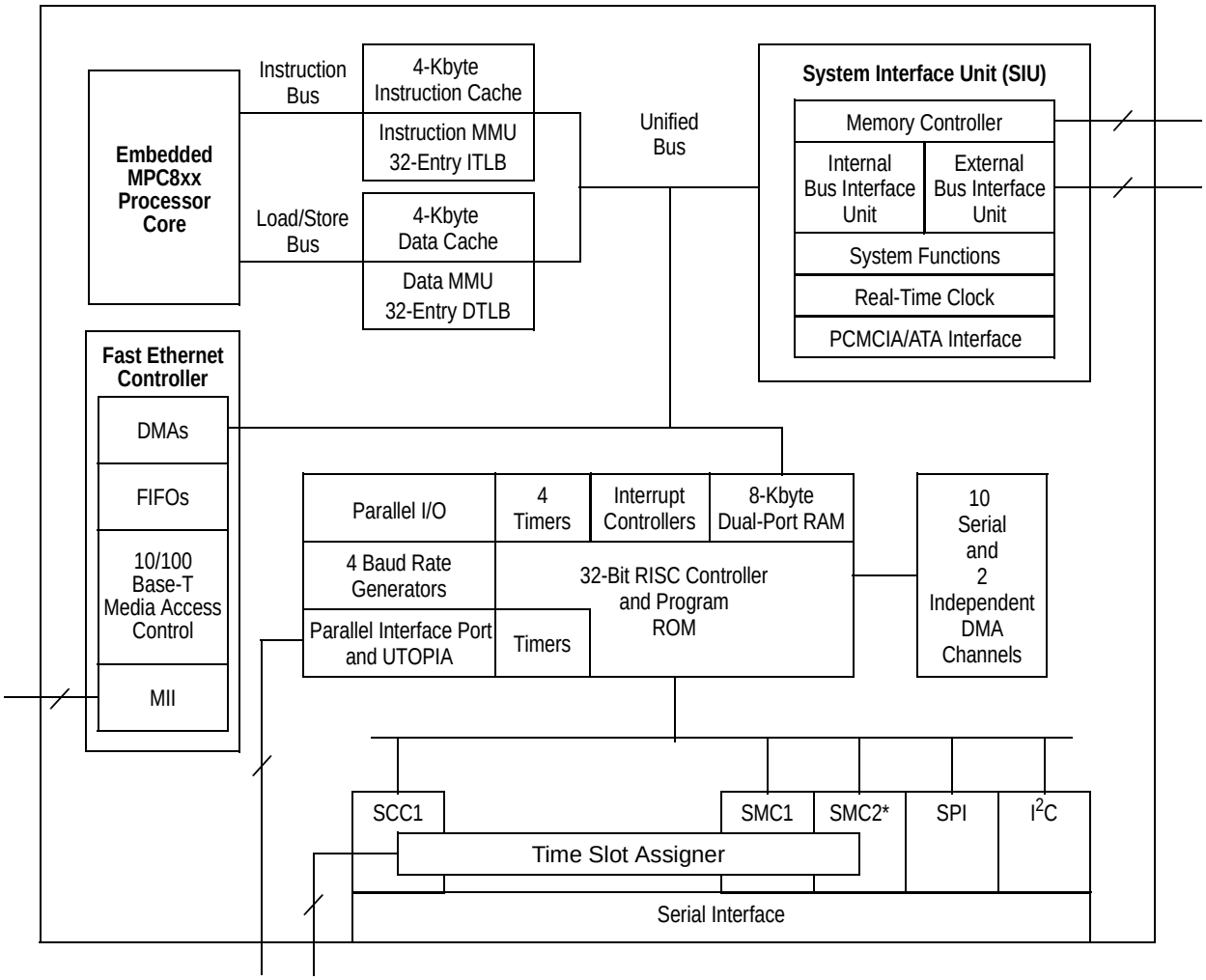


Figure 2. MPC857T Block Diagram

5 Similarities and Differences between MPC857T and MPC885

The following sections discuss pinout and memory mapping differences for the MPC857T and the MPC885.

5.1 Pinout

Both the MPC857T and the MPC885 use the 357 plastic ball grid array (PBGA) package. Buses and other functions are grouped in a logical order, but reuse of layout is not available. Parallel ports changed from four (Port A, B, C, and D) on the MPC857T to five (Port A, B, C, D, and E) on the MPC885. Each signal in the I/O ports can be configured as a general-purpose I/O signal or as a signal dedicated to supporting communications peripherals, such as Ethernet or USB. See the *MPC885 PowerQUICC Family Reference Manual* for more information.

Figure 3 shows the MPC885 pinout.

NOTE: This is the top view of the device.

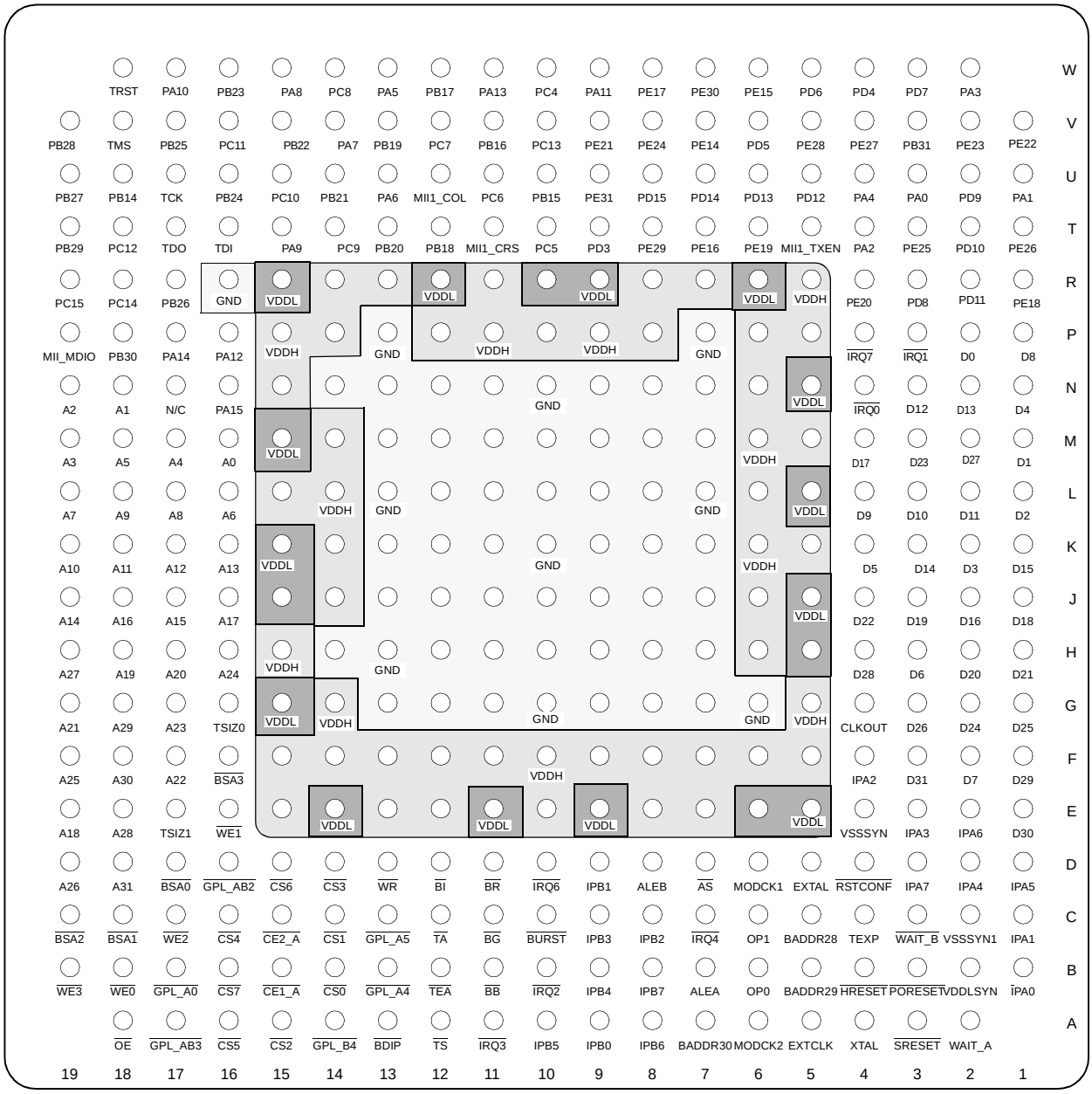


Figure 3. MPC885 Pinout

Figure 4 shows the MPC857T pinout.

NOTE: This is the top view of the device.

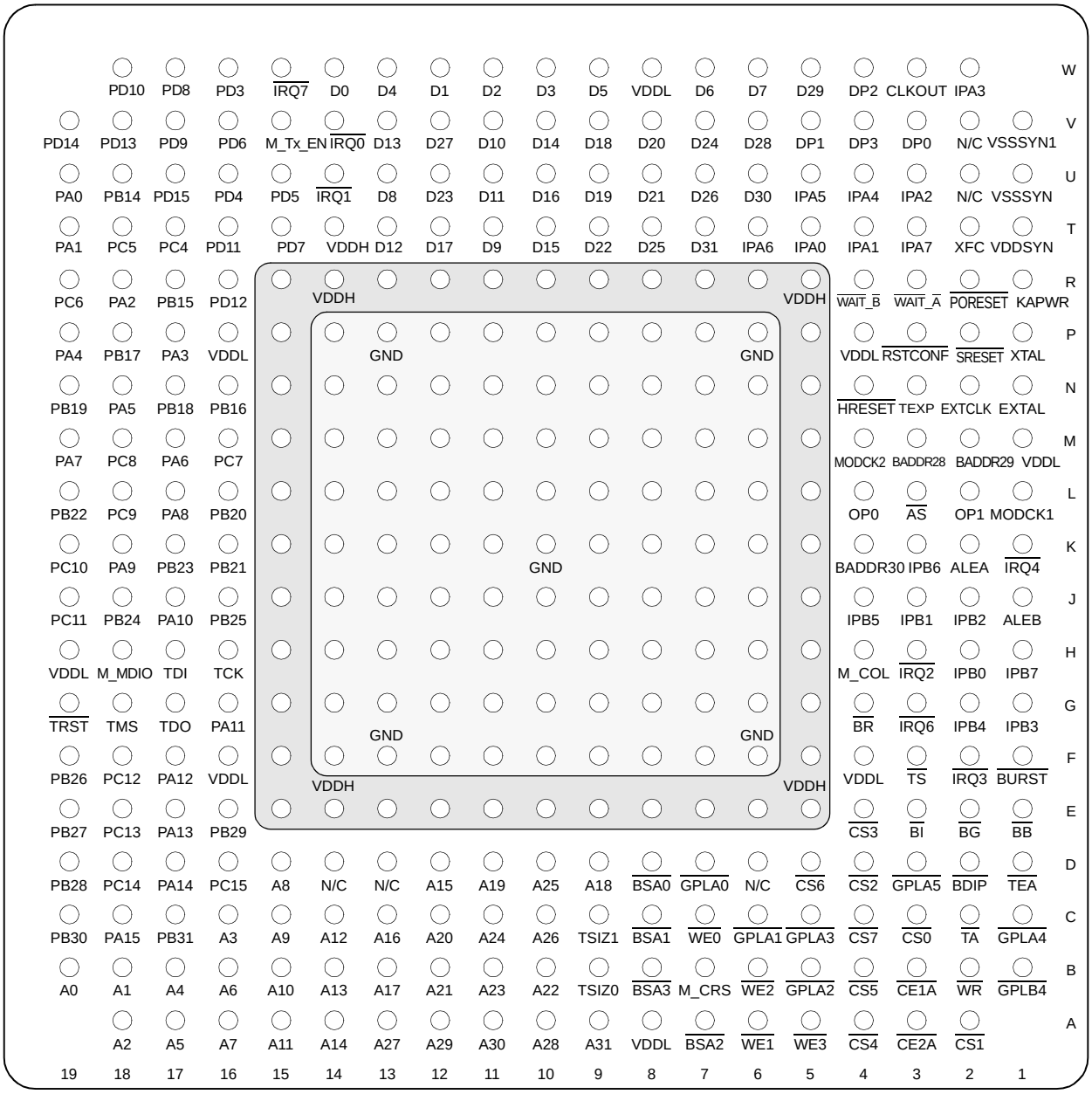


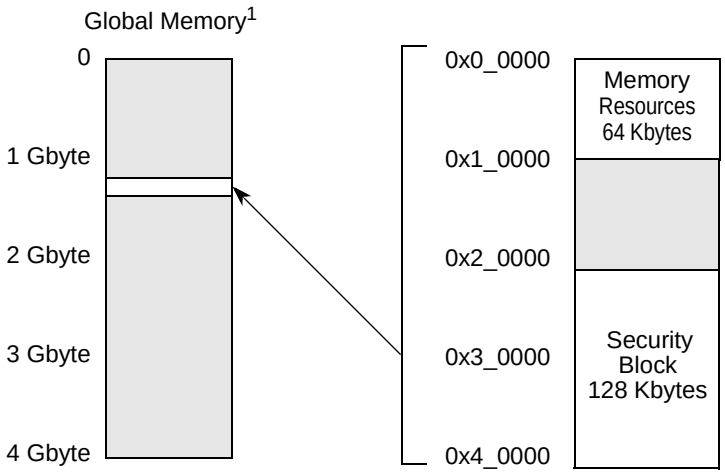
Figure 4. MPC857T Pinout

5.2 Memory Map

The memory maps for both the MPC857T and the MPC885 are very similar except for these differences:

- The SCC1 in the MPC857T is replaced with a USB 1.1 controller.
- Reserved space (offset 0xA20–0xA77) in the MPC857T is now for SCC2 and SCC3 in the MPC885.

- Port E registers in the MPC885 reside in a previously reserved area of the Port B registers in the MPC857T (starting at offset 0xAC8).
- The registers mapped for the FEC registers in the MPC857T are now mapped for FEC1 for the MPC885. The immediate reserved space following the FEC registers in the MPC857T is the location for the FEC2 registers in the MPC885 (starting at offset 0x1E00). For ease of porting, FEC2 registers are located in the same order as FEC1, with offset for FEC2 equal to FEC1 plus 0x1000.
- Dual-port RAM for both processors is from IMMR + 0x2000–0x2FFF, with expanded dual-port RAM from 0x3000–0x3BFF.
- The MPC857T's memory resources are mapped to a contiguous 64 Kbyte block; the MPC885's memory resources are mapped to a contiguous 256 Kbyte block, as shown in Figure 5, that includes the security block in the upper 128 Kbytes.
- Bits 14–15 in the 16-bit field IMMR[ISB] have new meaning in the MPC885. When IMMR[ISB] bits 14–15 are cleared, the internal memory map is the same as in the MPC857T. When IMMR[14–15] = 10, an additional 128 Kbyte memory block becomes available for the security engine, as shown in Figure 5.



1 Location of contiguous 256-Kbyte block of internal memory resources in this figure is for illustration only. The addresses shown are offsets from the IMMR.

Figure 5. MPC885 Memory Map

6 New Features for the MPC885

The following sections discuss the new features of the MPC885.

6.1 Hardware Changes

The following are the hardware changes from the MPC857T to the MPC885.

- There is no data parity generation/checking.
- The MPC885 only supports normal high and normal low power modes.

6.2 Digital Phase Lock Loop

The MPC885 features a digital phase lock loop (DPLL). The main purpose of the DPLL is to generate a stable reference frequency by multiplying the frequency and eliminating the clock skew. The DPLL allows the processor to operate at a high internal clock frequency using a low frequency clock input, providing two advantages. First, lower frequency clock input reduces the overall electromagnetic interference generated by the system. Second, the programmability of the oscillator enables the system to operate at a variety of frequencies with only a single external clock source. To ease the transition from the MPC857T phase lock loop (PLL) to the DPLL, a tool that calculates DPLL settings is available on the MPC885 product summary page at www.freescale.com. The major migration concerns regarding the DPLL are as follows:

- Input clock requirements are different
- Configuration of MODCK[1:2] has changed
- DPLL does not start to lock until the negation of $\overline{\text{POREST}}$ has occurred

For a detailed description of these items, please refer to the *MPC885 PowerQUICC Family Reference Manual*.

6.3 Security Engine

The block diagram of the security engine's internal architecture is shown in Figure 6. The bus interface module is designed to transfer 32-bit words between the bus and any register inside the security engine core.

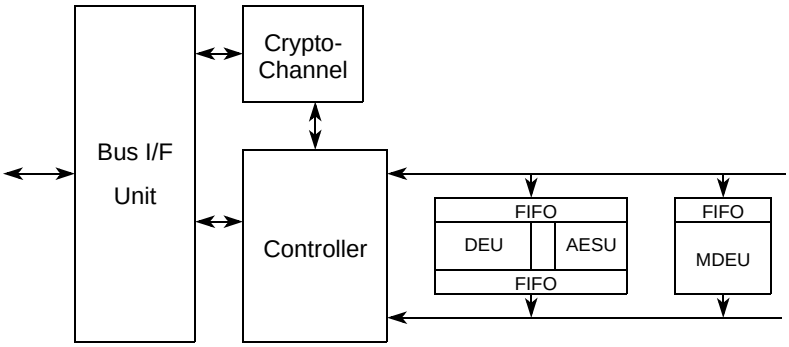


Figure 6. Security Engine Functional Blocks

An operation begins with a write of a pointer to the crypto-channel fetch register, which points to a data packet descriptor. The channel requests the descriptor and decodes the operation to be performed. The channel then asks the controller to assign crypto-execution units and fetch the keys, IVs, and data needed to perform the specific operation. The controller assigns execution units to the channel and makes requests to the master interface to satisfy the requests. As data is processed, it is written to the individual executions unit's output buffer and then back to system memory by means of the I/F module.

The internal registers for the security engine can be accessed when IMMR[14–15] = 10. The *MPC885 PowerQUICC Family Reference Manual* lists details of the registers and their locations in the internal memory map.

7 Summary

Although the migration from the MPC857T to the MPC885 requires layout and software changes, the benefits of an additional Fast Ethernet controller, USB 1.1, and an internal security engine may warrant the migration, depending on system requirements.

8 Revision History

Table 3 provides a revision history for this application note.

Table 3. Document Revision History

Revision	Date	Substantive Change(s)
0	10/13/2004	Initial release.

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