**Freescale Semiconductor**
Application Note

# PowerQUICC Design Checklist
## for PowerQUICC II Pro (MPC834x) Devices

*by    Networking and Multimedia Group
Freescale Semiconductor, Inc.
San Jose, CA*

This application note describes the generally recommended connections for new designs based on the Freescale Semiconductor MPC83*nn* processors:

- MPC8343E
- MPC8347E
- MPC8349E

The design checklist may also apply to future bus- or footprint-compatible processors. It can also serve as a useful guide to debugging a newly-designed system by highlighting those areas of a design that merit special attention during initial system startup.

For updates to this document, refer to the website listed on the back cover of this document.

**Contents**

*freescale*™
semiconductor

# 1 PowerQUICC II Pro Resources

This section describes resources provided to simplify the first phase of design. Before designing a system with a PowerQUICC II Pro device, become familiar with the available documentation, software, models, and tools.

## 1.1 References

Some references listed here may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

- Collateral
  - *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual* (MPC8349ERM)
  - *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Chip Errata* (MPC8349ECE)
  - *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications* (MPC8349EEC)
  - *MPC8347E PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications* (MPC8347EEC)
  - *MPC8343E PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications* (MPC8343EEC)
- Tools
  - Boot sequencer generator tool
  - UPM programming tool
- Models
  - IBIS
  - BSDL, Rev. 1.1 and Rev. 3.0 silicon

## 1.2 Device Errata

The device errata documents (MPC8349ECE, MPC8347ECE, MPC8343ECE) describe the latest fixes and work arounds for the PowerQUICC II Pro family of devices. Carefully study these documents before starting a design with the respective PowerQUICC II Pro device.

## 1.3 Boot Sequencer Tool

The PowerQUICC II Pro boot sequencer allows configuration of any memory-mapped register before power-on reset (POR) completes. The register data to be changed is stored in an $I^2C$ EEPROM. The PowerQUICC II Pro requires a particular data format for register changes as outlined in the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*. The boot sequencer tool is a C code file. When compiled and given a sample data file, it generates the appropriate raw data format as outlined in the MPC8349E reference manual; that is, an s-record file that can be used to program the EEPROM.

## 1.4 UPM Programming Tool

The UPM programming tool GUI is a user-friendly interface for programming all three PowerQUICC II Pro UPM machines. The GUI consists of a wave editor, table editor, and report generator. The user can directly edit the waveform or RAM array. Then the report generator prints out the UPM RAM array for use in a C program.

The UPM programming tool can be found on the MPC8349E, MPC8347E, or MPC8343E product page at the web site listed on the back cover of this document.

## 1.5 Available Training

Our third-party partners are part of an extensive Design Alliance Program. The current training partners can be found on our website under Design Alliance Program. Training material from past Smart Network Developer's Forums and Freescale Technology Forums are also available. These trainings modules are a valuable resource in understanding the PowerQUICC II Pro. This material is also available at our web site listed on the back cover of this document.

## 1.6 Product Revisions

**Table 1. PowerQUICC II Pro (MPC834*x*) Product Revisions**

| Device | Package | SVR (Rev. 1.0) | SVR (Rev. 1.1) | SVR (Rev. 3.0) | PVR (Rev. 1.0) | PVR (Rev. 1.1) | PVR (Rev. 3.0) |
|---|---|---|---|---|---|---|---|
| MPC8349E | TBGA | 8050_0010 | 8050_0011 | 8050_0030 | 8083_0010 | 8083_0011 | 8083_0030 |
| MPC8349 | TBGA | 8051_0010 | 8051_0011 | 8051_0030 | | | |
| MPC8347E | TBGA | 8052_0010 | 8052_0011 | 8052_0030 | | | |
| MPC8347 | TBGA | 8053_0010 | 8053_0011 | 8053_0030 | | | |
| MPC8347E | PBGA | 8054_0010 | 8054_0011 | 8054_0030 | | | |
| MPC8347 | PBGA | 8055_0010 | 8055_0011 | 8055_0030 | | | |
| MPC8343E | PBGA | 8056_0010 | 8056_0011 | 8056_0030 | | | |
| MPC8343 | PBGA | 8057_0010 | 8057_0011 | 8057_0030 | | | |

# 2 Power

This section provides design considerations for the PowerQUICC II Pro power supplies, as well as power sequencing. For information on PowerQUICC II Pro AC and DC electrical specifications and thermal characteristics, refer to MPC8349EEC, MPC8347EEC, and MPC8343EEC. For power sequencing recommendations, refer to Section 2.2, "Power Consumption."

## 2.1 Power Supply

The PowerQUICC II Pro has a core voltage, $V_{DD}$, which operates at a lower voltage than the I/O voltages $GV_{DD}$, $LV_{DD}$, and $OV_{DD}$. The $V_{DD}$ should be supplied through a variable switching supply or regulator to allow for compatibility with core voltage changes on future silicon revisions. The core voltage, 1.2 V

($\pm5\%$), is supplied across $V_{DD}$ and GND. The PowerQUICC II Pro I/O blocks are supplied with the following voltages:

- 2.5 V ($\pm5\%$) or 1.8 V ($\pm5\%$) across $GV_{DD}$ and GND
- 2.5 V ($\pm5\%$) or 3.3 V ($\pm10\%$) across $LV_{DD}$ and GND
- 3.3 V ($\pm10\%$) across $OV_{DD}$ and GND.

Typically, these voltages are supplied by simple linear regulators. This increases the complexity of the system because multiple voltage supplies and PCB power planes are required for the design. No external signals on PowerQUICC II Pro are 5-V tolerant. All input signals must meet the $G/L/OV_{IN}$ DC specification of the respective I/O block. See Table 2.

**Table 2. Power Supplies**

| Type | Name | Block | Recommended Value | Maximum Value (V) |
|------|------|-------|-------------------|-------------------|
| Core | $V_{DD}$ | e300 core voltage | 1.2 V ± 60 mV | 1.32 |
| PLL | $AV_{DD}$ | PLL supply voltages (e300, system, DDR, and LBIU PLLs) | 1.2 V ± 60 mV | 1.32 |
| I/O | $GV_{DD}$ | DDR DRAM I/O supply voltage | 2.5 V ± 125 mV<br>1.8V ± 90 mV | 2.75<br>1.98 |
| I/O | $LV_{DD1}$ | TSEC 1 and Ethernet Management Interface I/O supply voltages | 3.3 V ± 330 mV<br>2.5 V ± 125 mV | 3.63<br>2.75 |
| I/O | $LV_{DD2}$ | TSEC 2 I/O supply voltage | 3.3 V ± 330 mV<br>2.5 V ± 125 mV | 3.63<br>2.75 |
| I/O | $OV_{DD}$ | PCI, local bus, DUART, system control and power management, I$^2$C, and JTAG I/O voltage | 3.3 V ± 330 mV | 3.63 |

**NOTE**

For Revision 1.x devices, $LV_{DD1}$ and $LV_{DD2}$ are internally tied together and must be powered from the same I/O voltage supply. For Revision 3.0 devices, $LV_{DD1}$ and $LV_{DD2}$ can be powered from different I/O voltage supplies.

## 2.2 Power Consumption

The MPC8349EEC, MPC8347EEC, and MPC8343EEC hardware specifications estimate the power dissipation of $V_{DD}$ for various configurations of the coherent system bus (CSB) and the e300 core frequencies. Suitable thermal management is required to ensure that the junction temperature does not exceed the maximum specified value.

The typical numbers in these hardware specifications include dissipation for all blocks except the PLL supplies and I/Os, which must be added for an accurate assessment of whether a heat sink or other chip

cooling mechanism is required. Table 3 provides estimated I/O power numbers for the DDR, PCI, local bus, TSEC, and USB.

**Table 3. I/O Power Consumption Estimates**

| Interface | Parameters | $GV_{DD}$ (2.5 V) | $OV_{DD}$ (3.3 V) | $LV_{DD}$ (3.3 V) | $LV_{DD}$ (2.5 V) | Unit | Comments |
|---|---|---|---|---|---|---|---|
| DDR I/O 65% utilization Rs = 20 Ω Rt = 50 Ω sympathy | 200 MHz, 32-bit | 0.42 | — | — | — | W | — |
| | 266 MHz, 32-bit | 0.55 | — | — | — | W | — |
| | 300 MHz, 32-bit | 0.61 | — | — | — | W | — |
| | 333 MHz, 32-bit | 0.67 | — | — | — | W | — |
| | 200 MHz, 64-bit | 0.51 | — | — | — | W | — |
| | 266 MHz, 64-bit | 0.66 | — | — | — | W | — |
| | 300 MHz, 64-bit | 0.74 | — | — | — | W | — |
| | 333 MHz, 64-bit | 0.82 | — | — | — | W | — |
| PCI I/O Load = 30 pF | 33 MHz, 32-bit | — | 0.04 | — | — | W | Multiply by 2 if using two 32-bit ports |
| | 66 MHz, 32-bit | — | 0.07 | — | — | W | |
| | 33 MHz, 64-bit | — | 0.08 | — | — | W | — |
| | 66 MHz, 64-bit | — | 0.14 | — | — | W | — |
| Local bus I/O Load = 25 pF | 133 MHz, 32-bit | — | 0.27 | — | — | W | — |
| | 83 MHz, 32-bit | — | 0.17 | — | — | W | — |
| | 66 MHz, 32-bit | — | 0.14 | — | — | W | — |
| | 50 MHz, 32-bit | — | 0.11 | — | — | | — |
| TSEC I/O | MII | — | — | 0.01 | — | W | Multiply by 2 if using both TSECs |
| | GMII or TBI | — | — | 0.06 | — | W | |
| | RGMII or RTBI | — | — | — | 0.04 | W | |
| USB | 12 MHz | — | 0.01 | — | — | W | — |
| | 480 MHz | — | 0.20 | — | — | W | — |
| Other I/O | — | — | 0.01 | — | — | W | — |

## 2.3  Power Sequencing

When power is initially applied to multiple power supplies, the voltage rails ramp up at different rates. These rates depend on the power supply, the type of load on each power supply, and the way different voltages are derived. However, advances in the PowerQUICC II Pro ESD design allow flexibility in the order in which power rails ramp up, as long as the supplies do not exceed absolute maximum ratings (as

**PowerQUICC Design Checklist,  Rev. 10**

defined in the device-specific hardware specifications). The MPC834x does not require the core supply voltage and I/O supply voltages to be applied in any particular order.

### NOTE

From a system standpoint, if the I/O power supplies ramp up before the $V_{DD}$ core supply stabilizes, there may be a period of time when the I/O pins are driven to a logic one or logic zero state. After the power is stable, as long as $\overline{PORESET}$ is asserted, most IP pins are tri-stated. To minimize the time that I/O pins are actively driven, apply core voltage before I/O voltage and assert $\overline{PORESET}$ before the power supplies fully ramp up.

Table 2 shows the current maximum ratings for the power supplies. Supplies must not exceed these absolute maximum ratings. However, during normal operation, use of the recommended operating conditions presented in the hardware specifications is recommended. Any information in the relevant hardware specifications supersedes information in Table 2.

## 2.4    Power Planes

Each $V_{DD}$ pin should be provided with a low-impedance path to the board power supply. Similarly, each ground pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on-chip. The capacitor leads and associated printed-circuit traces connecting to chip $V_{DD}$ and ground should be kept to less than half an inch per capacitor lead.

## 2.5    Decoupling

Due to large address and data buses and high operating frequencies, the PowerQUICC II Pro can generate transient power surges and high-frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PowerQUICC II Pro system, and it requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each $V_{DD}$, $GV_{DD}$, $LV_{DD}$, and $OV_{DD}$ pin. These decoupling capacitors should receive their power from separate $V_{DD}$, $GV_{DD}$, $LV_{DD}$, $OV_{DD}$, and GND power planes in the PCB, using short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Other capacitors can surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance.

In addition, several bulk storage capacitors should be distributed around the PCB, feeding the $V_{DD}$, $GV_{DD}$, $LV_{DD}$, and $OV_{DD}$ planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure quick response time. They should also connect to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100–300 µF.

Use simulation to minimize noise on the power supplies before proceeding into the PCB design and manufacturing stage of development.

## 2.6    PLL Power Supply Filtering

Each PowerQUICC II Pro PLL gets power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, respectively). The $AV_{DD}$ level should always equal $V_{DD}$, and preferably be derived directly from $V_{DD}$ through a low frequency filter scheme.

There are several reliable ways to provide power to the PLLs, but the recommended solution is to use four independent filter circuits as illustrated in Figure 1, one to each of the four $AV_{DD}$ pins, thus reducing noise injection from one PLL to the other. This circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with a minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended instead of a single large value capacitor.

Place each circuit as closely as possible to the specific $AV_{DD}$ pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the $AV_{DD}$ pin, which is on the periphery of the package, without the inductance of vias. Figure 1 shows the PLL power supply filter circuit.
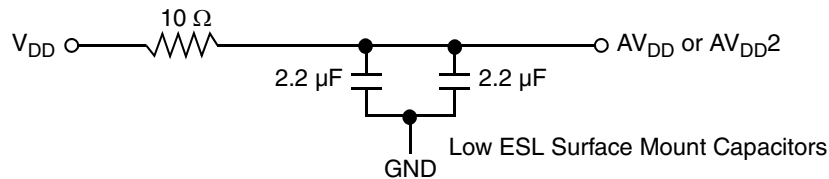


**Figure 1. PLL Power Supply Filter Circuit**

Table 4 summarizes the power signal pins.

**Table 4. Power Signal Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection If Used | Connection If Not Used | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | **Power Signals** | | | | | | | | |
| | $AV_{DD1}$ | — | X | X | X | X | 1.2 V ± 60 mV | | Power for e300 PLL |
| | $AV_{DD2}$ | — | X | X | X | X | 1.2 V ± 60 mV | | Power for system PLL |
| | $AV_{DD3}$[1] | — | X | X | X | X | 1.2 V ± 60 mV | | Power for DDR DLL |
| | $AV_{DD4}$ | — | X | X | X | X | 1.2 V ± 60 mV | | Power for LBIU DLL |
| | $GV_{DD}$ | — | X | X | X | X | 2.5 V ± 125 mV | | Power for DDR I/O voltage |
| | $LV_{DD1}$ | — | X | X | X | X | 2.5 V ± 125 mV 3.3 V ± 330 mV | | Power for TSEC1 and management interface |
| | $LV_{DD2}$ | — | X | X | X | X | 2.5 V ± 125 mV 3.3 V ± 330 mV | | Power for TSEC2 |
| | $V_{DD}$ | — | X | X | X | X | 1.2 V ± 60 mV | | Power for the core |

**Table 4. Power Signal Pin Listing (continued)**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | $OV_{DD}$ | — | X | X | X | X | 3.3 V ± 330 mV | Power for PCI, 10/100 Ethernet and other standard |
| | MVREF[1:2] | I | X | X | X | X | — | DDR reference voltage |

[1] DDR DLL not supported. In Revision 3.x, AVDD3 (AF9 in PBGA and AE1 in TBGA) should be NC. However, customers who are migrating from Revision 1.x to Revision 3.x using the existing board layout can leave these pins connected to 1.2 V. No layout change is required.

# 3 Clocking

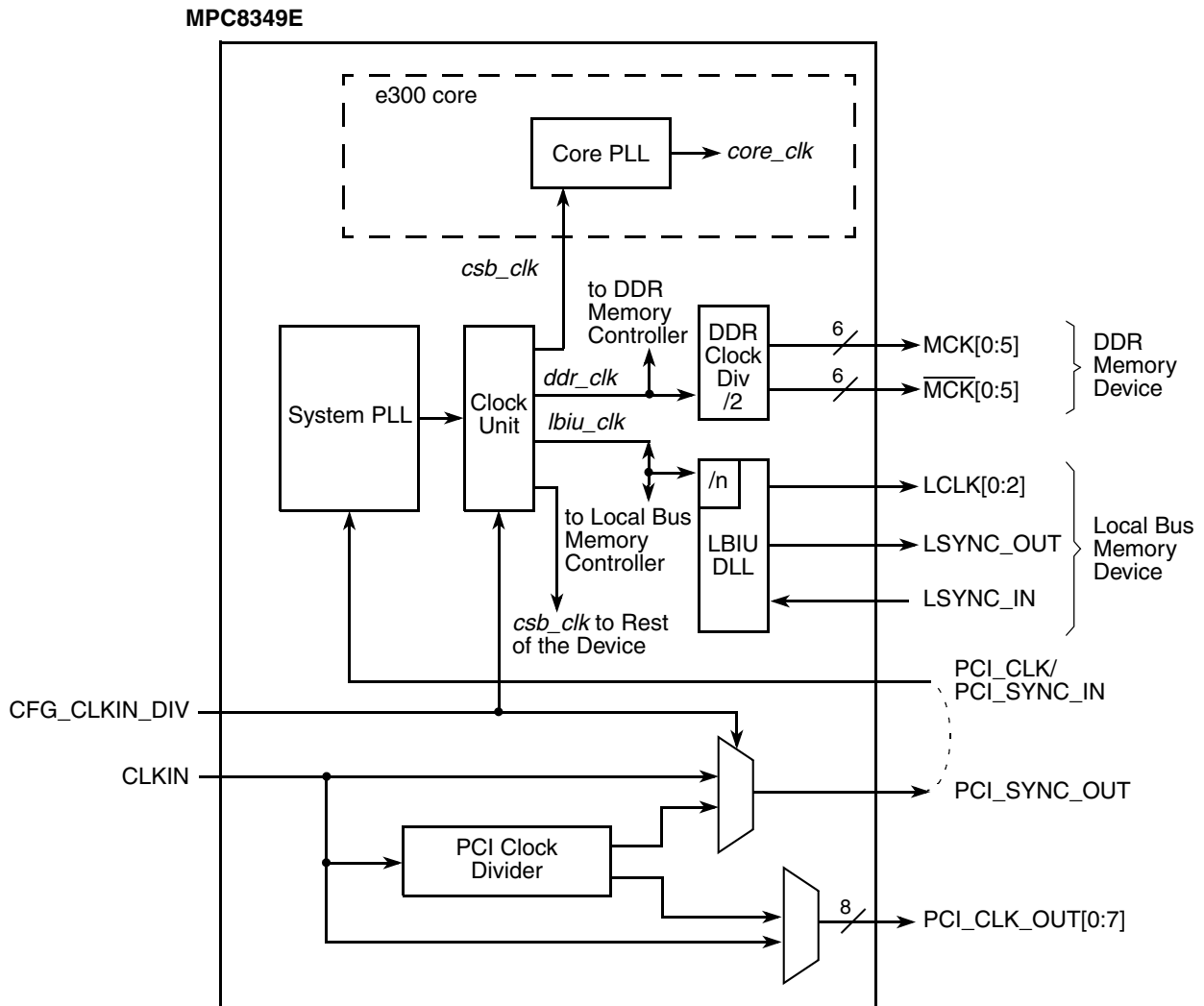Figure 2 shows the internal distribution of clocks within the MPC8349E.



**Figure 2. Clock Subsystem Block Diagram**

The primary clock source for the MPC8349E is one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured as a PCI host or PCI agent.

**NOTE**

The MPC8349E has eight PCI clock output signals. The MPC8347E and MPC8343E has only five PCI clock output signals (PCI_CLK_OUT[0:4]).

The system clock input is multiplied by a PLL to generate the coherent system bus (CSB) clock. The CSB provides a clock to the various logic blocks on-chip. It is divided by two to generate the DDR clocks, MCK[0:5]. It is divided by 2/4/8 (in the LCRR[CLKDIV] register) to generate local bus clocks, LCLK[0:2]. It is also multiplied by a second PLL (by the RCWH[COREPLL] power-on reset value) to generate the e300 core clock. See Table 5.

There are no default settings for the two PowerQUICC II Pro PLLs, so they must be configured at power-on reset. Set the appropriate fields of the hardware reset configuration words.

**Table 5. Clocking Quick Reference**

| Functional Block | Clock Derivation |
|---|---|
| csb_clk (System clock) | [CLKIN *or* PCI_CLK] × [2–16] |
| e300 core (***coreclk***) | ***csb_clk*** × [1, 1.5, 2, 2.5, 3] |
| DDR (***MCLK***) | ***csb_clk*** ÷ 2 |
| Local bus | ***csb_clk*** ÷ [2, 4, 8] |
| PCI1 clock | CLKIN *or* CLKIN ÷ 2 |
| PCI2 clock | CLKIN *or* CLKIN ÷ 2 |
| TSEC1/TSEC2 | 125 MHz external clock |
| $I^2C$ | ***csb_clk*** ÷ (I2CFDR ratio) |
| USB | 60 MHz/30 MHz External clock from PHY |
| Real time clock | External clock |

## 3.1   System Clock in PCI Host Mode

When the PowerQUICC II Pro is configured as a PCI host device (RCWH[PCIHOST] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the PCI_SYNC_OUT and PCI_CLK_OUT multiplexors. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN ÷ 2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT connects externally to PCI_SYNC_IN so that the internal clock subsystem can synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

## 3.2 System Clock in PCI Agent Mode

When the PowerQUICC II Pro is configured as a PCI agent device, PCI_CLK is the primary input clock. In agent mode, the CLKIN signal should be tied to GND, and the clock output signals, PCI_CLK_OUT$n$ and PCI_SYNC_OUT, are not used.

In agent mode, the CFG_CLKIN_DIV configuration input can be used to double the internal clock frequencies, if sampled as 1 during PORESET assertion. This feature is useful if a fixed internal frequency is desired, regardless of whether the PCI clock is running at 33 or 66 MHz. PCI specifications require the PCI clock frequency information to be provided by the M66EN signal.

## 3.3 Clocking Example

To maximize the frequencies of certain key interfaces, use the following inputs:

- **CLKIN** = 66.67 MHz
- **CFG_CLKIN_DIV** (pin is pulled low) = 0
- CSB multiplier *(HRCW[SPMF])* = 5
- Core multiplier *(HRCW[COREPLL])* = 2
- Local bus divider *(LCRR[CLKDIV])* = 4

The resulting frequencies for the following interfaces are:

- *csb_clk* = CLKIN $\times$ SPMF $\times$ (1 + CFG_CLKIN_DIV) = **333 MHz**
- *core_clk* = *csb_clk* $\times$ COREPLL = **667 MHz**
- **MCLK** = *csb_clk* $\div$ 2 = **167 MHz** (333 MHz data rate)
- **LCLKn** = *csb_clk* $\div$ 4 = **83.25 MHz**
- **PCI_CLK** = CLKIN = **66 MHz**

These are the current maximum frequencies of certain key interfaces. Check the relevant product website for updated options.

Table 6 summarizes the clock signal pins.

**Table 6. Clock Signal Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | | | | | Clocks | | | | |
| | PCI_CLK_OUT[0:4] | O | X | X | X | X | As needed | Open | • **Device as PCI host:** Functions as PCI output clock banks. OCCR register determines if clocks are set as CLKIN or CLKIN $\div$ 2.<br>• **Device as PCI agent:** These signals are not used. |

**Table 6. Clock Signal Pin Listing  (continued) (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | PCI_CLK_OUT[5:7] | O | — | — | — | X | As needed | Open | • **Device as PCI host:** Functions as PCI output clock banks. OCCR register determines if clocks are set as CLKIN or CLKIN÷2. <br>• **Device as PCI agent:** These signals are not used. |
| X | PCI_SYNC_IN/ PCI_CLK | I | X | X | X | X | As needed | Always connected | • **Device as PCI host:** Functions as PCI_SYNC_IN. Connect externally to PCI_SYNC_OUT. <br>• **Device as PCI agent:** Functions as PCI_CLK. A valid 25–66.67 MHz clock signal (at $OV_{DD}$ level) must be applied to this signal when used. |
| X | PCI_SYNC_OUT | O | X | X | X | X | Connect to PCI_SYNC_IN | Open | • **Device as PCI host:** Connect externally to PCI_SYNC_IN signal for de-skewing of external PCI clock routing. Loop trace should match with PCI_CLK_OUTx signal traces. <br>• **Device as PCI agent:** This signal is not used. |
| | RTC/PIT_CLOCK | I | X | X | X | X | Tie to 32.768 kHz crystal | 1 k–4.7 kΩ to GND | Real-time clock/periodic interval timer input from external 32.768 kHz crystal. |
| X | CLKIN | I | X | X | X | X | Connect to 25–66.67 MHz clock signal | 1 k–4.7 kΩ to GND | Clock input when configured in PCI host mode. A valid 25–66.67 MHz clock signal (at $OV_{DD}$ level) must be applied to this signal when used. |

# 4    Power-On Reset and Reset Configurations

A detailed power-on reset flow is as follows:

1. Power to the device is applied.
2. The system asserts $\overline{PORESET}$ (and optionally $\overline{HRESET}$) and $\overline{TRST}$ initializing all registers to their default states.
3. The system applies a stable CLKIN (PCI host mode) or PCI_CLK (PCI agent mode) signal and stable reset configuration inputs (CFG_RESET_SOURCE, CFG_CLKIN_DIV).
4. The system negates $\overline{PORESET}$ after at least 32 stable CLKIN or PCI_CLK clock cycles.
5. The device samples the reset configuration input signals to determine the clock division and the reset configuration words source.

6. The device starts loading the reset configuration words. When the reset configuration word low is loaded, the system PLL begins to lock. When the system PLL is locked, the *csb_clk* is supplied to the e300 PLL.

7. The e300 PLL begins to lock.

8. The device drives $\overline{\text{HRESET}}$ asserted until the e300 PLL is locked and until the reset configuration words are loaded.

9. If enabled, the boot sequencer loads configuration data from the serial ROMs as described in the *MPC8349E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.

## 4.1    Reset Configuration Signals

Various device functions of the PowerQUICC II Pro are initialized by sampling certain signals during the assertion of the $\overline{\text{PORESET}}$ signal after a stable clock is supplied. These inputs are either pulled high or low. While these pins are generally output pins during normal operation, they are treated as inputs while $\overline{\text{PORESET}}$ is asserted.

The CFG_RESET_SOURCE[0:2] input signals are sampled during the assertion of $\overline{\text{PORESET}}$ to select the interface to load the reset configurations words:

- $\text{I}^2\text{C}$-1 interface
- A device (that is, CPLD, EEPROM, or Flash) on the local bus
- From an internally-defined word value. See Table 7.

**Table 7. Reset Configuration Word Source**

| Reset Configuration Signal Name | Value (Binary) | Meaning |
|---|---|---|
| CFG_RESET_SOURCE[0:2] | 000 | Reset configuration words are loaded from a device on the local bus. |
| | 001 | Reset configuration words are loaded from a device on $\text{I}^2\text{C}$-1. PCI_CLK/PCI_SYNC_IN is in the range of 25–44 MHz. This option will be removed from future designs. Thus, it is recommended to use the 010 option. |
| | 010 | Reset configuration word is loaded from a device on $\text{I}^2\text{C}$-1. PCI_CLK/PCI_SYNC_IN is in the range of 25–66.67 MHz. |
| | 011–111 | Hard coded options 0–4. |

The CFG_CLKIN_DIV input signal is also sampled during the assertion of $\overline{\text{PORESET}}$ to determine the relationship between CLKIN and PCI_SYNC_OUT. See Table 8.

**Table 8. CLKIN Divisor Configuration**

| Reset Configuration Signal Name | Value (Binary) | Meaning |
|---|---|---|
| CFG_CLKIN_DIV | 0 | In PCI host mode:<br>• CLKIN:PCI_SYNC_OUT = 1:1<br>• *csb_clk* = (PCI_SYNC_IN × SPMF)<br>• All PCI_CLK_OUT clocks are limited to the CLKIN frequency.<br>In PCI agent mode:<br>• *csb_clk* = (PCI_CLK × SPMF) |
| | 1 | In PCI host mode:<br>• CLKIN:PCI_SYNC_OUT = 2:1<br>• *csb_clk* = (PCI_SYNC_IN × 2 × SPMF)<br>• The PCI_CLK_OUT clocks may be programmed to CLKIN or CLKIN÷2 in the OCCR register.<br>In PCI agent mode:<br>• *csb_clk* = (PCI_CLK × 2 × SPMF) |

## 4.2    Reset Configuration Words

The reset configuration words control the clock ratios and other basic device functions such as PCI host or agent mode, boot location, TSEC modes, and endian mode. The reset configuration words are loaded from the local bus or from the I$^2$C interface during the power-on or hard reset flows.

If the HRCW is loaded through the local bus, the LA[27:31] pins are used and not the LAD[27:31] pins. The LAD[27:31] pins are not driven during HRCW loading. Only the LA[27:31] increment during the load of the HRCW. In essence, the device does a type of burst access to the flash memory when it loads the HRCW. It drives the high-order bits of the address on LAD[0:26], which is also the first address in a 4-byte sequence, asserts LALE, latches the first byte, and then increments LA[27:31] to get the next 3 bytes. It then drives the high-order bits for the second access, asserts LALE, latches a byte, and again increments the LA[27:31] to get the next 3 bytes. Out of reset, the LA[27:31] and LAD[27:31] mirror each other (while LALE is asserted).

For details on the reset configuration words, refer to the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*.

## 4.3    Useful System POR Debug Registers

The hardware reset configuration settings can be read in the reset configuration word low register (RCWLR), the reset configuration word high register (RCWHR), the reset status register (RSR), and the system PLL mode register (SPMR). For details, see the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*. Note that all of these resisters are read-only, except RSR.

## 4.4    Boot Sequencer

The boot sequencer provides the means to load the hardware reset configuration word and to configure any memory-mapped register before the boot-up code runs.

**PowerQUICC Design Checklist,  Rev. 10**

Reset configuration load mode is selected based on the settings of the CFG_RESET_SOURCE pins during the power-on reset sequence. The $I^2C$-1 interface loads the reset configuration words from an EEPROM at a specific calling address while the rest of the device is in the reset state. When the reset configuration words are latched inside the device, $I^2C$-1 is reset until $\overline{\text{HRESET}}$ is negated. Then the device is initialized using boot sequencer mode.

Boot sequencer mode is selected at power-on reset by the BOOTSEQ field in the reset configuration word high register (RCWH). If the boot sequencer mode is selected, the $I^2C$ module communicates with one or more EEPROM through the $I^2C$-1 interface to initialize one or more configuration register of the PowerQUICC II Pro. For example, this code can be used to configure the port interface registers if the device is booting from the PCI. Refer to the *MPC8349E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for the complete data format for programming the $I^2C$ EEPROM.

The boot sequencer contains a basic level of error detection. If the $I^2C$ boot sequencer fails while loading the reset configuration words are loaded, RSR[BSF] is set. If a preamble or CRC fail is detected in boot sequencer mode, there is no internal or external indication that the boot sequencer operation failed Use one of the GPIO pins for that purpose.

Table 9 summarizes the reset configuration pins.

**Table 9. Reset Configuration Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| **System Control** | | | | | | | | |
| X | $\overline{\text{PORESET}}$ | I | X | X | X | X | As needed + 2 k–10 kΩ to $OV_{DD}$ | | Using a pull-up depends on voltage monitor used in design. If the voltage monitor uses an open-drain output, a pull-up is needed. If an active output is used, a pull-up may not be needed |
| X | $\overline{\text{HRESET}}$ | I/O | X | X | X | X | As needed + 1 k–4.7 kΩ to $OV_{DD}$ | | Open-drain signal. Output during power-on and hard reset flows. Input after reset flow completes. |
| X | $\overline{\text{SRESET}}$ | I/O | X | X | X | X | As needed + 1 k–4.7 kΩ to $OV_{DD}$ | | Open-drain signal. Output during power-on, hard, and soft reset flows. Input after reset flow completes. |

**Table 9. Reset Configuration Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| X | LGPL0/LSDA10/ **cfg_reset_source0** | I/O | X | X | X | X | As needed | | • Input during power-on and hard reset flows, providing the reset configuration word source. Signal values should be driven by logic during power-on and hard reset flows OR through pull-up/down resistors (4.7 k$\Omega$ to OV$_{DD}$ or 1 k$\Omega$ to GND) • Functional output signal after reset flow completes. Pull-up/down resistors not needed. |
| X | LGPL1/$\overline{\text{LSDWE}}$/ **cfg_reset_source1** | I/O | X | X | X | X | As needed | | |
| X | LGPL3/$\overline{\text{LSDCAS}}$/ **cfg_reset_source2** | I/O | X | X | X | X | As needed | | |
| X | LGPL5/ cfg_clkin_div | I/O | X | X | X | X | **PCI host:** 1 k$\Omega$ to OV$_{DD}$ or 1 k$\Omega$ to GND  **PCI agent:** 1 k$\Omega$ to GND | 1 k$\Omega$ to GND | • Input during power-on and hard reset flows. • Functional signal after reset flow completes. |

# 5 JTAG and Debug

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 4. Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE® Std 1149.1 specification, but it is provided on all processors built on Power Architecture® technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ independently to control the processor fully. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 4 allows the COP port to assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ independently, while ensuring that the target can drive $\overline{\text{PORESET}}$ as well.

The COP interface has a standard header, shown in Figure 3, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 3 is common to all known emulators.

If the JTAG interface and COP header are not used, Freescale recommends all of the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{PORESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 4. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.

| | | | |
|---|---|---|---|
| COP_TDO | 1 | 2 | NC |
| COP_TDI | 3 | 4 | $\overline{\text{COP\_TRST}}$ |
| NC | 5 | 6 | COP_VDD_SENSE |
| COP_TCK | 7 | 8 | $\overline{\text{COP\_CHKSTP\_IN}}$ |
| COP_TMS | 9 | 10 | NC |
| $\overline{\text{COP\_SRESET}}$ | 11 | 12 | NC |
| $\overline{\text{COP\_HRESET}}$ | 13 | KEY No pin | |
| $\overline{\text{COP\_CHKSTP\_OUT}}$ | 15 | 16 | GND |

**Figure 3. COP Connector Physical Pinout**

**Figure 4. JTAG Interface Connection**
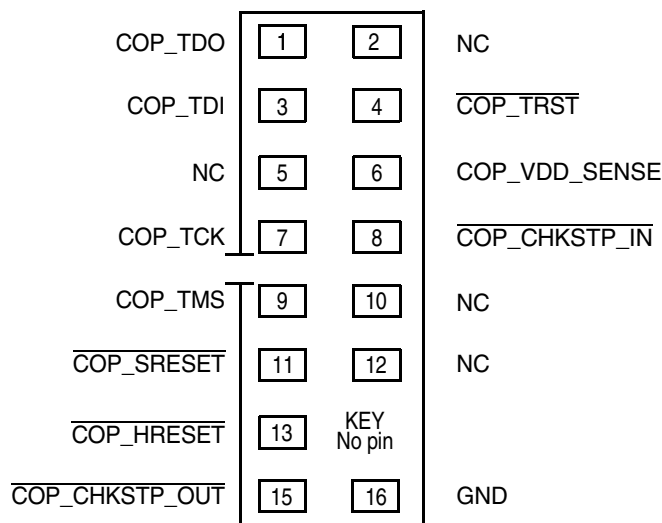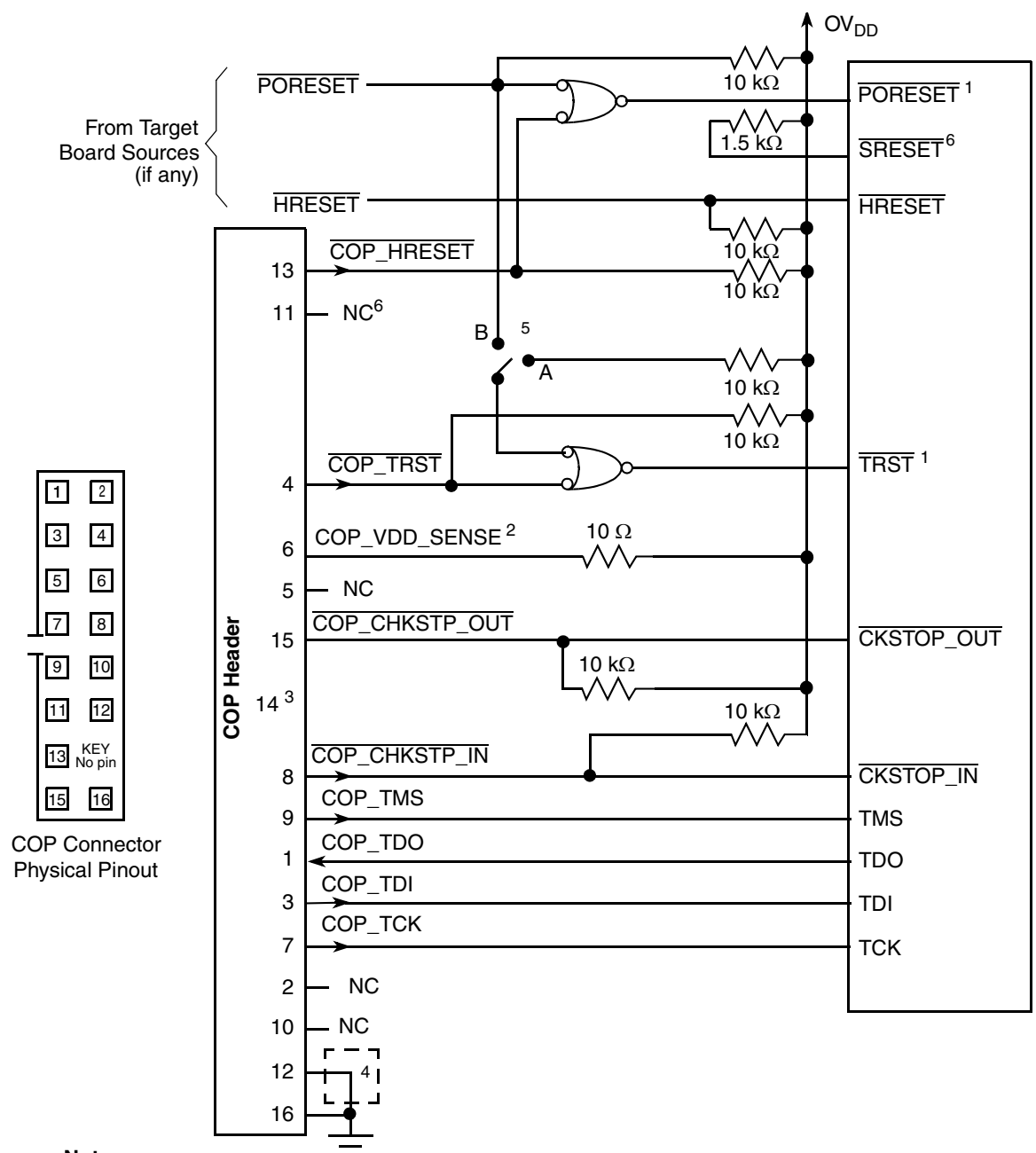
**Notes:**
1. The COP port and target board should be able to assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ independently to the processor to control the processor fully as shown here.
2. Populate this with a 10 $\Omega$ resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. See erratum RESET3 in *MPC8349ECE*.

**PowerQUICC Design Checklist, Rev. 10**

## 5.1 Debug Using In-Circuit Emulator

There may be issues when you use a JTAG-based in-circuit emulator to boot the PowerQUICC Pro II device as reset configuration words are sourced from an unprogrammed Flash device on the local bus. There is no valid RCW already present in Flash memory when the PowerQUICC II Pro device performs the $\overline{\text{PORESET}}$ sequence. The CPU core is disabled and the in-circuit emulator cannot take control of the CPU. The following methods allow an in-circuit emulator to attach to the CPU core and program a valid RCW into a Flash device on the local bus:

- If a CPLD (or other logic) is present, provide an option for the CPLD to provide the RCW during $\overline{\text{PORESET}}$.
- Design the board with logic that allows clocking for both PCI host and agent mode. Have the board boot in PCI agent mode using an internal hard-coded configuration source to provide the RCW.
- Use the $I^2C$-1 interface.

Table 10 summarizes the JTAG and TEST pins.

**Table 10. JTAG and TEST Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | | | | | | | **JTAG** | | |
| | TCK | I | X | X | X | X | As needed | | Commonly used for boundary scan testing. If pin is truly not used can tie directly to GND. |
| | TDI | I | X | X | X | X | As needed | | This JTAG pin has a weak internal pull-up P-FETs that is always enabled. |
| | TDO | O | X | X | X | X | As needed | | Actively driven during $\overline{\text{RESET}}$ |
| | TMS | I | X | X | X | X | As needed | | This JTAG pin has a weak internal pull-up P-FETs that is always enabled. |
| X | $\overline{\text{TRST}}$ | I | X | X | X | X | Tie to $\overline{\text{PORESET}}$ or Output of negative OR gate logic | | • This JTAG pin has a weak internal pull-up P-FETs that is always enabled.<br>• If an in-circuit emulator is used in the design, $\overline{\text{TRST}}$ should be tied to the output of negative OR gate logic. The inputs to the negative OR gate logic should be any external $\overline{\text{TRST}}$ sources and the $\overline{\text{PORESET}}$ signal. |
| | | | | | | | **Test** | | |
| | TEST | I | X | X | X | X | Tie directly to GND | | — |

**Table 10. JTAG and TEST Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | TEST_SEL | I | X | X | X | X | Tie directly to GND or 2 k–10 kΩ to $OV_{DD}$ | | • MPC8349 (TBGA package): This pin must be tied to GND.<br>• MPC8347 (TBGA package): This pin must be tied to $OV_{DD}$.<br>• MPC8347 (PBGA package): This pin must be tied to GND.<br>• MPC8343 (PBGA package): This pin must be tied to $OV_{DD}$. |
| **PMC** | | | | | | | | | |
| | QUIESCE | O | X | X | X | X | As needed | Open | — |
| **Thermal Management** | | | | | | | | | |
| | THERM0 | I | X | X | X | X | As needed | Open | Thermal sensitive resistor |

# 6 Functional Blocks

This section presents the recommendations and guidelines for designing with various functional blocks on the PowerQUICC II Pro.

## 6.1 PCI Bus Interface

The reset configuration word high controls the hardware configuration of the PCI blocks as follows:

- RCWH[PCIHOST]—Host/agent mode for PCI-1. In PCI agent mode, only PCI1 is enabled. PCI2 cannot be used.
- RCWH[PCI64]—Configures one 64-bit PCI interface using PCI1 or two 32-bit PCI interfaces. This field must be set to 0 for MPC8347 and MPC8343 designs.
- RCWH[PCI1ARB]—PCI1 internal/external arbiter mode select.
- RCWH[PCI2ARB]—PCI2 internal/external arbiter mode select.

As Table 11 shows, signals of the PCI1 interface are multiplexed with the CompactPCI Hot Swap pins. Either PCI1 or Hot Swap functionality is selected by the RCWH[PCI1ARB] bit setting. When an external arbiter is selected (RCWH[PCI1ARB] = 0), the CompactPCI Hot Swap pins function. When an internal arbiter is selected (RCWH[PCI1ARB] = 1), the $\overline{GNT}x/\overline{REQ}x$ pins function.

Some signals of the PCI2 interface on the MPC8349 are multiplexed with GPIO2 pins. Either PCI2 or GPIO2 functionality is selected by the setting of the HRCW[PCI64] bit.

Refer to the *MPC8349E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for details on the reset configuration word high settings.

**Table 11. PCI Bus Interface Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | If Used | If Not Used | |
| | **PCI Interface** | | | | | | | | |
| | $\overline{\text{PCI1\_INTA}}$/ $\overline{\text{IRQ\_OUT}}$ | O | X | X | X | X | 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | Open drain signal. In agent mode, $\overline{\text{INTA}}$ typically connects to a central interrupt controller. In host mode, $\overline{\text{INTA}}$ may be used to assert interrupts to other devices, such as a second processor. |
| | $\overline{\text{PCI1\_RESET\_OUT}}$ | O | X | X | X | X | As needed | Open | This signal is used only in host mode. It should be left unconnected in agent mode. |
| | PCI1_AD[31:0] | I/O | X | X | X | X | As needed | 2 k–10 kΩ to OV$_{DD}$ or Open | If the PCI1 port is not used, no termination is needed if the bus is parked. Software needs to park the bus as follows: 1. RCWHR[PCIHOST] = 1 2. RCWHR[PCI1ARB] = 1 3a. PCI Arbiter Control Configuration Register PM bit = 1, or 3b. PCI_GCR[BBR] = 1 (for PCI1 interface) |
| | PCI1_C/$\overline{\text{BE}}$[3:0] | I/O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ or Open | If the PCI1 port is not used, no termination is needed if the bus is parked. Software needs to park the bus as follows: 1. RCWHR[PCIHOST] = 1 2. RCWHR[PCI1ARB] = 1 3a. PCI Arbiter Control Configuration Register PM bit = 1, or 3b. PCI_GCR[BBR] = 1 (for PCI1 interface) |
| | PCI1_PAR | I/O | X | X | X | X | As needed | 2 k–10 kΩ to OV$_{DD}$ | If the PCI1 port is not used, this signal must be pulled up. |
| | $\overline{\text{PCI1\_FRAME}}$ | I/O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | PCI specification requires a weak pullup. |
| | $\overline{\text{PCI1\_TRDY}}$ | I/O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | PCI specification requires a weak pullup. |
| | $\overline{\text{PCI1\_IRDY}}$ | I/O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | PCI specification requires a weak pullup. |
| | $\overline{\text{PCI1\_STOP}}$ | I/O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | PCI specification requires a weak pullup. |

**PowerQUICC Design Checklist,  Rev. 10**

**Table 11. PCI Bus Interface Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | $\overline{PCI1\_DEVSEL}$ | I/O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | PCI specification requires a weak pullup. |
| X | PCI1_IDSEL | I | X | X | X | X | **PCI host:** Tie to GND **PCI agent:** One of PCI1_AD[31:0] | Tie to GND | IDSEL should be connected to GND for host systems and to one address line for agent systems. If the PCI port is not used, it should be grounded. • PCI host is selected by RCWH[PCIHOST] = 1. • PCI agent is selected by RCWH[PCIHOST] = 0. |
| | $\overline{PCI1\_SERR}$ | I/O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | PCI specification requires a weak pullup. |
| | $\overline{PCI1\_PERR}$ | I/O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | PCI specification requires a weak pullup. |
| | $\overline{PCI1\_REQ0}$ | I/O | X | X | X | X | **External arbiter:** As needed **Internal arbiter:** As needed + 2 k–10 kΩ to OV$_{DD}$ | **External arbiter:** Open **Internal arbiter:** 2 k–10 kΩ to OV$_{DD}$ | If an external arbiter is used, $\overline{REQ0}$ becomes an *output* signal and does not need to be terminated. • External arbiter selected by RCWH[PCI1ARB] = 0. • Internal arbiter selected by RCWH[PCI1ARB] = 1. |
| | $\overline{PCI1\_REQ}$[1]/ CPCI1_HS_ES | I | X | X | X | X | **External arbiter:** As needed **Internal arbiter:** As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | This pin is multiplexed with a CompactPCI Hot Swap function. CompactPCI functionality selected when external arbiter is used. • External arbiter selected by RCWH[PCI1ARB] = 0. • Internal arbiter selected by RCWH[PCI1ARB] = 1. |
| | $\overline{PCI1\_REQ}$[2:4] | I | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | — |

**PowerQUICC Design Checklist, Rev. 10**

## Table 11. PCI Bus Interface Pin Listing (continued)

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | PCI1_GNT0 | I/O | X | X | X | X | **External arbiter:** As needed + 2 k–10 kΩ to OV$_{DD}$  **Internal arbiter:** As needed | **External arbiter:** 2 k–10 kΩ to OV$_{DD}$  **Internal arbiter:** Open | If an external arbiter is used, $\overline{GNT0}$ becomes an *input* signal and should be pulled up with 2 k–10 kΩ to OV$_{DD}$.  • External arbiter selected by RCWH[PCI1ARB] = 0.  • Internal arbiter selected by RCWH[PCI1ARB] = 1. |
| | $\overline{PCI1\_GNT}$[1]/ CPCI_HS_LED | O | X | X | X | X | As needed | Open | This pin is multiplexed with a CompactPCI Hot Swap function. CompactPCI functionality selected when external arbiter is used.  • External arbiter selected by RCWH[PCI1ARB] = 0.  • Internal arbiter selected by RCWH[PCI1ARB] = 1. |
| | $\overline{PCI1\_GNT}$[2]/ CPCI1_HS_ENUM | O | X | X | X | X | **External arbiter:** As needed + 2 k–10 kΩ to OV$_{DD}$  **Internal arbiter:** As needed | **External arbiter:** Open  **Internal arbiter:** Open | This pin is multiplexed with a CompactPCI Hot Swap function. CompactPCI functionality selected when external arbiter is used.  • If **CompactPCI** Hot Swap function is used, a weak pullup is required (2 k–10 kΩ to OV$_{DD}$).  • External arbiter selected by RCWH[PCI1ARB] = 0.  • Internal arbiter selected by RCWH[PCI1ARB] = 1. |
| | $\overline{PCI1\_GNT}$[3:4] | O | X | X | X | X | As needed | Open | — |
| | $\overline{PCI2\_RESET\_OUT}$/ GPIO2[0] | O | — | — | — | X | As needed | 4.7 kΩ to Ovdd | PCI_RESET_OUT is used only in PCI Host mode. It should be left unconnected in PCI Agent mode. GPIO functionality is selected by RCWH[PCI64], and can be left OPEN if not used when functioning as GPIO. |
| | PCI2_AD[31:0]/ PCI1_AD[63:32] | I/O | — | — | — | X | As needed | 2 k–10 kΩ to OV$_{DD}$ or Open | If the PCI2 port is not used, no termination is needed if the bus is parked. Software needs to park the bus as follows: 1. RCWHR[PCIHOST] = 1 2. RCWHR[PCI2ARB] = 1 3a. PCI Arbiter Control Configuration Register PM bit = 1, or 3b. PCI_GCR[BBR] = 1 (for PCI2 interface) |

**Table 11. PCI Bus Interface Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | If Used | If Not Used | |
| | PCI2_C_$\overline{BE}$[3:0]/ PCI1_C_$\overline{BE}$[7:4] | I/O | — | — | — | X | 2 k–10 kΩ to $OV_{DD}$ | 2 k–10 kΩ to $OV_{DD}$ or Open | If the PCI2 port is not used, no termination is needed if the bus is parked. Software needs to park the bus as follows: 1. RCWHR[PCIHOST] = 1 2. RCWHR[PCI2ARB] = 1 3a. PCI Arbiter Control Configuration Register PM bit = 1, or 3b. PCI_GCR[BBR] = 1 (for PCI2 interface) |
| | PCI2_PAR/ PCI1_PAR64 | I/O | — | — | — | X | As needed | 2 k–10 kΩ to $OV_{DD}$ | If the PCI1 64-bit port and PCI2 32-bit port are not used, this signal must be pulled up. • PCI1 functionality is selected by RCWH[PCI64] and connection rules still apply. |
| | $\overline{PCI2\_FRAME}$/ GPIO2[1] | I/O | — | — | — | X | As needed + 2 k–10 kΩ to $OV_{DD}$ | 2 k–10 kΩ to $OV_{DD}$ | PCI specification requires a weak pullup. • GPIO functionality is selected by RCWH[PCI64], and can be left open if not used when functioning as GPIO. |
| | $\overline{PCI2\_TRDY}$ | I/O | — | — | — | X | As needed + 2 k–10 kΩ to $OV_{DD}$ | 2 k–10 kΩ to $OV_{DD}$ | PCI specification requires a weak pullup. |
| | $\overline{PCI2\_IRDY}$ | I/O | — | — | — | X | As needed + 2 k–10 kΩ to $OV_{DD}$ | 2 k–10 kΩ to $OV_{DD}$ | PCI specification requires a weak pullup. |
| | $\overline{PCI2\_STOP}$ | I/O | — | — | — | X | As needed + 2 k–10 kΩ to $OV_{DDD}$ | 2 k–10 kΩ to $OV_{DD}$ | PCI specification requires a weak pullup. |
| | $\overline{PCI2\_DEVSEL}$/ GPIO2[5] | I/O | — | — | — | X | As needed + 2 k–10 kΩ to $OV_{DD}$ | 2 k–10 kΩ to $OV_{DD}$ | PCI specification requires a weak pullup. • GPIO functionality is selected by RCWH[PCI64], and can be left open if not used. |
| | $\overline{PCI2\_SERR}$/ $\overline{PCI1\_ACK64}$ | I/O | — | — | — | X | As needed + 2 k–10 kΩ to $OV_{DD}$ | 2 k–10 kΩ to $OV_{DD}$ | PCI specification requires a weak pullup. • PCI1 functionality is selected by RCWH[PCI64] and connection rules still apply. |
| | $\overline{PCI2\_PERR}$/ $\overline{PCI1\_REQ64}$ | I/O | — | — | — | X | As needed + 2 k–10 kΩ to $OV_{DD}$ | 2 k–10 kΩ to $OV_{DD}$ | PCI specification requires a weak pullup. • PCI1 functionality is selected by RCWH[PCI64] and connection rules still apply. |

**PowerQUICC Design Checklist, Rev. 10**

**Table 11. PCI Bus Interface Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | $\overline{PCI2\_REQ0}$/ GPIO2[6] | I/O | — | — | — | X | **External arbiter:** As needed<br><br>**Internal arbiter:** As needed + 2 k–10 k$\Omega$ to OV$_{DD}$ | **External arbiter:** Open<br><br>**Internal arbiter:** 2 k–10 k$\Omega$ to OV$_{DD}$ | GPIO functionality is selected by RCWH[PCI64], and can be left OPEN if not used when functioning as GPIO. If an external arbiter is used, $\overline{REQ0}$ becomes an output signal and does not need to be terminated.<br>• External arbiter selected by RCWH[PCI2ARB] = 0.<br>• Internal arbiter selected by RCWH[PCI2ARB] = 1. |
| | $\overline{PCI2\_REQ}$[1:2]/ GPIO[7:8] | I/O | — | — | — | X | As needed + 2 k–10 k$\Omega$ to OV$_{DD}$ | 2 k–10 k$\Omega$ to OV$_{DD}$ | GPIO functionality is selected by RCWH[PCI64], and can be left OPEN if not used when functioning as GPIO. |
| | $\overline{PCI2\_GNT0}$/ GPIO[9] | I/O | — | — | — | X | **External arbiter:** As needed + 2 k–10 k$\Omega$ to OV$_{DD}$<br><br>**Internal arbiter:** As needed | **External arbiter:** 2 k–10 k$\Omega$ to OV$_{DD}$<br><br>**Internal arbiter:** Open | GPIO functionality is selected by RCWH[PCI64], and can be left OPEN if not used when functioning as GPIO. If an external arbiter is used, $\overline{GNT0}$ becomes an input signal and should be pulled up with 2 k–10 k$\Omega$ to OV$_{DD}$.<br>• External arbiter selected by RCWH[PCI2ARB] = 0<br>• Internal arbiter selected by RCWH[PCI2ARB] = 1 |
| | $\overline{PCI2\_GNT}$[1:2]/ GPIO[10:11] | I/O | — | — | — | X | As needed | 2 k–10 k$\Omega$ to OV$_{DD}$ | GPIO functionality is selected by RCWH[PCI64], and can be left OPEN if not used when functioning as GPIO. |
| | M66EN | I | X | X | X | X | As needed | 5 k$\Omega$ to OV$_{DD}$ or 1 k$\Omega$ to GND | Open-drain signal. No role if PCI is not used. |

## 6.2  DDR SDRAM

Refer to the following application notes for details on layout consideration and DDR programming guidelines:

- AN2582: "Hardware and Layout Design Considerations for DDR Memory Interfaces," for signal integrity and layout considerations.
- AN2583: "Programming the PowerQUICC™ III DDR SDRAM Controller," for DDR programming guidelines

**NOTE**

> Disable the clocks that the DDRCLKDR register does not use. By default, all clocks are operational, but not all clock signals are used in a given application. Therefore, disabling the unused clocks first lowers the power consumption and then lowers the unused switching activity in the part. DDRCLKDR is not a part of the memory controller register set; it is located in the global utility register section.

The DDR bus should not be configured during use. Rather, it should be configured by executing code from the local bus.

The DDR controller on the PowerQUICC II Pro can be configured with a 64- or 32-bit data bus interface. DDR_SDRAM_CFG[32_BE] controls the bus width selection. The burst length is set to 8 beats for 32-bit mode by properly configuring DDR_SDRAM_CFG[8_BE]. Refer to *MPC8349E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for details on these register settings.

**NOTE**

> For PowerQUICC II Pro devices, only the source synchronous clock mode is supported for the DDR controller. Software must ensure that the DDR_SDRAM_CLK_CNTL[SS_EN] bit is set to 1 before the DDR interface is enabled.

Table 12 summarizes the DDR SDRAM pins.

**Table 12. DDR SDRAM Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | | | | | | | If Used | If Not Used | |
| DDR SDRAM Memory Interface | | | | | | | | | |
| | MDQ[0:31] | I/O | X | X | X | X | As needed | Open | When in use, proper signal integrity analysis must be performed using the respective device IBIS model.<br>• Parallel termination is optional for DDR signals and should be simulated to verify necessity.<br>• Differential termination is included on DIMMs. It is only required for discrete memory applications. |
| | MDQ[32:63] | I/O | — | X | X | X | As needed | Open | When in use, proper signal integrity analysis must be performed using the respective device IBIS model. |
| | MECC[0:4]/ MSRCID[0:4] | I/O | X | X | X | X | As needed | Open | Pin functionality determined by SICRL[0] bit setting. |
| | MECC[5]/MDVAL | I/O | X | X | X | X | As needed | Open | Pin functionality determined by SICRL[0] bit setting. |
| | MECC[6:7] | I/O | X | X | X | X | As needed | Open | — |

**Table 12. DDR SDRAM Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | If Used | If Not Used | |
| | MDM[0:3] | O | X | X | X | X | As needed | Open | — |
| | MDM[4:7] | O | — | X | X | X | As needed | Open | — |
| | MDM[8] | O | X | X | X | X | As needed | Open | — |
| | MDQS[0:3] | I/O | X | X | X | X | As needed | Open | — |
| | MDQS[4:7] | I/O | — | X | X | X | As needed | Open | — |
| | MDQS[8] | I/O | X | X | X | X | As needed | Open | — |
| | MBA[0:1] | O | X | X | X | X | As needed | Open | — |
| | MBA[2] | O | X | X | X | X | As needed | Open | For Rev. 1.x devices: Leave unconnected. For Rev. 3.0 devices and onward: Pin is supported. |
| | MA[0:14] | O | X | X | X | X | As needed | Open | — |
| | $\overline{\text{MWE}}$ | O | X | X | X | X | As needed | Open | — |
| | $\overline{\text{MRAS}}$ | O | X | X | X | X | As needed | Open | — |
| | $\overline{\text{MCAS}}$ | O | X | X | X | X | As needed | Open | — |
| | $\overline{\text{MCS}}$[0:3] | O | X | X | X | X | As needed | Open | — |
| | MCKE[0:1] | O | X | X | X | X | As needed | Open | This output is actively driven during reset rather than being three-stated during reset. |
| | MCK[0:3] | O | X | X | X | X | As needed | Open | — |
| | $\overline{\text{MCK}}$[0:3] | O | X | X | X | X | As needed | Open | — |
| | MCK[4:5] | O | — | X | X | X | As needed | Open | — |
| | $\overline{\text{MCK}}$[4:5] | O | — | X | X | X | As needed | Open | — |
| | ODT[0:3] or MODT[0:3] | O | X | X | X | X | As needed | Open | For Rev. 1.x devices: ODT[0:3] pins are defined, leave unconnected. For Rev. 3.0 devices and onward: MODT[0:3] pins are defined and supported for DDR-II. |

## 6.2.1 SPARE1/MDIC1 and SPARE2/MDIC0

The two spare pins (SPARE1 and SPARE2) in Rev. 1.0/1.1 silicon are used for input impedance calibration for DDR2 in Rev. 3.0. As long as the user uses DDR1, MDIC0/MDIC1 act as spares and terminations for these two pins follow the SPARE2/SPARE1 termination recommendations for Rev. 1.1 as indicated in

Table 13. Similarly, if the user selects DDR2, the terminations follow the MDIC0/MDIC1 termination recommendations.

**Table 13. SPARE1/MDIC1 and SPARE2/MDIC0 Termination Recommendations**

| Pins | Rev. 1.0 / 1.1 | Rev. 3.0 | |
| --- | --- | --- | --- |
| | DDR1 | DDR1 | DDR2 |
| SPARE1/MDIC1 | Open | Open | 18 $\Omega$ to $GV_{DD}$ |
| SPARE2/MDIC0 | 0 $\Omega$ to GND | 0 $\Omega$ to GND | 18 $\Omega$ to GND |

The user selects the DDR type by configuring the DDR_SDRAM_CFG[SDRAM_TYPE] and the DDRCDR registers.

## 6.2.2 DDR1 Considerations in Revision 3.x

Customers using DDR1 in Revision 3.x, either migrating from Revision 1.x to Revision 3.x or considering a new design with DDR1, should follow the recommendations provided in this section for a successful DDR1 interface operation in their system.

- The DDR1 driver strength should be set to half strength on both the memory controller side and the DRAM side. This is done to reduce the overall system noise by setting the following registers:
  — (Offset 0x0_0128) DDRCDR = 0x0004_0001
  — (Offset 0x0_2110) DDR_SDRAM_CFG [HSE] = 0b1
  — (Offset 0x0_2118) DDR_SDRAM_MODE [bit 14] = 0b1
- The termination scheme should be set to reduce the overall system noise on DDR1 interface. This is done by using the following termination scheme:
  — For all MDQ/MDQS/MDM signals, the parallel termination resistor (RTT) = 100 $\Omega$ and the series resistor (RS) = 10 $\Omega$.
  — For all address/command/control signals the parallel termination resistor (RTT) = 150 $\Omega$ and series resistor (RS) = 22 $\Omega$.

### NOTE

Observe the existing recommendations on proper layout for DDR1 as stated in application note AN2582.

It is highly recommended that users repeat the IBIS simulation with the new IBIS model that is modified for the silicon revision 3.x

## 6.2.3 Unused Signals Considerations for Both DDR1 and DDR2

All unused clock signals should disabled via MCKENR register (offset 0x0_1010).

All unused ECC signals should be connected to GND via a 150-$\Omega$ resistor.

## 6.2.4 MVREF*n* Connection Options

Each of the MVREF1 and MVREF2 supply inputs must be connected through serial resistors of 100 Ω. The resistors must be the closest component to the MPC834*x* MVREF*n* ball connection. Additionally, the number of decoupling capacitors used should be as stated in AN2582, "Hardware and Layout Design Considerations for DDR Memory Interfaces." The two options are shown in Figure 5 and in Figure 6.
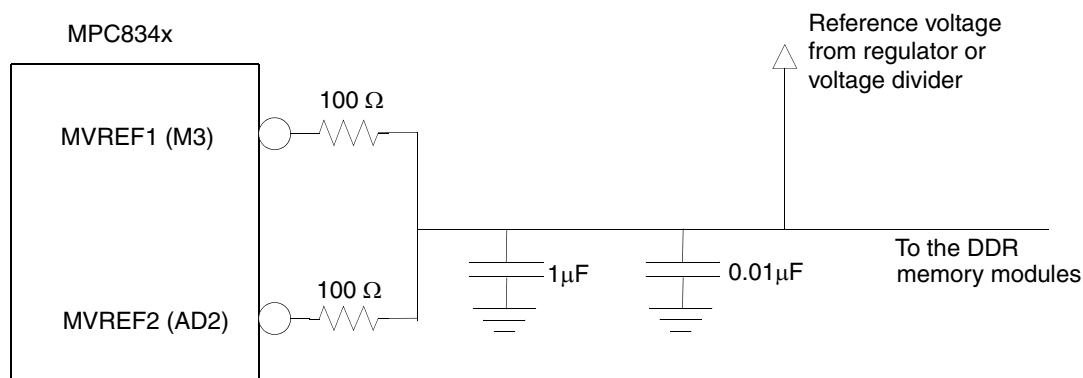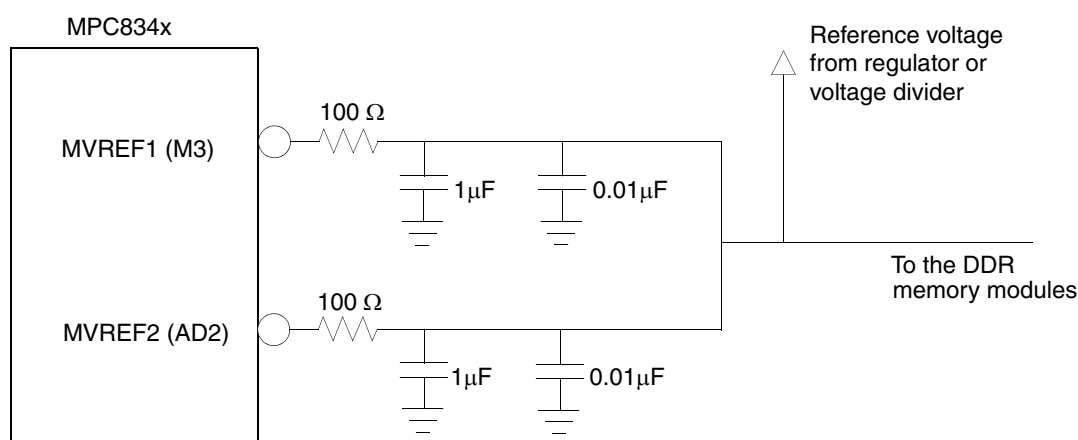


**Figure 5. MVREF1 and MVREF2 Connection Option #1**



**Figure 6. MVREF1 and MVREF2 Connection Option #2**

## 6.3 Local Bus Controller

The local bus frequency is adjusted through the LCRR[CLKDIV] register. If modified, the DLL requires a re-lock time prior to use. The lock time can vary between ~7680 to 122,880 CSB clock cycles and is a ratio between the LBC and CSB clock. The 2:1 ratio corresponds to the minimum lock time and the 8:1 ratio corresponds to the maximum lock time. After reset, the PowerQUICC II Pro defaults to a 8:1 ratio.

The local bus clock is not configured while it is executing from the local bus, but rather by executing code from the DDR.

The PowerQUICC II Pro local bus features a multiplexed address and data bus, LAD[0:31]. An external latch is required to de-multiplex these signals to the connecting device. LAD[0] is the most significant

address and data bit, while LAD[31] is the least significant address and data bit. Table 14 lists guidelines for connecting to 8-, 16-, and 32-bit devices.

**Table 14. Local Bus Byte Lane Control**

| Device Data Width | Most Significant Bit | Least Significant Bit | Byte Lane Control | | |
|---|---|---|---|---|---|
| | | | GPCM | UPM | SDRAM |
| 8-bit | LAD[0] | LAD[7] | $\overline{LWE}$[0] | $\overline{LBS}$[0] | LSDDQM[0] |
| 16-bit | LAD[0] | LAD[15] | $\overline{LWE}$[0:1] | $\overline{LBS}$[0:1] | LSDDQM[0:1] |
| 32-bit | LAD[0] | LAD[31] | $\overline{LWE}$[0:3] | $\overline{LBS}$[0:3] | LSDDQM[0:3] |

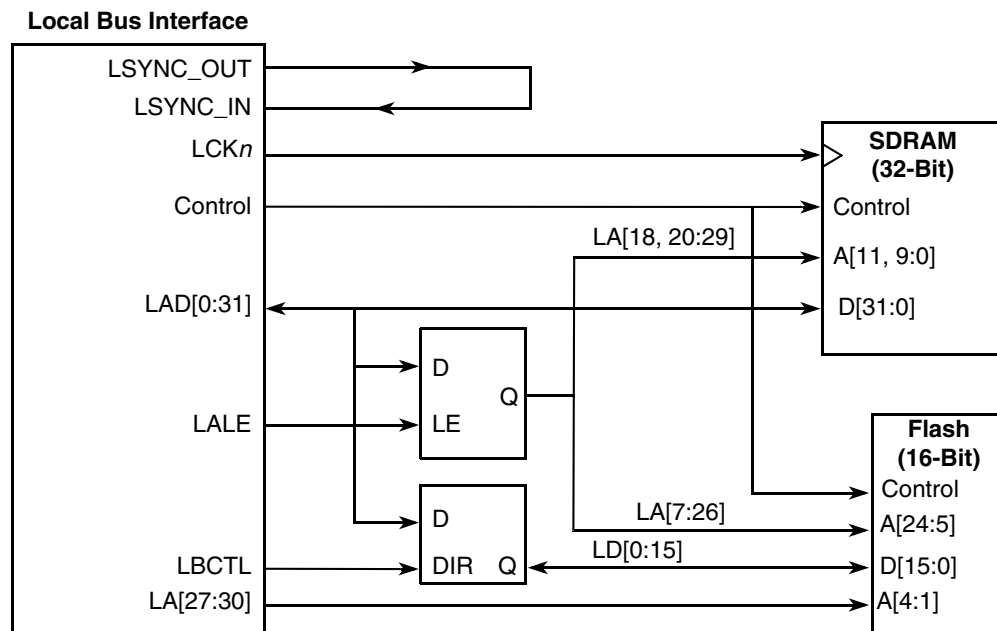Figure 7 shows a simplified connection to a 32-bit SDRAM device and a 16-bit flash memory device.



**Figure 7. Local Bus Connection to SDRAM and Flash**

Table 15 summarizes the local bus pins.

**Table 15. Local Bus Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | If Used | If Not Used | |
| | Local Bus Interface | | | | | | | | |
| | LAD[0:31] | I/O | X | X | X | X | As needed | 2 k–10 kΩ to OV$_{DD}$ | See note for the LA[27:32] signals. |
| | LDP[0]/ $\overline{CKSTOP\_OUT}$ | I/O | X | X | X | X | As needed | 2 k–10 kΩ to OV$_{DD}$ | Pin functionality is selected by RCWH[LDP] |

**PowerQUICC Design Checklist, Rev. 10**

**Table 15. Local Bus Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
| | | | | | | | If Used | If Not Used | |
|---|---|---|---|---|---|---|---|---|---|
| | LDP[1]/ $\overline{\text{CKSTOP\_IN}}$ | I/O | X | X | X | X | As needed | 2 k–10 kΩ to OV$_{DD}$ | Pin functionality is selected by RCWH[LDP] |
| | LDP[2:3] | I/O | X | X | X | X | As needed | 2 k–10 kΩ to OV$_{DD}$ | — |
| | LA[27] | O | X | X | X | X | As needed | Open | If the HRCW is loaded through the local bus, the LA[27:31 pins are used and not the LAD[27:31] pins. The LAD[27:31 pins are not driven during HRCW loading. Only the LA[27:31] increment during the load of the HRCW. In essence, the device does a type of burst access to the flash memory when it loads the HRCW. It drives the high-order bits of the address on LAD[0:26], which is also the first address in a 4-byte sequence, asserts LALE, latches the first byte, and then increments LA[27:31] to get the next 3 bytes. It then drives the high-order bits for the second access, asserts LALE, latches a byte, and again increments the LA[27:31] to get the next 3 bytes. Out of reset, the LA[27:31] and LAD[27:31] mirror each other (while LALE is asserted). |
| | LA[28:31] | O | X | X | X | X | As needed | Open | |
| | $\overline{\text{LCS}}$[0:3] | O | X | X | X | X | As needed | Open | — |
| | $\overline{\text{LWE}}$[0:3]/$\overline{\text{LBS}}$[0:3]/ LSDDQM[0:3] | O | X | X | X | X | As needed | Open | — |
| | LBCTL | O | X | X | X | X | As needed | Open | — |
| | LALE | O | X | X | X | X | As needed | Open | — |
| X | LGPL0/LSDA10/ **cfg_reset_source0** | I/O | X | X | X | X | As needed | — | Input during power-on and hard reset flows, providing the reset configuration word source. Signal values should be driven by an FPGA during power-on and hard reset flows OR through pull-up/down resistors (4.7 kΩ to OV$_{DD}$ or 1 kΩ to GND). Functional output signal after reset flow completes. Pull-up/down resistors not needed. |
| X | LGPL1/$\overline{\text{LSDWE}}$/ **cfg_reset_source1** | I/O | X | X | X | X | As needed | Open | |
| | LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$ | O | X | X | X | X | As needed | Open | — |

**PowerQUICC Design Checklist, Rev. 10**

**Table 15. Local Bus Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | If Used | If Not Used | |
| X | LGPL3/$\overline{\text{LSDCAS}}$/ **cfg_reset_source2** | I/O | X | X | X | X | As needed | Open | Input during power-on and hard reset flows, providing the reset configuration word source. Signal values should be driven by an FPGA during power-on and hard reset flows OR through pull-up/down resistors (4.7 k$\Omega$ to OV$_{DD}$ or 1 k$\Omega$ to GND). Functional output signal after reset flow completes. Pull-up/down resistors not needed. |
| | LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LPBSE | I/O | X | X | X | X | **LPBSE:** As needed **Others:** As needed + 1 k–10 k$\Omega$ to OV$_{DD}$ | 4.7 k$\Omega$ to OV$_{DD}$ | Pin functionality is selected by LBCR[LPBSE] • LPBSE mode: no pull-up required. • If LGPL4 (UPM) funtionality is used, 1 k$\Omega$ to OV$_{DD}$ is needed. Otherwise, 10 k$\Omega$ to OV$_{DD}$ can be used. |
| X | LGPL5/cfg_clkin_div | I/O | X | X | X | X | **PCI host:** 1 k$\Omega$ to OV$_{DD}$ or 1 k$\Omega$ to GND **PCI agent:** 1 k$\Omega$ to GND | 1 k$\Omega$ to GND | Input during power-on and hard reset flows. Functional signal after reset flow completes. Functional output signal after reset flow completes. Pull-up/down resistors not needed. |
| | LCKE | O | X | X | X | X | As needed | Open | — |
| | LCLK[0:2] | O | X | X | X | X | As needed | Open | — |
| | LSYNC_OUT | O | X | X | X | X | 22–33 $\Omega$ damping resistor in feedback path (LSYNC_OUT to LSYNC_IN) | | It is highly recommended to place damping resistor close to LSYNC_OUT pin. Simulation should be performed to verify damping resistor value. Trace loop from LSYNC_OUT to LSYNC_IN should go halfway out to synchronous device (DRAM DIMM or discrete devices). |
| | LSYNC_IN | I | X | X | X | X | | | |

# 6.4  General-Purpose I/O Timers

The two general-purpose I/O modules, GPIO1 and GPIO2, can each support 32 general-purpose I/O ports. Each port can be configured as an input or an output. If a port is configured as an input, it can optionally generate an interrupt upon detection of a change. If a port is configured as an output, it can be individually configured as an open-drain or fully active output. Each GPIO port is multiplexed with other functions.

GPIO1 is multiplexed with general-purpose timers and TSEC2 interface pins. GPIO2 is multiplexed with TSEC1 interface pins, and $\overline{\text{IRQ}}$ pins. Each GPIO pin is programmed using the system I/O configuration

**PowerQUICC Design Checklist,  Rev. 10**

low (SICRL) and system I/O configuration register high (SICRH) registers. Starting with Rev. 3.0 of the PowerQUICC II Pro family, DMA control signals are also multiplexed with some of the GPIO1 pins.

Four general-purpose timers are multiplexed with the GPIO1[0:11] pins. Each timer interface consists of the $\overline{\text{TGATE}n}$, TIN*n,* and $\overline{\text{TOUT}n}$ pins. Each timer pin is programmed using the system I/O configuration low (SICRL) register. For a full description of how the four general-purpose timers are used, consult the *MPC8349E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.

Table 16 summarizes the general-purpose I/O pins.

**Table 16. General-Purpose I/O Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | If Used | If Not Used | |
| **General-Purpose I/O Timers** | | | | | | | | | |
| | GPIO1[0]/ $\overline{\text{DMA\_DREQ0}}$/ GTM1_TIN1/ GTM2_TIN2 | I/O | X | X | X | X | As needed | 4.7 kΩ to OVdd | For Rev. 1.x devices:<br>• Pin functionality determined by SICRL[6] bit setting.<br>For Rev. 3.0 devices and onward:<br>• DMA functionality added<br>• Pin functionality determined by SICRL[6,20] bit settings. |
| | GPIO1[1]/ $\overline{\text{DMA\_DACK0}}$/ $\overline{\text{GTM1\_TGATE1}}$/ $\overline{\text{GTM2\_TGATE2}}$ | I/O | X | X | X | X | As needed | 4.7 kΩ to OVdd | For Rev. 1.x devices:<br>• Pin functionality determined by SICRL[7] bit setting.<br>For Rev. 3.0 devices and onward:<br>• DMA functionality added<br>• Pin functionality determined by SICRL[7,21] bit settings. |
| | GPIO1[2]/ $\overline{\text{DMA\_DDONE0}}$/ $\overline{\text{GTM1\_TOUT1}}$ | I/O | X | X | X | X | As needed | 4.7 kΩ to OVdd | For Rev. 1.x devices:<br>• Pin functionality determined by SICRL[8] bit setting.<br>For Rev. 3.0 devices and onward:<br>• DMA functionality added<br>• Pin functionality determined by SICRL[8,22] bit settings. |
| | GPIO1[3]/ $\overline{\text{DMA\_DREQ1}}$/ GTM1_TIN2/ GTM2_TIN1 | I/O | X | X | X | X | As needed | 4.7 kΩ to OVdd | For Rev. 1.x devices:<br>• Pin functionality determined by SICRL[9] bit setting.<br>For Rev. 3.0 devices and onward:<br>• DMA functionality added<br>• Pin functionality determined by SICRL[9,23] bit settings. |

**Table 16. General-Purpose I/O Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | | | | | | | If Used | If Not Used | |
| | GPIO1[4]/ $\overline{\text{DMA\_DACK1}}$/ $\overline{\text{GTM1\_TGATE1}}$/ $\overline{\text{GTM2\_TGATE2}}$ | I/O | X | X | X | X | As needed | 4.7 kΩ to OVdd | For Rev. 1.x devices:<br>• Pin functionality determined by SICRL[10] bit setting.<br>For Rev. 3.0 devices and onward:<br>• DMA functionality added<br>• Pin functionality determined by SICRL[10,24] bit settings. |
| | GPIO1[5]/ $\overline{\text{DMA\_DDONE1}}$/ $\overline{\text{GTM1\_TOUT2}}$/ $\overline{\text{GTM2\_TOUT1}}$ | I/O | X | X | X | X | As needed | 4.7 kΩ to OVdd | For Rev. 1.x devices:<br>• Pin functionality determined by SICRL[11:12] bit settings.<br>For Rev. 3.0 devices and onward:<br>• DMA functionality added<br>• Pin functionality determined by SICRL[11:12] bit settings. |
| | GPIO1[6]/ $\overline{\text{DMA\_DREQ2}}$/ GTM1_TIN3/ GTM2_TIN4 | I/O | X | X | X | X | As needed | 4.7 kΩ to OVdd | For Rev. 1.x devices:<br>• Pin functionality determined by SICRL[13] bit setting.<br>For Rev. 3.0 devices and onward:<br>• DMA functionality added<br>• Pin functionality determined by SICRL[13,25] bit settings. |
| | GPIO1[7]/ $\overline{\text{DMA\_DACK2}}$/ $\overline{\text{GTM1\_TGATE3}}$/ $\overline{\text{GTM2\_TGATE4}}$ | I/O | X | X | X | X | As needed | 4.7 kΩ to OVdd | For Rev. 1.x devices:<br>• Pin functionality determined by SICRL[14] bit setting.<br>For Rev. 3.0 devices and onward:<br>• DMA functionality added<br>• Pin functionality determined by SICRL[14,26] bit settings. |
| | GPIO1[8]/ $\overline{\text{DMA\_DDONE2}}$/ $\overline{\text{GTM1\_TOUT3}}$ | I/O | X | X | X | X | As needed | 4.7 kΩ to OVdd | For Rev. 1.x devices:<br>• Pin functionality determined by SICRL[15] bit setting.<br>For Rev. 3.0 devices and onward:<br>• DMA functionality added<br>• Pin functionality determined by SICRL[16,28] bit settings. |
| | GPIO1[9]/ $\overline{\text{DMA\_DREQ1}}$/ GTM1_TIN4/ GTM2_TIN3 | I/O | X | X | X | X | As needed | 4.7 kΩ to OVdd | For Rev. 1.x devices:<br>• Pin functionality determined by SICRL[16] bit setting.<br>For Rev. 3.0 devices and onward:<br>• DMA functionality added<br>• Pin functionality determined by SICRL[16,28] bit settings. |

**Table 16. General-Purpose I/O Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | If Used | If Not Used | |
| | GPIO1[10]/ $\overline{\text{DMA\_DACK3}}$/ $\overline{\text{GTM1\_TGATE4}}$/ $\overline{\text{GTM2\_TGATE3}}$ | I/O | X | X | X | X | As needed | 4.7 kΩ to OVdd | For Rev. 1.x devices:<br>• Pin functionality determined by SICRL[17] bit setting.<br>For Rev. 3.0 devices and onward:<br>• DMA functionality added<br>• Pin functionality determined by SICRL[17, 29] bit settings. |
| | GPIO1[11]/ $\overline{\text{DMA\_DDONE3}}$/ $\overline{\text{GTM1\_TOUT4}}$/ $\overline{\text{GTM2\_TOUT3}}$ | I/O | X | X | X | X | As needed | 4.7 kΩ to OVdd | For Rev. 1.x devices:<br>• Pin functionality determined by SICRL[18:19] bit settings.<br>For Rev. 3.0 devices and onward:<br>• DMA functionality added<br>• Pin functionality determined by SICRL[18:19] bit settings. |

# 6.5  Universal Serial Bus (USB)

Figure 8 shows the USB interface block diagram.
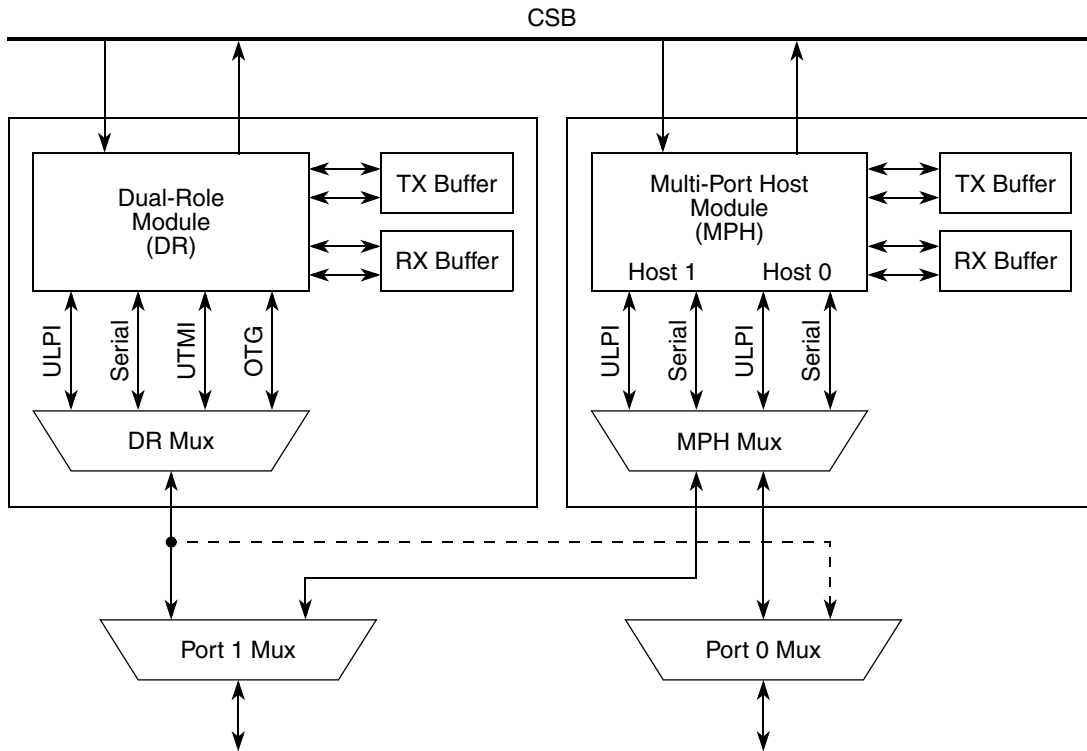


**Figure 8. USB Interface Block Diagram**

The PowerQUICC II Pro family implements up to two universal serial bus (USB) modules, a multiport host (MPH) module, and a dual-role (DR) module. The MPH module provides up to two USB 2.0 hosts, each of which can be configured to connect to either an ULPI PHY or a serial FS/LS transceiver. The DR module has three basic operating modes: host, device, and OTG. The DR module can be configured to connect to either an ULPI PHY, UTMI PHY, or FS/LS serial transceiver.

Software configures the USB interfaces. Two physical USB ports (Port 1 and Port 0) can be tied to either the multiport host module or the dual-role module. The system I/O configuration register low (SICRL) is used to tie a specific module to a USB port. The MPH/DR port status and control registers (MPHPORTSC1, MPHPORTSC2, DRPORTSC1) determines the actual physical interface used. Table 17 summarizes the supported configurations for the USB modules and external ports. Table 18 summarizes the universal serial bus pins.

**Table 17. USB External Port Configurations**

| Config No. | External USB Port 1 | External USB Port 0 | Software Settings |
|---|---|---|---|
| | **DR Device** | **MPH Host 0** | **SICRL[1:2] = 10** |
| 1 | Host/Device/OTG, *ULPI* | Host, *ULPI* | DRPORTSC1[31:30] = 10<br>MPHPORTSC1[31:30] = 10 |
| 2 | Host/Device, *Serial* | Host, *Serial* | DRPORTSC1[31:30] = 11<br>MPHPORTSC1[31:30] = 11 |
| 3 | Host/Device/OTG, *ULPI* | Host, *Serial* | DRPORTSC1[31:30] = 10<br>MPHPORTSC1[31:30] = 11 |
| 4 | Host/Device, *Serial* | Host, *ULPI* | DRPORTSC1[31:30] = 11<br>MPHPORTSC1[31:30] = 10 |
| | **MPH Host 1** | **MPH Host 0** | **SICRL[1:2] = 00** |
| 5 | Host, *ULPI* | Host, *ULPI* | MPHPORTSC1[31:30] = 10<br>MPHPORTSC2[31:30] = 10 |
| 6 | Host, *Serial* | Host, *Serial* | MPHPORTSC1[31:30] = 11<br>MPHPORTSC2[31:30] = 11 |
| | **DR Device** | | **SICRL[1:2] = 11** |
| 7 | Device, *UTMI* | | DRPORTSC1[31:30,28] = 001 |
| | **DR OTG (Negotiable Host/Device)** | | **SICRL[1:2] = 11** |
| 8 | OTG, *Serial OTG* | | MPHPORTSC1[31:30] = 10<br>MPHPORTSC2[31:30] = 10 |

**Table 18. Universal Serial Bus Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | **USB Port 1** | | | | | | | | |
| | MPH1_D0_ENABLEN/ DR_D0_ENABLEN | I/O | X | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |
| | MPH1_D1_SER_TXD/ DR_D1_SER_TXD | I/O | X | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |
| | MPH1_D2_VMO_SE0/ DR_D2_VMO_SE0 | I/O | X | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |
| | MPH1_D3_SPEED/ DR_D3_SPEED | I/O | X | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |
| | MPH1_D4_DP/ DR_D4_DP | I/O | X | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$* signals are valid. |
| | MPH1_D5_DM/ DR_D5_DM | I/O | X | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |
| | MPH1_D6_SER_RCV/ DR_D6_SER_RCV | I/O | X | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |
| | MPH1_D7_DRVVBUS/ DR_D7_DRVVBUS | I/O | X | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |
| | MPH1_NXT/ DR_SESS_VLD_NXT | I | X | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |
| | MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_ DPPULLUP | I/O | X | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |
| | MPH1_STP_SUSPEND/ DR_STP_SUSPEND | O | X | X | X | X | As needed | Open | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |
| | MPH1_PWRFAULT/ DR_RX_ERROR_ PWRFAULT | I | X | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |
| | MPH1_PCTL0/ DR_TX_VALID_PCTL0 | O | X | X | X | X | As needed | Open | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |

**Table 18. Universal Serial Bus Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | MPH1_PCTL1/ DR_TX_VALIDH | O | X | X | X | X | As needed | Open | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |
| | MPH1_CLK/DR_CLK | I | X | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[1] bit setting. MPC8343: Only $\overline{DR}$ signals are valid. |
| | **USB Port 0** | | | | | | | | |
| | MPH0_D0_ENABLEN/ DR_D8_CHGVBUS | I/O | — | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_D1_SER_TXD/ DR_D9_DCHGVBUS | I/O | — | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_D2_VMO_SE0/ DR_D10_DPPD | I/O | — | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_D3_SPEED/ DR_D11_DMMD | I/O | — | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_D4_DP/ DR_D12_VBUS_VLD | I/O | — | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_D5_DM/ DR_D13_SESS_END | I/O | — | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_D6_SER_RCV/ DR_D14 | I/O | — | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_D7_DRVVBUS/ DR_D15_IDPULLUP | I/O | — | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_NXT/ DR_RX_ACTIVE_ID | I | — | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_DIR_DPPULLUP/ DR_RESET | I/O | — | X | X | X | As needed | 4.7 kΩ to OVdd | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_STP_SUSPEND/ DR_TX_READY | I/O | — | X | X | X | As needed | Open | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_PWRFAULT/ DR_RX_VALIDH | I | — | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_PCTL0/ DR_LINE_STATE0 | I/O | — | X | X | X | As needed | Open | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_PCTL1/ DR_LINE_STATE1 | I/O | — | X | X | X | As needed | Open | Pin functionality determined by SICRL[2] bit setting. |
| | MPH0_CLK/ DR_RX_VALID | I | — | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by SICRL[2] bit setting. |

# 6.6    Integrated Programmable Interrupt Controller (IPIC)

The integrated programmable interrupt controller (IPIC) provides interrupt management for receiving hardware-generated interrupts from internal and external sources. It also prioritizes and delivers the interrupts to the CPU for servicing. In addition to the signals listed in Table 19, the general-purpose input and output ports (GPIO1, GPIO2) can be configured to generate interrupts to the PowerQUICC II Pro IPIC unit.

The $\overline{\text{IRQ}}$ lines are multiplexed with signals from GPIO2, CKSTOP_IN, and CKSTOP_OUT interface pins. The configuration of each $\overline{\text{IRQ}}$ pin is programmed using the system I/O configuration high register (SICRH).

Table 19 summarizes the programmable interrupt controller pins.

**Table 19. Programmable Interrupt Controller Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection If Used | Connection If Not Used | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **Programmable Interrupt Controller** | | |
| | $\overline{\text{MCP\_OUT}}$ | O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | Open drain signal |
| | $\overline{\text{IRQ}}$[0]/$\overline{\text{MCP\_IN}}$/ GPIO2[12] | I/O | X | X | X | X | **GPIO:** As needed<br><br>**Others:** As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | Pin functionality determined by SICRH[17] bit setting. |
| | $\overline{\text{IRQ}}$[1:5]/ GPIO2[13:17] | I/O | X | X | X | X | **GPIO:** As needed<br><br>**Others:** As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | Pin functionality determined by SICRH[18:22] bit settings. |

**Table 19. Programmable Interrupt Controller Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | If Used | If Not Used | |
| | $\overline{IRQ}$[6]/GPIO2[18]/ $\overline{CKSTOP\_OUT}$ | I/O | X | X | X | X | **GPIO:** As needed<br><br>**Others:** As needed + 2k-10k $\Omega$ to OV$_{DD}$ | 2 k–10 k$\Omega$ to OV$_{DD}$ | Pin functionality determined by SICRH[23:24] bit settings. |
| | $\overline{IRQ}$[7]/GPIO2[19]/ $\overline{CKSTOP\_IN}$ | I/O | X | X | X | X | **GPIO:** As needed<br><br>**Others:** As needed + 2k-10k $\Omega$ to OV$_{DD}$ | 2 k–10 k$\Omega$ to OV$_{DD}$ | Pin functionality determined by SICRH[25:26] bit settings. |

# 6.7    Three-Speed Ethernet Controllers (TSEC)

The three-speed Ethernet controller (TSEC) supports 10, 100, and 1000 Mbps Ethernet/802.3 networks. The complete TSEC is designed for single MAC applications with several standard MAC-PHY interfaces to connect to an external Ethernet transceiver:

- 10/100 Mbps/1 Gbps IEEE 802.3 GMII
- 10/100 Mbps IEEE 802.3 MII
- 10-Mbps IEEE 802.3 MII
- 1-Gbps IEEE 802.3z TBI
- 10/100 Mbps RGMII
- 1-Gbps full-duplex RGMII
- 1-Gbps RTBI

Two TSECs can be independently configured to support any one of these interfaces. The reset configuration word high controls the hardware configuration of the two TSEC MAC-PHY interfaces. RCWH[TSEC1M] and RCWH[TSEC2M] are used to configure TSEC1 and TSEC2, respectively, in either GMII, RGMII, TBI, or RTBI mode. In GMII mode, the MACCFG2[I/F mode] bits select between an MII or GMII interface.

Some TSEC1 interface pins are multiplexed with GPIO2 pins; some TSEC2 interface pins are multiplexed with GPIO1 pins and the USB interface pins. Each TSEC pin is programmed using the system I/O configuration register high (SICRH) register.

Table 20 shows the pin usage and software configuration for each particular MAC-PHY mode. TSEC interface pins not used in a particular MAC-PHY mode, can be used as GPIO by setting the appropriate bits in the SICRH register.

**Table 20. TSEC MAC-PHY Modes**

|  | MII | GMII | RGMII | TBI | RTBI |
|---|---|---|---|---|---|
| EC_GTX_CLK125 | — | 125 MHz clock | 125 MHz clock | 125 MHz clock | 125 MHz clock |
| TSEC*n*_COL | COL | — | — | — | — |
| TSEC*n*_CRS | CRS | — | — | SDET | — |
| TSEC*n*_GTX_CLK | — | GTX_CLK | GTX_CLK | GTX_CLK | GTX_CLK |
| TSEC*n*_RX_CLK | RX_CLK | RX_CLK | RX_CLK | RX_CLK0 | RX_CLK |
| TSEC*n*_RX_DV | RX_DV | RX_DV | RX_CTL | RCG[8] | RCG[4]/RCG[9] |
| TSEC*n*_RX_ER | RX_ER | RX_ER | — | RCG[9] | — |
| TSEC*n*_RXD[7:4] | — | RxD[7:4] | — | RCG[7:4] | — |
| TSEC*n*_RXD[3:0] | RxD[3:0] | RxD[3:0] | RxD[3:0]/RxD[7:4] | RCG[3:0] | RCG[3:0]/RCG[8:5] |
| TSEC*n*_TX_CLK | TX_CLK | — | — | RX_CLK1 | — |
| TSEC*n*_TXD[7:4] | — | TxD[7:4] | — | TCG[7:4] | — |
| TSEC*n*_TXD[3:0] | TxD[3:0] | TxD[3:0] | TxD[3:0]/TxD[7:4] | TCG[3:0] | TCG[3:0]/TCG[8:5] |
| TSEC*n*_TX_EN | TX_EN | TX_EN | TX_CTL | TCG[8] | TCG[4]/TCG[9] |
| TSEC*n*_TX_ER | TX_ER | TX_ER | — | TCG[9] | — |
| Software configuration | RCWH[TSEC*n*M]=10 MACCFG2[22:23]=01 | RCWH[TSEC*n*M]=10 MACCFG2[22:23]=10 | RCWH[TSEC*n*M]=00 MACCFG2[22:23]=10 | RCWH[TSEC*n*M]=11 MACCFG2[22:23]=10 | RCWH[TSEC*n*M]=01 MACCFG2[22:23]=10 |

**NOTE**

MPC8343E supports only MII, RGMII, and RTBI MAC-PHY modes.

## 6.7.1 Management Interface

The TSEC has one management interface that controls all external PHYs. The management interface of TSEC1 controls the TBI PHY from TSEC1 as well as all external PHYs. The management interface of TSEC2, shown in Figure 9, controls the TBI PHY from TSEC2 only.
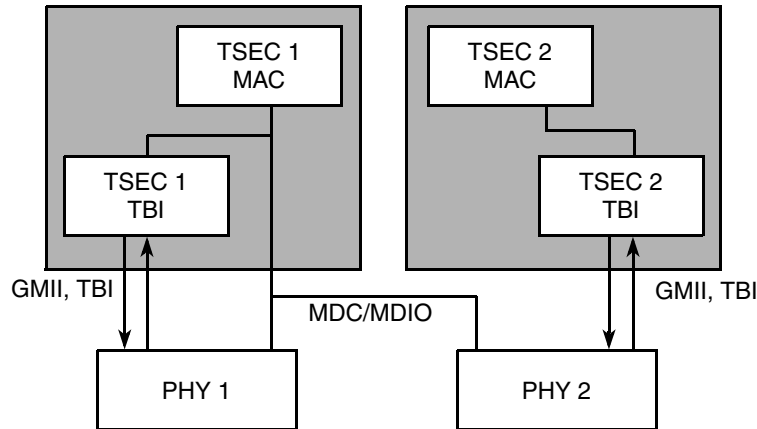


**Figure 9. TSEC Management Interface**

## 6.7.2 Graceful Stop

The TSEC interfaces can be stopped by the graceful stop mechanism. Stopping the transmit and receive buffers without using graceful stop can yield unpredictable results. To stop the transmit buffer with graceful stop, the processor must first set DMACTL[GTS] to gracefully stop the transmitter and then poll IEVENT[GTSC] to confirm that the stop is complete. Only then should the transmitter be disabled by clearing MACCFG1[TxEN].

To stop the receive buffer with graceful stop, first turn off the TSEC receiver to prevent any additional data from coming in. Then enable the graceful stop by setting DMACTL[GRS]. Wait for the confirmation by polling IEVENT[GRSC].

Table 21 summarizes the TSEC pins.

**Table 21. Three-Speed Ethernet Controller Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | **Ethernet Management** | | | | | | | | |
| | EC_MDC | O | X | X | X | X | As needed | Open | — |
| | EC_MDIO | I/O | X | X | X | X | As needed + 2 k–10 k$\Omega$ to LV$_{DD1}$ | 2 k–10 k$\Omega$ to LV$_{DD1}$ | — |

**Table 21. Three-Speed Ethernet Controller Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | If Used | If Not Used | |
| | **Gigabit Ethernet Reference Clock** | | | | | | | | |
| | EC_GTX_CLK125 | I | X | X | X | X | 125 MHz clock | 1 kΩ to GND | A 125 MHz reference clock should be supplied if either TSEC is being used in GMII, RGMII, TBI, or RTBI modes. |
| | **Three-Speed Ethernet Controller 1** | | | | | | | | |
| | TSEC1_COL/ GPIO2[20] | I/O | X | X | X | X | As needed | Open | Pin functionality determined by the SICRH[3] bit setting. |
| | TSEC1_CRS/ GPIO2[21] | I/O | X | X | X | X | As needed | Open | Pin functionality determined by the SICRH[3] bit setting. |
| | TSEC1_GTX_CLK | O | X | X | X | X | As needed | Open | Actively driven during $\overline{\text{RESET}}$ RGMII/RTBI mode: PC board trace should be routed such that an additional trace delay of greater than 1.5 ns will be added. Check Errata TSEC7 and its workaround. |
| | TSEC1_RX_CLK | I | X | X | X | X | As needed | 1 kΩ to GND | RGMII/RTBI mode: PC board trace should be routed so that an additional trace delay of greater than 1.5 ns is added to received clock signal as compared to data signals. Check Errata TSEC7 and its workaround. |
| | TSEC1_RX_DV | I | X | X | X | X | As needed | 1 kΩ to GND | — |
| | TSEC1_RX_ER/ GPIO2[26] | I/O | X | X | X | X | As needed | Open | Pin functionality determined by SICRH[6] bit setting. |
| | TSEC1_RXD[7:4]/ GPIO2[22:25] | I/O | — | X | X | X | As needed | Open | Pin functionality determined by SICRH[5] bit setting. |
| | TSEC1_RXD[3:0] | I | X | X | X | X | As needed | 1 kΩ to GND | — |
| | TSEC1_TX_CLK | I | X | X | X | X | As needed | 1 kΩ to GND | — |
| | TSEC1_TXD[7:4]/ GPIO2[27:30] | I/O | — | X | X | X | As needed | Open | Pin functionality determined by the SICRH[7] bit setting. |
| X | TSEC1_TXD3 | O | X | X | X | X | As needed | 4.7k to LVDD1 | For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net |
| | TSEC1_TXD[2:0] | O | X | X | X | X | As needed | Open | — |
| | TSEC1_TX_EN | I/O | X | X | X | X | As needed | Open | — |

**Table 21. Three-Speed Ethernet Controller Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | If Used | If Not Used | |
| | TSEC1_TX_ER/ GPIO2[31] | I/O | X | X | X | X | As needed | Open | Pin functionality determined by the SICRH[8] bit setting. |
| **Three-Speed Ethernet Controller 2** | | | | | | | | | |
| | TSEC2_COL/ GPIO1[21] | I/O | X | X | X | X | As needed | Open | Pin functionality determined by the SICRH[9] bit setting. |
| | TSEC2_CRS/ GPIO1[22] | I/O | X | X | X | X | As needed | 4.7 kΩ to Ovdd | Pin functionality determined by the SICRH[10] bit setting. |
| | TSEC2_GTX_CLK | O | X | X | X | X | As needed | Open | RGMII/RTBI mode: PC board trace should be routed so that an additional trace delay of greater than 1.5 ns is added. Check Errata TSEC7 and its workaround. |
| | TSEC2_RX_CLK | I | X | X | X | X | As needed | 1 kΩ to GND | RGMII/RTBI mode: PC board trace should be routed so that an additional trace delay of greater than 1.5 ns is added to received clock signal as compared to data signals. Check Errata TSEC7 and its workaround. |
| | TSEC2_RX_DV/ GPIO1[23] | I/O | X | X | X | X | As needed | Open | Pin functionality determined by the SICRH[11] bit setting. |
| | TSEC2_RXD[7:4]/ GPIO1[26:29] | I/O | — | X | — | X | As needed | Open | Pin functionality determined by the SICRH[12] bit setting. |
| | TSEC2_RXD[3:0]/ GPIO1[13:16] | I/O | X | X | X | X | As needed | Open | Pin functionality determined by the SICRH[11] bit setting. |
| | TSEC2_RX_ER/ GPIO1[25] | I/O | X | X | X | X | As needed | Open | Pin functionality determined by the SICRH[13] bit setting. |
| | TSEC2_TXD[7]/ GPIO1[31] | I/O | — | X | X | X | As needed | Open | Pin functionality determined by the SICRH[14] bit setting. |
| | TSEC2_TXD[6]/ DR_XCVR_TERM_SEL | O | — | X | X | X | As needed | Open | Pin functionality determined by the SICRH[14] bit setting. |
| | TSEC2_TXD[5]/ DR_UTMI_OPMODE1 | O | — | X | X | X | As needed | Open | Pin functionality determined by the SICRH[14] bit setting. |
| | TSEC2_TXD[4]/ DR_UTMI_OPMODE0 | O | — | X | X | X | As needed | Open | Pin functionality determined by the SICRH[14] bit setting. |
| | TSEC2_TXD[3:0]/ GPIO1[17:20] | I/O | X | X | X | X | As needed | Open | Pin functionality determined by the SICRH[11] bit setting. |
| | TSEC2_TX_ER/ GPIO1[24] | I/O | X | X | X | X | As needed | Open | Pin functionality determined by the SICRH[15] bit setting. |

**Table 21. Three-Speed Ethernet Controller Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | TSEC2_TX_EN/ GPIO1[12] | I/O | X | X | X | X | As needed | Open | Pin functionality determined by the SICRH[11] bit setting. |
| | TSEC2_TX_CLK/ GPIO1[30] | I/O | X | X | X | X | As needed | 1 kΩ to GND | Pin functionality determined by the SICRH[16] bit setting. |

# 6.8 DUART

Table 22 lists the dual UART pins.

**Table 22. Dual UART Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | | | | | **Dual UART** | | | | | |
| | UART_SOUT[1:2]/ MSRCID[0:1]/ LSRCID[0:1] | O | X | X | X | X | As needed | Open | Pin functionality determined by the SICRL[4:5] bit setting. |
| | UART_SIN[1:2]/ MSRCID[2:3]/ LSRCID[2:3] | I/O | X | X | X | X | As needed | 4.7 kΩ to Ovdd | Pin functionality determined by the SICRL[4:5] bit setting. |
| | UART_CTS[1]/ MSRCID[4]/ LSRCID[4] | I/O | X | X | X | X | As needed | 4.7 kΩ to Ovdd | Pin functionality determined by the SICRL[4:5] bit setting. |
| | UART_CTS[2]/ MDVAL/LDVAL | I/O | X | X | X | X | As needed | 4.7 kΩ to Ovdd | Pin functionality determined by the SICRL[4:5] bit setting. |
| | UART_RTS[1:2] | O | X | X | X | X | As needed | Open | — |

# 6.9 I²C Interface

Table 23 lists the I²C pins.

**Table 23. I²C Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | **I²C Interface** | | | | | | | | |
| | IIC1_SCL | I/O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | Open-drain signal |
| | IIC1_SDA | I/O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | Open-drain signal |
| | IIC2_SCL | I/O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | Open-drain signal |
| | IIC2_SDA | I/O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | Open-drain signal |

# 6.10 SPI

Table 24 lists the SPI pins.

**Table 24. SPI Pin Listing**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | **SPI Interface** | | | | | | | | |
| | SPIMOSI/$\overline{LCS}$[6] | I/O | X | X | X | X | **SPI:** As needed + 2 k–10 kΩ to OV$_{DD}$ **LCS:** As needed | 2 k–10 kΩ to OV$_{DD}$ | • Software configurable open-drain signal using SPMODE[OD] bit. Pull-up required only if configured as open drain. • $\overline{LCS}$ functionality added for Rev. 3.0 devices and onward. Pin functionality is selected by RCWH[LDP] value or SICRL[0] bit setting. |

**Table 24. SPI Pin Listing (continued)**

| Critical | Signal | Pin Type | MPC8343 | MPC8347(P) | MPC8347(T) | MPC8349 | Connection | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **If Used** | **If Not Used** | |
| | SPIMISO/$\overline{\text{LCS}}$[7] | I/O | X | X | X | X | **SPI:** As needed + 2 k–10 kΩ to OV$_{DD}$<br><br>**LCS:** As needed | 2 k–10 kΩ to OV$_{DD}$ | • Software configurable open-drain signal using SPMODE[OD] bit. Pull-up required only if configured as open drain.<br>• $\overline{\text{LCS}}$ functionality added for Rev. 3.0 devices and onward. Pin functionality is selected by RCWH[LDP] value or SICRL[0] bit setting. |
| | SPICLK | I/O | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | • Software configurable open-drain signal using SPMODE[OD] bit. Pull-up required only if configured as open drain. |
| | SPISEL | I | X | X | X | X | As needed + 2 k–10 kΩ to OV$_{DD}$ | 2 k–10 kΩ to OV$_{DD}$ | — |

# 7 Revision History

Table 25 provides a revision history for this application note.

**Table 25. Document Revision History**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 10 | 01/2011 | • Updated Section 6.2.2, "DDR1 Considerations in Revision 3.x," Section 6.2.3, "Unused Signals Considerations for Both DDR1 and DDR2," and Section 6.2.4, "MVREFn Connection Options."<br>• Updated first two paragaphs of Section 6.7.2, "Graceful Stop."<br>• In Table 21, added "Check Errata TSEC7 and its workaround" for TSEC1_GTX_CLK and TSEC1_RTX_CLK and TSEC2_GTX_CLK and TSEC2_RTX_CLK. Removed the note for EC_MDIO pin.<br>• In Table 15, added the 4.7 kΩ to OV$_{DD}$ for pin LGPL4/LGTA/LUPWAIT. |
| 9 | 05/2010 | • Added Section 6.2.2, "DDR1 Considerations in Revision 3.x."<br>• Added Section 6.2.3, "Unused Signals Considerations for Both DDR1 and DDR2."<br>• Added Section 6.2.4, "MVREFn Connection Options." |
| 8 | 05/2008 | • In Table 11, change unused pin PCI2_GNT[1:2]/GPIO[10:11] to "2 k–10 kΩ to OV$_{DD}$."<br>• In Table 15, change unused pin LDP[2:3] to "2 k–10 kΩ to OV$_{DD}$." |
| 7 | 11/2007 | • In Table 21, edited and added eTSEC1 rows and added a note. Added "X" in critical column. |
| 6 | 08/2007 | • Thoroughly updated Section 5, "JTAG and Debug"<br>• There were several input signals that were either left floating or not specified. We updated these signals to ensure that unused inputs are either tied to GND or VDD. They cannot be left floating. |
| 5 | 04/2007 | • Table 15: Added a note explicitly stating that If the HRCW is loaded through the local bus, the LA[27:31 pins are used and not the LAD[27:31] pins. The LAD[27:31] pins are not driven during HRCW loading.<br>• Also included this information in Section 4.2, "Reset Configuration Words." |

**Table 25. Document Revision History (continued)**

| Rev. Number | Date | Substantive Change(s) |
|:---:|:---:|:---|
| 4 | 01/2007 | • Table 4: Added footnote 1 to $AV_{DD3}$. |
| 3 | 12/2006 | • Added Section 6.2.1, "SPARE1/MDIC1 and SPARE2/MDIC0."<br>• Changed all Rev. 2 Silicon references to Rev. 3 Silicon.<br>• Modified Figure 3. |
| 2 | 06/2006 | • Modified Figure 3.<br>• Section 2.3, added a sentence to the end of the first paragraph.<br>• Section 2.3, updated the note following the first paragraph.<br>• Table 11, modified PCI1_AD[31:0] and PCI2_AD[31:0] rows. |
| 1 | 01/2006 | • Section 2.1, added Note after Table 2.<br>• Table 10, modified THERM0 row.<br>• Table 11, modified PCI1_GNT2 and M66EN rows.<br>• Table 12, modified MECC[0:4], MECC[5], MECC[6:7], MDQS[0:3], MDQS[4:7], and MDQS[8] rows.<br>• Table 14, modified LDP[2:3] row. |
| 0 | 12/2005 | Initial release. |

*How to Reach Us:*

**Home Page:**
www.freescale.com

**Web Support:**
http://www.freescale.com/support

**USA/Europe or Locations Not Listed:**
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

**Europe, Middle East, and Africa:**
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

**Japan:**
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

**Asia/Pacific:**
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

**For Literature Requests Only:**
Freescale Semiconductor
   Literature Distribution Center
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
   @hibbertgroup.com

Document Number: AN2931
Rev. 10
01/2011