Freescale Semiconductor
Application Note

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Migration from MPC834x Revision 1.x to Revision 3.x

by *Networking and Multimedia Group*
Freescale Semiconductor, Inc.
Austin, TX

1 Overview

MPC834x revision 3.x supersedes revision 1.x. This revision is hardware backward-compatible with the previous revisions, but requires some changes in software. Additional features, such as DDR2 and DMA external support, are added based on customer feedback.

This document outlines the differences between silicon revisions 1.x and 3.x with respect to software, hardware, internal module revision, and chip pin assignment. It also provides information for board designers migrating from revision 1.x to 3.x. This document is relevant for both software and hardware developers.

This document is not intended to replace the latest silicon or reference manual errata. Please check the Freescale website at www.freescale.com for the latest versions of errata and related documents.

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2 New Features

The following new features are available in revision 3.x:

- The errata in revision 1.x have been fixed with the exception of LBC2 and TSEC20. TSEC7 was not removed because customers can adjust the delay to meet the specification when doing PCB layout. See MPC834x device errata.
- Four local bus chip select signals were added: LCS[4:7]. These signals are multiplexed with LDP and SPI pins. It is now possible to connect to additional memory devices.
- New DDR2 SDRAM support features:
  - Low power
  - Driver impedance calibration
  - On-die termination (ODT)
  - Faster than DDR1
- For the DDR controller, the optional $\overline{\text{MDQS}}$ pins are not implemented. These pins are not required at frequencies < ~533MHz; single-ended MDQS, instead of differential MDQS, has been implemented.
- PCI is upgraded to PCI 2.3.
- Four sets of external DMA handshake signals, one set per channel, have been added to support direct data transfer between external memory devices and peripherals. The signals are $\overline{\text{DMA\_DREQ}}$[0:3], $\overline{\text{DMA\_DACK}}$[0:3] and $\overline{\text{DMA\_DDONE}}$[0:3].
- Security enhancements:
  - SEC revision 2.4 is implemented.
  - MDEU (message digest execution unit) SHA-224 support added
  - Storage/NAS enhancements:
    - XOR parity generation accelerator for RAID applications
    - Battery backup support added

3 Software Differences

This section lists important software programming differences between revision 1.x and revision 3.x. Note that the processor version, system version, and REVID values have changed. See Section 5, “PVR, SVR, and REVID Values in the Various Revisions,” for the updated values.

3.1 DDR Software Setting Changes

Table 1 lists important changes to the DDR programming model and to register settings between revision 1.x and revision 3.x. Although most of the registers values require no change when migrating from revision 1.x to 3.x, the user is strongly encouraged to go through Table 1 in detail and find the most appropriate settings for the specific memory device in use.

Table 1. DDR1 Software Setting Changes

Register	Offset	Field	Bits	Change
TIMING_CFG_1	0x0_2108	ACTTOPRE (activate-to-precharge interval)	4–7	Fields have different setting selections in revision 3.x. The default setting for ACTTOPRE (0000) is no longer reserved in revision 3.x. The default 16 clocks work on DDR1. The REFREC setting (0000) valid in revision 1.x is removed in revision 3.x.
		REFREC (refresh recovery time)	16–19	
TIMING_CFG_2	0x0_210C	CPO (CAS to preamble override)	4–8	One extra bit (bit 8) has been added in revision 3.x to add additional granularities. A setting valid in revision 1.x (1011) is not available in revision 3.x. The default setting works on DDR1 since READ_LAT = CAS latency + ADD_LAT, where ADD_LAT = 0 clocks on reset.
		ACSM (address and control shift mode)	12[1]	Field was removed in revision 3.x. This bit is now part of WR_LAT field.
		WR_LAT (write latency)	10–12	New field. Write latency for DDR1 is fixed at 1 clock; thus, WR_LAT should be set to 001 (or 000 for silicon 1.x backward compatibility).[2]
		RD_TO_PRE (read to precharge)	16–18	New field. For DDR1 with burst length of 4, RD_TO_PRE should be set to 010; for DDR1 with burst length of 8, it should be set to 100. The default setting (000) will give you either 2 or 4 cycles depending on your DDR_SDRAM_CFG[8_BE] setting. The RD_TO_PRE is 2 cycles, if 4-beat bursts is programmed. It is 4 cycles, if 8-beat bursts is programmed.
		CKE_PLS (minimum CKE pulse width)	23–25	New field. Can be set to 001 (or 000 for silicon 1.x backward compatibility).[2]
		FOUR_ACT (window for four activates)	26–31	New field. Should be set to 000001 (or 000000 for silicon 1.x backward compatibility).[2]
DDR_SDRAM_CLK_CNTL	0x0_2130	SS_EN (source synchronous enable)	0[1]	Field was removed in revision 3.x; controller operates source-synchronously by default. Program SS_EN on rev 3.x has no effect.

Table 1. DDR1 Software Setting Changes (continued)

Register	Offset	Field	Bits	Change
DEBUG_1	0x0_2F00[1]	—	—	Register has been re-defined. Do not write to this register. Field IR (issue refresh, bit 25 in revision 1.x) is no longer necessary. Field BI (bypass initialization, bit 31 in revision 1.x) is re-located to DDR_SDRAM_CFG[31].

Note:

1 Applies to silicon rev 1.x only.

2 Refer to Section 9.6.1, “Programming Differences Between Memory Types,” in *MPC8349EA PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*, Rev. 1.

3.2 New DDR Fields and Registers in Revision 3.x

Table 2 lists registers and register fields new to revision 3.x.

Table 2. New Registers and Fields

Register	Offset	Field	Bits	Change
CS*n*_CONFIG	0x0_2000 0x0_2008 0x0_2010 0x0_2018	ODT_RD_CFG (ODT for reads configuration)	9–11	New field; previously reserved. Only use for DDR2.
		ODT_WR_CFG (ODT for writes configuration)	13–15	New field; previously reserved. Only use for DDR2.
		BA_BITS_CS_*n* (number of bank bits on chip select *n*)	16–17	New field; previously reserved. Must be set to 00 for DDR1.
TIMING_CFG_3	0x0_2100	—	—	New register
TIMING_CFG_0	0x0_2104	—	—	New register
TIMING_CFG_1	0x0_2108	CASLAT (CAS latency)	12–15	Field has expanded by 1 bit (bit 12, previously reserved). New bit setting(s) are now available: 1000 4.5 clocks 1001 5 clocks ……. 1111 8 clocks
		ACTTOACT (activate-to-activate interval)	25–27	Field has new settings (previously reserved): 101 5 clocks 110 6 clocks 111 7 clocks
TIMING_CFG_2	0x0_210C	ADD_LAT (additive latency)	1–3	Field was previously reserved. Use only for DDR2.
		CPO ($\overline{\text{MCAS}}$-to-preamble override)	4–8	Field has expanded by 1 bit (bit 8, previously reserved). Note new settings added (see manual).
		WR_DATA_DELAY (write command to data strobe timing)	19–21	Field has new settings (previously reserved): 101 5/4 clock delay 110 3/2 clock delay

Table 2. New Registers and Fields (continued)

Register	Offset	Field	Bits	Change
DDR_SDRAM_CFG	0x0_2110	SDRAM_TYPE (RAM type)	5–7	Field has expanded by 1 bit (bit 5, previously reserved). DDR_2 setting now added: 011 (default is 010, DDR_1)
		BA_INTLV_CTL (bank interleaving control)	17–23	New fields (previously reserved: all zeros)
		x32_EN (x32 enable)	26	
		PCHB8 (precharge bit 8 enable)	27	
		HSE (half-strength drive enable)	28	
		MEM_HALT (DDR memory controller halt)	30	
		BI (bypass initialization)	31	
DDR_SDRAM_CFG_2	0x0_2114	—	—	New register; default all zeros
DDR_SDRAM_MODE_2	0x0_211C	—	—	New register; default all zeros
DDR_SDRAM_MD_CNTL	0x0_2120	—	—	New register; default all zeros
DDR_SDRAM_INTERVAL	0x0_2124	REFINT (refresh interval)	0–15	Field has expanded by 2 extra bits (bits 0–1 previously reserved).
DDR_DATA_INIT	0x0_2128	—	—	New register; default all zeros
DDR_SDRAM_CLK_CNTL	0x0_2130	CLK_ADJUST (clock adjust)	5–8	Field has expanded by 1 bit (bit 8 previously RESERVED): Note new settings are now available.
DDR_INIT_ADDR	0x0_2148	—	—	New register; default all zeros
DDR_IP_REV1	0x0_2BF8	—	—	New register; read only
DDR_IP_REV2	0x0_2BFC	—	—	New register; read only
ERR_DETECT	0x0_2E40	ACE (automatic calibration error)	24	New field (previously reserved). Report calibration error.
ERR_DISABLE	0x0_2E44	ACED (automatic calibration error disable)	24	New field (previously reserved). Enable report of calibration error.
ERR_INT_EN	0x0_2E48	ACEE (automatic calibration error interrupt enable)	24	New field (previously reserved). Enable interrupt when calibrate error occurs.
CAPTURE_ATTRIBUTES	0x0_2E4C	TSIZ (transaction size)	5–7	Field has expanded by 1 bit (bit 5, previously reserved)

4 Pin Assignments

MPC834x revision 3.x is pin-compatible with the revision 1.x. New pins are either muxed with existing pins or assigned to previously reserved pins. Table 3 lists the MPC834x revision 3.x pin assignments.

Table 3. MPC834x Revision 3.x Pin Assignments

Name	Description	Block	No. of Signals	I/O	Alternate Function	TBGA	PBGA
$\overline{\text{LCS}}$[4]	Chip Selection	LBC	1	O	$\overline{\text{LDP}}$[2]	AN22	H2
$\overline{\text{LCS}}$[5]	Chip Selection	LBC	1	O	$\overline{\text{LDP}}$[3]	AM22	G1
$\overline{\text{LCS}}$[6]	Chip Selection	LBC	1	O	SPIMOSI	AN32	D7
					PCI_CLK_OUT[3]	AN10	W1
$\overline{\text{LCS}}$[7]	Chip Selection	LBC	1	O	SPIMISO	AP33	C7
					PCI_CLK_OUT[4]	AJ11	V3
$\overline{\text{DMA\_DREQ0}}$/GPIO[0]	DMA Request	DMA	1	I	GTM1_TIN1/GTM2_TIN2	F24	D27
$\overline{\text{DMA\_DACK0}}$/GPIO[1]	DMA Acknowledge	DMA	1	O	$\overline{\text{GTM1\_TGATE1}}$/ $\overline{\text{GTM2\_TGATE2}}$	E24	E26
$\overline{\text{DMA\_DDONE0}}$/GPIO[2]	DMA Done	DMA	1	I	GTM1_TOUT1	B25	D28
$\overline{\text{DMA\_DREQ1}}$/GPIO[3]	DMA Request	DMA	1	I	GTM1_TIN2/GTM2_TIN1	D24	G25
$\overline{\text{DMA\_DACK1}}$/GPIO[4]	DMA Acknowledge	DMA	1	O	$\overline{\text{GTM1\_TGATE2}}$/ $\overline{\text{GTM2\_TGATE1}}$	A25	J24
$\overline{\text{DMA\_DDONE1}}$/GPIO[5]	DMA Done	DMA	1	I	GTM1_TOUT2	B24	F26
$\overline{\text{DMA\_DREQ2}}$/GPIO[6]	DMA Request	DMA	1	I	GTM1_TIN3/GTM2_TIN4	A24	E27
$\overline{\text{DMA\_DACK2}}$/GPIO[7]	DMA Acknowledge	DMA	1	O	$\overline{\text{GTM1\_TGATE3}}$/ $\overline{\text{GTM2\_TGATE4}}$	D23	E28
$\overline{\text{DMA\_DDONE2}}$/GPIO[8]	DMA Done	DMA	1	I	GTM1_TOUT3	B23	H25
$\overline{\text{DMA\_DREQ3}}$/GPIO[9]	DMA Request	DMA	1	I	GTM1_TIN4/GTM2_TIN3	A23	F27
$\overline{\text{DMA\_DACK3}}$/GPIO[10]	DMA Acknowledge	DMA	1	O	$\overline{\text{GTM1\_TGATE4}}$/ $\overline{\text{GTM2\_TGATE3}}$	F22	K24
$\overline{\text{DMA\_DDONE3}}$/GPIO[11]	DMA Done	DMA	1	I	GTM1_TOUT4	E22	G26
MODT[0:3]	DDR On-Die Termination	DDR2	4	O	—	AH3 AJ5 AH1 AJ4	AG5 AD4 AH6 AF4
MDIC1	Driver Impedance Calibration	DDR2	1	I/O	—	AA1	AF12
MDIC0	Driver Impedance Calibration	DDR2	1	I/O	—	AB1	AG11
MBA[2]	DDR2 Address Bank	DDR2	1	O	—	H4	AD22

Note:

1. In revision 1.x, MODT[0:3] and MBA[2], SPARE1, and SPARE2 are pre-reserved pins.
2. In revision 3.x, MDIC1 and MDIC0 correspond, respectively to SPARE1 and SPARE2 in revision 1.x.
3. In revision 3.x, tying MDICO to GND using an 18-Ω resistor and MDIC1 to DDR power using an 18-Ω resistor is recommended.
4. In revision 3.x, AVDD3 (AF9 in PBGA, and AE1 in TBGA) should be NC. However, for customer who is migrating from revision 1.x to revision 3.x using existing board layout, it is still okay to leave them connected to the 1.2v. No layout change is required.

5 PVR, SVR, and REVID Values in the Various Revisions

New PVR and SVR values have been assigned based on the processor and system revisions. Their values are listed in Table 4.

Table 4. PVR and SVR Values

Device	Package	SVR			PVR		
		Rev1.0	Rev1.1	Rev3.1	Rev1.0	Rev1.1	Rev3.1
MPC8349E	TBGA	8050_0010	8050_0011	8050_0030	8083_0010	8083_0011	8083_0031
MPC8349		8051_0010	8051_0011	8051_0030	8083_0010	8083_0011	8083_0031
MPC8347E		8052_0010	8052_0011	8052_0030	8083_0010	8083_0011	8083_0031
MPC8347		8053_0010	8053_0011	8053_0030	8083_0010	8083_0011	8083_0031
MPC8347E	PBGA	8054_0010	8054_0011	8054_0030	8083_0010	8083_0011	8083_0031
MPC8347		8055_0010	8055_0011	8055_0030	8083_0010	8083_0011	8083_0031
MPC8343E		8056_0010	8056_0011	8056_0030	8083_0010	8083_0011	8083_0031
MPC8343		8057_0010	8057_0011	8057_0030	8083_0010	8083_0011	8083_0031

Additionally, the value returned in SPRIDR[REVID] has changed from 0x0101 (revision 1.x) to 0x0300 (revision 3.x).

6 Configuration of Newly Added Functions

The new local bus chip selects are muxed with other functionality on this device. The SICRL and SICRH registers must be configured correctly if the chip selects are to be used. SICRL and SICRH control the multiplexing of the device I/O pins. All newly added pins are configured in these registers. Table 5 and Table 6 show how to configure the SICRL and SICRH registers.

Table 5 defines the bit fields of SICRL. Each Pin Function column lists the name of the multi-function pin used in this option. Some groups have only two options (shown as Pin Function 0 and Pin Function 1) and therefore only one control bit. In this case they can only have a value of 0b0 or 0b1. Other groups may have four options (shown as Pin Function 0, Pin Function 1, Pin Function 2, and Pin Function 3), and therefore two control bits. In this case they can have a value of 0b00, 0b01, 0b10 or 0b11.

Table 5. Configuration Settings for the SICRL Register

SICRL [Bits] Value		0b0/0b00	0b1/0b01	0b10	0b11
Bits	**Group**	**Pin Function 0**	**Pin Function 1**	**Pin Function 2**	**Pin Function 3**
0	LDP_A	$\overline{\text{LCS}}$[5]	LDP[3]	—	—
		$\overline{\text{LCS}}$[4]	LDP[2]	—	—
		$\overline{\text{CKSTOP\_IN}}$	LDP[1]	—	—
		$\overline{\text{CKSTOP\_OUT}}$	LDP[0]	—	—
3	SPI	SPIMOSI	$\overline{\text{LCS}}$[6]	—	—
		SPIMISO	$\overline{\text{LCS}}$[7]	—	—
11–12	GPIO1_F	GPIO[5]	$\overline{\text{GTM1\_TOUT2}}$	$\overline{\text{GTM2\_TOUT1}}$	$\overline{\text{DMA\_DDONE1}}$
18–19	GPIO1_L	GPIO[11]	$\overline{\text{GTM1\_TOUT4}}$	$\overline{\text{GTM2\_TOUT3}}$	$\overline{\text{DMA\_DDONE3}}$
20	DMA_A	Controlled by SICRL[6]	$\overline{\text{DMA\_DREQ0}}$	—	—
21	DMA_B	Controlled by SICRL[7]	$\overline{\text{DMA\_DACK0}}$	—	—
22	DMA_C	Controlled by SICRL[8]	$\overline{\text{DMA\_DDONE0}}$	—	—
23	DMA_D	Controlled by SICRL[9]	$\overline{\text{DMA\_DREQ1}}$	—	—
24	DMA_E	Controlled by SICRL[10]	$\overline{\text{DMA\_DACK1}}$	—	—
25	DMA_F	Controlled by SICRL[13]	$\overline{\text{DMA\_DREQ2}}$	—	—
26	DMA_G	Controlled by SICRL[14]	$\overline{\text{DMA\_DACK2}}$	—	—
27	DMA_H	Controlled by SICRL[15]	$\overline{\text{DMA\_DDONE2}}$	—	—
28	DMA_I	Controlled by SICRL[16]	$\overline{\text{DMA\_DREQ3}}$	—	—
29	DMA_J	Controlled by SICRL[17]	$\overline{\text{DMA\_DACK3}}$	—	—

Table 6 defines the bit fields of SICRH.

Table 6. Configuration Settings for the SICRH Register

SICRH [Bits] Value		0b0/0b00	0b1/0b01	0b10	0b11
Bits	**Group**	**Pin Function 0**	**Pin Function 1**	**Pin Function 2**	**Pin Function 3**
27	PCI	PCI_CLK_OUT[3:4]	$\overline{\text{LCS}}$[6:7]	—	—

7 DDR1 Considerations in Revision 3.x

Customers using DDR1 in revision 3.x, either migrating from revision 1.x to revision 3.x or considering a new design with DDR1, should follow the recommendations provided in this section for a successful DDR1 interface operation in their system.

1. The DDR1 driver strength should be set to half strength on both the memory controller side and the DRAM side. This is done to reduce the overall system noise by setting the following registers:
   - (Offset 0x0_0128) DDRCDR = 0x0004_0001
   - (Offset 0x0_2110) DDR_SDRAM_CFG [HSE] =0’b1
   - (Offset 0x0_2118) DDR_SDRAM_MODE [bit 14] =0’b1
2. The termination scheme should be set to reduce the overall system noise on DDR1 interface. This is done by using the following termination scheme:
   - For all MDQ/MDQS/MDM signals the parallel termination resistor RTT = 100 Ω, and the series resistor RS = 10 Ω.
   - For All address/command/control signals the parallel termination resistor RTT = 150 Ω and series resistor RS = 22 Ω.
   - All unused clock signals should disabled via (Offset 0x0_1010) MCKENR register.
   - All unused ECC signals should be connected to GND via a 150-Ω resistor.

NOTE

The existing recommendations on proper layout for DDR1 as stated in application note AN2582 should be observed.

It is highly recommended to repeat the IBIS simulation with the new IBIS model that is modified for the silicon revision 3.x

8 Board-Level and Timing Changes Between Revision 1.x and Revision 3.x

Customers using revision 1.x silicon who want to upgrade to revision 3.x silicon without DDR2, can simply replace the chip without any modification of the board.

Beginning with MPC8349ERMAD, Rev. 1.2, 08/2006 and MPC8349EARM, Rev. 1, 08/2006 there has been a documented requirement to ensure that TSEC1_TXD3 is pulled up with an external resistor or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net. Users who are upgrading to revision 3.x silicon are advised to refer to the documentation and ensure that these requirements are being met by their board designs.

For customers using DDR2, two spare pins (SPARE1 and SPARE2) in Rev. 1.x silicon are now used for input impedance calibration for DDR2 in Rev. 3.x. As long as the user uses DDR1, MDIC0/MDIC1 act as spares and terminations for these two pins follow the SPARE2/SPARE1 termination recommendations for Rev. 1.x as indicated in Table 7. Likewise, if user selects DDR2, the terminations follow the MDIC0/MDIC1 termination recommendations.

Table 7. SPARE1/MDIC1 and SPARE2/MDIC0 Termination Recommendations

Pins	Rev. 1.x	Rev. 3.x	
	DDR1	DDR1	DDR2
SPARE1 / MDIC1	Open	Open	18 Ω to GV_{DD}
SPARE2 / MDIC0	0 Ω to GND	0 Ω to GND	18 Ω to GND

The user selects between DDR1 and DDR2 by configuring the DDR_SDRAM_CFG[SDRAM_TYPE] and the DDRCDR[DDR_TYPE] registers. Note that both registers are initially configured for DDR1 upon reset. The SDRAM_TYPE = (010) and DDR_TYPE = (1) are the default settings for DDR1. Please do not clear these registers by mistake if you are intended to use DDR1.

Due to the memory controller enhancement made on Rev. 3.x to support DDR2, the input and output DDR1 AC timing specifications between Rev. 1.x and Rev. 3.x will be slightly different. Please compare the timing differences in the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications* and the *MPC8349EA PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications*. User must ensure that timing margins meet the new requirements.

9 Revision History

Table 8 provides a revision history for this application note.

Table 8. Document Revision History

Rev. Number	Date	Substantive Change(s)
6	01/2009	In Section 7, “DDR1 Considerations in Revision 3.x,” changed “(Offset 0x0_0128) DDRCDR = 0x0000_0001,” to say “(Offset 0x0_0128) DDRCDR = 0x0004_0001.”
5	12/2008	Added Section 7, “DDR1 Considerations in Revision 3.x.”
4	01/2008	in Table 1, updated the Change column for register TIMING_CFG_2; fields WR_LAT, CKE_PLS, and FOUR_ACT.
3	11/2007	Inserted new paragraph in Section 7.
2	01/2007	Re-wrote Section 3.1, “DDR Software Setting Changes.” Modified Footnote under Table 3 regarding AVDD3 (pin AE1 or AF9) stating that no layout change is required. Added pin function option description in Section 6, “Configuration of Newly Added Functions.” Added more information in Section 7, “Board-Level and Timing Changes Between Revision 1.x and Revision 3.x.”
1	08/2006	Changed title from “Migration from MPC834x Revision 1.1 to Revision 2.0” to “Migration from MPC834x Revision 1.1 to Revision 3.0.” Section 3, “Software Differences,” updated. Section 5, “PVR, SVR, and REVID Values in the Various Revisions,” updated and new revision IDs added. Section 7, “Board-Level and Timing Changes Between Revision 1.x and Revision 3.x,” added.
0	11/2005	Initial release.

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USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
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Europe, Middle East, and Africa:
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Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
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www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

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