Freescale Semiconductor
Application Note

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PowerQUICC™ III Power Measurements Application Note

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This application note provides an overview of power dissipation concepts with the PowerQUICC III. The concepts of core and I/O power, as well as static and dynamic power, are distinguished. The note provides estimates for the power reduction attained when unused blocks within the PowerQUICC III are disabled. Three methods for estimating the static power consumption of a given device are also described and compared. Effect of temperature over power is also described.

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1 Power Dissipation Concepts

The concepts of power dissipation are outlined in this section. Specifically, the distinction between core and I/O power is discussed. Further separation of the core power component into dynamic and static power components is also explained.

1.1 Core Power vs. I/O Power

The total power dissipation in a PowerQUICC III communication processor includes the core power and the I/O power. In terms of an equation, this can be stated simply as:

$$\textit{Total Power Dissipation} = \textit{Core Power Dissipation} + \textit{I/O Power Dissipation}$$

Eqn. 1

Core power refers to power consumed on the VDD rail. Hence, core power includes not only the power dissipated by the e500 core, but also the various other internal blocks, such as L2 cache, CPM/QE RISC core(s), On-Chip Network, etc.

I/O power refers to power consumed on the following rails: OVDD, GVDD, LVDD, BVDD, and XVDD. When discussing on-chip I/O power consumption, the dissipation in termination resistors is not included.

The PLL supply rail (AxVDD) consumes a relatively small amount of power compared to the total power consumption of the device. PLL supply power dissipation is stated separately from the core and I/O power.

1.2 Dynamic Power vs. Static Power

The core power dissipation in a processor can be conceptually separated into two major components, expressed simply as:

$$\textit{Core Power Dissipation} = \textit{Dynamic Power} + \textit{Static Power}$$

Eqn. 2

Dynamic power arises due to signal transitions and is primarily dependent on clock frequencies. If the clocks are turned off, the dynamic power would be zero. It is also referred to as AC power.

Static power refers to the power dissipation that occurs even when the clocks are not active, and is due to the leakage current that flows from every transistor that is powered on. It is also sometimes referred to as leakage power, sleep power, or DC power. Static power is primarily dependent on core voltage and junction temperature. As transistors become smaller and faster, static power becomes increasingly significant in both its absolute amount and as a proportion of the total core power. The static power of a PowerQUICC III device may be approximated by measuring the core power dissipation when the device is placed into the sleep power-saving mode.

2 Estimated Power Reduction by Disabling Unused Blocks

The PowerQUICC III SoC platform provides a wide variety of functional blocks. These blocks correspond to interfaces such as Ethernet and RapidIO, as well as other functions such as security. Most applications do not use all blocks that are present, but all blocks are enabled after reset by default. In order to reduce power consumption, the PowerQUICC III features the ability to disable unused blocks. This section provides estimates of the power reduction achievable on the VDD supply rail when disabling various blocks.

Blocks that can be powered down are listed in the following table.

Table 1. PowerQUICC III Functional Blocks

MPC8560 / MPC8540	MPC8555E / MPC8541E
PCI	PCI1
—	PCI2
LBC	
—	SEC
RIO	—
CPM	
DMA	
TSEC1	
TSEC2	
I2C	
—	DUART

2.1 Methodology and Assumptions

Powering down a block is achieved by writing to the Device Disable Register (DEVDISR) appropriately. Note that disabled blocks must not be re-enabled without a hard reset.

Powering down a block via the DEVDISR turns off all clocks to that block. Thus, dynamic power consumption on the VDD rail is reduced, but static power on the VDD rail is not affected. Only the power savings on the VDD rail was studied; the corresponding effect on I/O power supplies, if any, were not measured.

To measure the power reduction achievable, a first measurement is made under the following conditions:

- An 85xxADS was used with the device running the Dhrystone 2.1 benchmark in an infinite loop with all blocks enabled.
- The case temperature was held at 105°C.
- The core voltage was set to VDD=1.2V.

A second measurement is then made under the same temperature, voltage, and frequency conditions, while also running Dhrystone 2.1, but with the desired block disabled. The Dhrystone benchmark is downloaded to the device via the JTAG interface using PowerTAP Pro. The Dhrystone benchmark has additional initialization code that can be used to disable any desired block before the main loop begins.

The power reduction when a block is shut down is dynamic (i.e. AC power) since only the clocks are turned off. Since power is still supplied to the block, static power (i.e. DC power) is still dissipated. Thus, using the same case temperature and voltage between the two measurements ensures that the static power contained in the two measurements is nearly identical. Taking the difference between the two measurements removes the static power portion and provides the dynamic power reduction due to disabling the specific block.

Dynamic power generally has little variance from part to part. Hence, only one MPC8560 device and one MPC8555E device were used to perform this characterization.

Under Dhrystone, except for the e500, note that most of the functional blocks in the device are not very active. Thus, the dynamic power estimate provided for a block corresponds to that block being relatively idle. Note that dynamic power management is always enabled and automatically turns off clocks within a block when sections of the block are idle.

2.2 Measured Results

The measured power reduction on the MPC8560 and MPC8555E when a block is disabled is shown in the table below.

Table 2. Measured Power Reduction

	Measured Power Reduction (W)					
Core:CCB Ratio	**2:1**		**5:2**		**3:1**	
Core/CCB (MHz)	**667/333**		**833/333**		**800/267**	
Disabled Block	**MPC8560**	**MPC8555E**	**MPC8560**	**MPC8555E**	**MPC8560**	**MPC8555E**
PCI	0.184		0.190		0.149	
PCI1		0.149		0.145		0.115
PCI2		0.146		0.146		0.113
LBC	0.083	0.060	0.091	0.066	0.066	0.046
SEC		0.166		0.170		0.133
RIO	0.179		0.191		0.147	
TSEC1	0.130	0.068	0.139	0.088	0.109	0.058
TSEC2	0.131	0.067	0.142	0.086	0.109	0.058
I2C	0.004	0.008	0.013	0.031	0.008	0.002
DUART		0.019		0.041		0.010
CPM	0.868	0.948	1.130	1.230	1.099	1.189
DMA	0.041	0.031	0.052	0.049	0.036	0.026

The data is provided for three different frequency combinations, each corresponding to a unique core-to-CCB ratio.

All MPC8555E results are applicable to the MPC8541E. All MPC8560 results, except for the CPM, also apply to the MPC8540.

Experiments were also conducted to see the effect of disabling multiple blocks. In general, the power reduction is approximately additive, but could be slightly lower. The results are shown in Table 3.

Table 3. Measured Power Reduction from Disabling Multiple Blocks

	Measured Power Reduction (W)					
Core:CCB Ratio	**2:1**		**5:2**		**3:1**	
Core/CCB (MHz)	**667/333**		**833/333**		**800/267**	
Disabled Block	**MPC8560**	**MPC8555E**	**MPC8560**	**MPC8555E**	**MPC8560**	**MPC8555E**
TSEC1 & TSEC2	0.263	0.133	0.273	0.152	0.220	0.108
PCI	0.180	—	0.189	—	0.146	—
PCI1/PCI2	—	0.277		0.274		0.216

The overall conclusion is that disabling unused blocks saves anywhere from a few tens to a few hundred milliwatts of core power, depending on the specific block that is disabled.

3 Methods for Static Power Estimation

Static power for PowerQUICC III devices may be estimated by any of the following methods:

- Extrapolation to zero frequency based on measurements at 2 frequency combinations that have the same core-to-CCB ratio.
- Placing the device in sleep mode.

These methods are discussed in this section, and are applicable to the MPC8540, MPC8560, MPC8555E, and MPC8541E. Measurement results are used to illustrate these methods based on experiments conducted at various times on different devices and boards.

3.1 Extrapolation to Zero Frequency

Estimating the static power of a given device by the method of extrapolation to zero frequency can be performed via the following steps:

- Maintain the case temperature (TC) and the core voltage (VDD) at fixed values throughout all the measurements.
- Run an application such as Dhrystone that has a steady power dissipation (i.e. peak and average power are about the same). Other than having steady power dissipation, other aspects of the application are unimportant.

- Take power measurements at two frequency combinations that have the same core-to-CCB ratio.
- Plot core power against frequency for the two measurements; either core or CCB frequency could be used on the horizontal axis. Draw a line through these two points; the y-intercept of this line provides the static power estimate for the specific device used.

To demonstrate this method, measurements were taken on an MPC8560 while running Dhrystone. The measurements were performed at TC=105 C and VDD=1.2V. The results are tabulated below.

Table 4. Extrapolation to Zero Frequency

Ratio	Core(MHz)	CCB(MHz)	Power(W)
2.0	0	0	2.43
	533	267	6.10
	600	300	6.56
	667	333	7.02
2.5	0	0	2.49
	667	267	6.53
	750	300	7.04
	833	333	7.53
3.0	0	0	2.44
	800	267	6.94
	900	300	7.51
	1000	333	8.07

For the purpose of illustration, the core power was measured at three different core-to-CCB ratios. For each ratio, measurements were taken at three unique frequency combinations (although two would have been sufficient).

The results of extrapolating to zero are shown in the rows where both the core and CCB frequency are shown as zero. These extrapolations were calculated using Microsoft Excel's INTERCEPT function and are all very close to about 2.4W for this device.

The chart below shows plots of the core power against core frequency, one line per core-to-CCB ratio. The y-intercepts of all three lines match closely at about 2.4W.

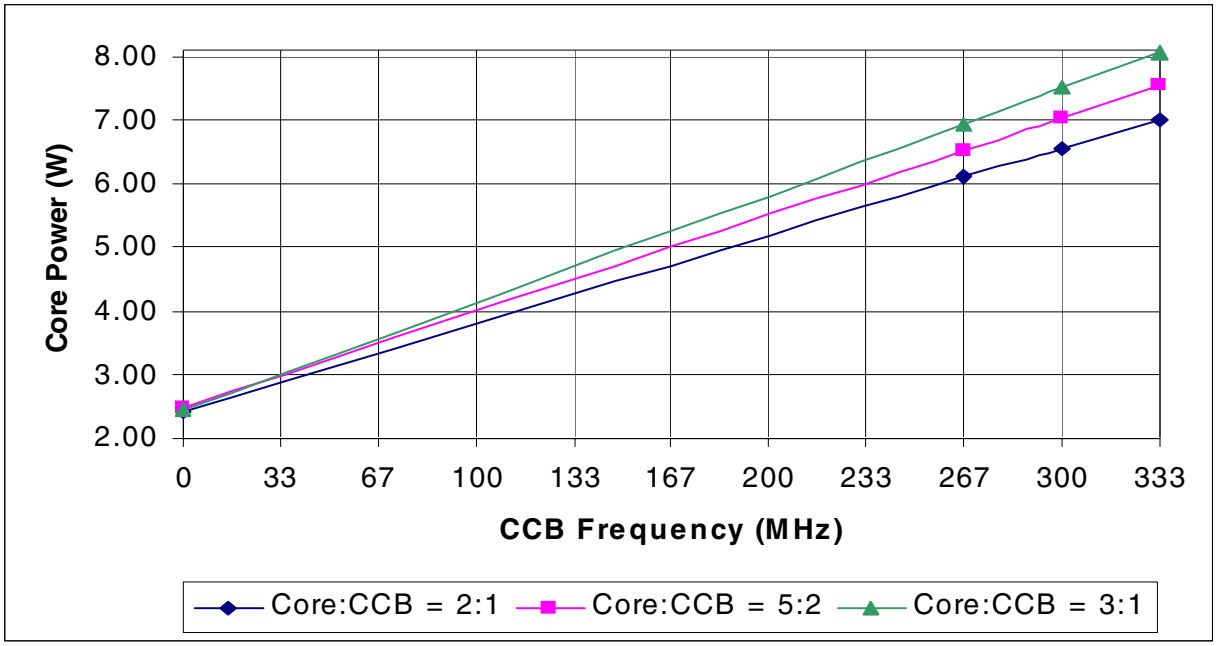

Figure 1. Core Power vs. Core Frequency

This example demonstrates the effectiveness of this technique in that any one core-to-CCB ratio could have been used with measurements taken at two unique frequency combinations.

Note that, regardless of the core-to-CCB ratio used, the y-intercepts should match closely since static power is independent of frequency. Plotting the core power against core frequency instead of CCB frequency will provide identical static power estimates.

3.2 Using Sleep Mode

Placing the part in sleep mode may be achieved via either of the following methods:

- Setting MSR[WE] and HID0[SLEEP]
- Setting POWMGTCSR[SLP]

Refer to the reference manual for the recommended instruction sequence. Note that setting these bits initiates sleep mode. However, in order for the device to successfully reach sleep mode, I/O traffic to the device must be stopped. The logic that controls the power down sequence waits for all I/O interfaces to become idle before stopping the core.

In experiments using the COP debugger with an ADS Pilot board, devices were placed in sleep mode with the cop freeze command supported by the debugger. Sleep power measurements taken with two MPC8555E devices are shown below.

Table 5. MPC8555E Sleep Power Measurements

Core (MHz)	CCB (MHz)	Power (W)	
		Part#1	Part#2
400	200	1.55	2.50
533	267	1.63	2.59
667	333	1.71	2.66

The above results were obtained at TC=110°C and VDD=1.2V at three frequency combinations at the same core-to-CCB ratio of 2:1. The results show the sleep power increasing slightly with frequency.

3.3 Sleep vs. Static Power

The term sleep power is often used synonymously with static power. When a device is placed in a power-saving sleep mode, the vast majority of the device has been shut down, but the interrupt controller is still active so that an interrupt can wake up the device. Hence, sleep power has a small frequency dependence and would be higher than the static power under identical temperature and voltage conditions. In most cases, the difference between sleep and static power is likely to be negligible.

3.4 Correlation of Static Power Among Methods

Table 6 shows the results of experiments that demonstrate good correlation between several methods. Four MPC8560 parts were used in the experiments. All measurements were taken at TC=105°C and VDD=1.2V on an 8560ADS Rev A board. The tester sleep power measurements are also shown in the right-most column; these sleep power values were obtained at TC=110°C and VDD=1.2V. The entries highlighted in light grey correspond to static power estimates, while the entries in dark grey are total power measurements while running an application at the indicated core and CCB frequencies.

Table 6. Comparison of Various Method

Part #	Core (MHz)	CCB (MHz)	Dhrystone Power (W)	UBoot Prompt Power (W)	Tester Sleep at 110 C
1	0	0	2.89	2.84	2.83
	667	267	7.52	6.72	
	833	333	8.68	7.69	
2	0	0	2.59	2.62	2.50
	667	267	7.28	6.49	
	833	333	8.45	7.46	
3	0	0	2.90	2.87	2.81
	667	267	7.49	6.70	
	833	333	8.63	7.65	
4	0	0	2.95	2.97	2.71
	667	267	7.45	6.69	
	833	333	8.58	7.62	

The first and second observations are that the extrapolation to zero frequency method results in similar estimates regardless of the application used. In this case, power measurements were performed while running Dhrystone 2.1 and under an idle UBoot prompt.

Third, the extrapolation method and the production tester sleep power results provide results that differ by 0.06W to 0.26W.

Note that tester-based sleep power measurements and the development board-based estimation methods are not expected to match exactly even if the case temperatures and voltages used are the same. This is due to measurement variances and errors involved in all the measurements. Note the following:

- Sleep measurements in the tester are made at a case temperature of 110°C to provide some test margin in the screening process. However, as with any temperature controlled environment, there can be a few degrees of variance in the actual temperature achieved.
- Sleep power is not the same as static power as discussed earlier.
- When using the ADS board, the Marlow temperature controller contacts the case with some thermal grease applied between them to fill in air gaps. The application of thermal grease by hand does not result in uniform spread and grease layer thickness may differ each time.
- The temperature controller has a circular head while the device case is square, and the head does not cover the entire case.
- It has been observed that results can be slightly different even for the same part under otherwise identical conditions and using the same temperature controller and other measuring instruments. The exact positioning of the temperature controller, thermal grease application and quality of the contact between the temperature controller head and device case are believed to be the primary causes of the variance.

3.5 Junction vs. Case Temperature

The true junction temperature is estimated to be a few degrees higher than the case when the device is powered. Using a linear, one-dimensional thermal model, the junction temperature is:

$$TJ = TC + (RJC \times P)$$

Eqn. 3

where RJC and P are the device junction-to-case thermal resistance and total power dissipation, respectively. RJC is 0.8°C/W and 0.96°C/W for the MPC8540/MPC8560 and MPC8541E/MPC8555E, respectively.

Based on this one-dimensional thermal model, a 8.5W total power dissipation in an MPC8560 would correspond to 6.8°C higher junction than case temperature. In reality, the overall thermal resistance is likely to be slightly lower since the part also dissipates power through the board, etc. Hence, TC=105°C is likely to correspond to a TJ of perhaps 110°C when the total power dissipation is about 8.5W.

3.6 Measurement Guidelines

Some “soak time” is required before taking measurements. It is best that the board and device have been powered up and in use for 10 to 30 minutes before measurements are taken. Based on voltmeter readings that indicate core power, usually less than a minute is required for the temperature controller to stabilize the case temperature when the device frequency or application being run is changed.

The best way to ensure that thermal steady state has been achieved is to measure the resistance across the THERM0/1 pins, although this was not done in the experiments in this paper. This could be another factor adding to the variance of the measurements.

If the voltmeter readings do not appear to be stable even after a few minutes or if the variance of measurements appear to be high under different measurement methods that should provide similar results, the most likely cause is that the temperature controller is not making adequate contact with the device.

4 Core Power Variation with Temperature

PowerQUICC III devices are specified to operate at a junction temperature (TJ) of up to 105°C. Designers often target their thermal design to achieve a target junction temperature a few degrees below 105°C to provide a safety margin. In some cases, even lower target junction temperatures may be desired.

This section provides information on the variation of core power with case temperature based on lab characterization.

While the data is believed to be accurate and representative, no guarantee is provided that all production parts will conform to this characterized data. Furthermore, note that case temperature is used here but recommended operating temperature of the device is specified with respect to the junction.

The maximum core power for different case temperatures at core=833MHz, CCB=333MHz, and VDD=1.2V is shown in the table below for the MPC8555E and MPC8560.

Table 7. Maximum Core Power vs. Case Temperature at Core=833MHz, CCB=333MHz, VDD=1.2V

Case Temperature (C)	MPC8555EMaximum Core Power (W)	MPC8560 Maximum Core Power (W)
25.0	6.8	8.1
30.0	6.8	8.2
35.0	6.9	8.3
40.0	7.0	8.4
45.0	7.1	8.6
50.0	7.2	8.7
55.0	7.3	8.9
60.0	7.5	9.0
65.0	7.6	9.2
70.0	7.8	9.4
75.0	8.0	9.7
80.0	8.1	9.9
82.5	8.2	10.0
85.0	8.3	10.2
87.5	8.4	10.3
90.0	8.5	10.4
92.5	8.7	10.6
95.0	8.8	10.7
97.5	8.9	10.9
100.0	9.0	11.0
102.5	9.2	11.2
105.0	9.3	11.4

5 Summary

The extrapolation method and sleep mode method are recommended for use in estimating static power for a device.

It must be ensured that the case temperature is also measured and/or controlled so as to obtain an accurate measurement since static power varies exponentially with junction temperature.

Similar methods are also expected to work with 90nm PowerQUICC III devices.

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