Freescale Semiconductor
Application Note

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MPC8533E PowerQUICC III Bring-up Guide

This document provides recommendations for new designs based on the MPC8533E PowerQUICC III family of integrated host communications processors (collectively referred to throughout this document as MPC8533E):

- MPC8533E
- MPC8533

This document may also be useful for debugging newly designed systems by highlighting those aspects of a design that merit special attention during initial system startup.

For updates to this document, refer to the website listed on the back cover of this document.

Contents

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1 Introduction

This section outlines recommendations to simplify the first phase of design. Before designing a system with a MPC8533E device, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

1.1 MPC8533E Overview

This section provides a high-level overview of MPC8533E features. Figure 1 shows the major functional units within the device.

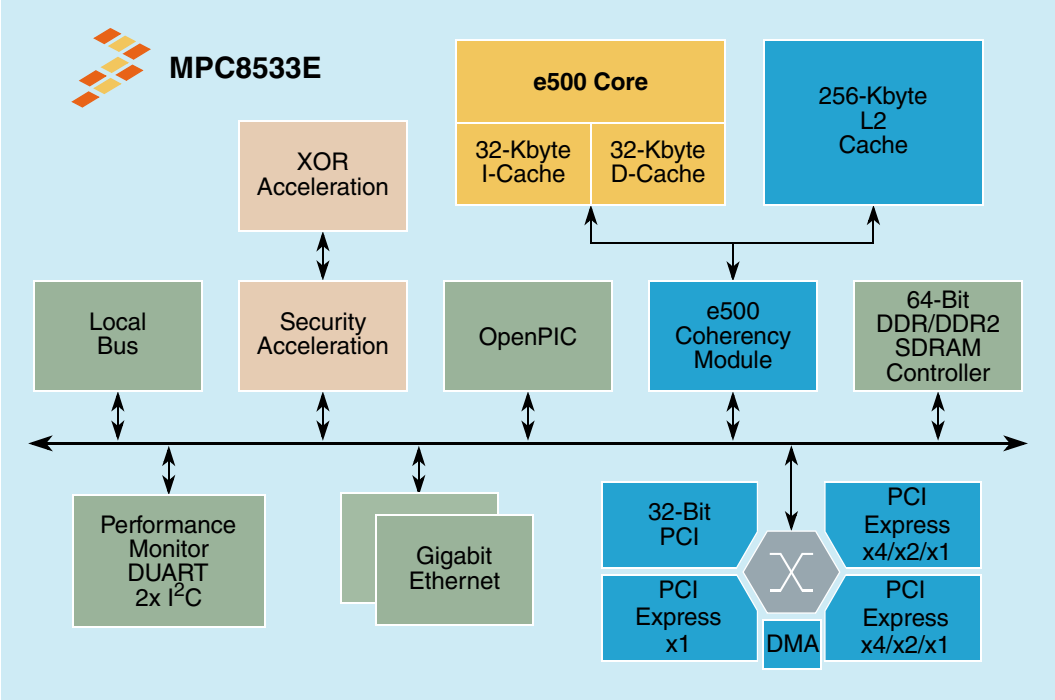


Figure 1. MPC8533E Block Diagram

1.2 References

The following list describes available collateral:

- *MPC8533E PowerQUICC III™ Integrated Host Processor Family Reference Manual* (MPC8533ERM)
- *Errata to MPC8533E PowerQUICC™ III Integrated Host Processor Family Reference Manual* (MPC8533ERMAD)
- *Device Errata for the MPC8533E PowerQUICC™ III* (MPC8533ECE)
- *MPC8533E PowerQUICC III™ Integrated Processor Hardware Specifications* (MPC8533EEC)

- *PowerQUICC™ DDR2 SDRAM Controller Register Setting Considerations* (AN3369)
- *Programming the PowerQUICC™ III/PowerQUICC II Pro DDR SDRAM Controller* (AN2583)
- *Hardware and Layout Design Considerations for DDR Memory Interfaces* (AN2582)
- *Hardware and Layout Design Considerations for DDR2 SDRAM Memory Interfaces* (AN2910)

The following list describes available tools:

- Software
  - Boot sequencer generator tool (I2CBOOTSEQ)
  - UPM Programming tool (LBCUPMIBCG)
- Hardware
  - Development System (MPC8544DS) including schematics, bill of materials, board errata list, User's Guide, and configuration guide

The following list describes available models:

- IBIS
- BSDL
- Flowtherm

1.3 Device Errata

The device errata document MPC8533ECE describes the latest fixes and work arounds for the MPC8533E. The errata document should be thoroughly researched prior to starting a design with the respective MPC8533E device.

1.4 Boot Sequencer Tool

The MPC8533E features the boot sequencer to allow configuration of any memory-mapped register before the completion of power-on reset (POR). The register data to be changed is stored in an I^2C EEPROM. The MPC8533E requires a particular data format for register changes as outlined in the MPC8533ERM. The boot sequencer tool (I2CBOOTSEQ) is a C-code file. When compiled and given a sample data file, it will generate the appropriate raw data format as outlined in the MPC8533ERM. The file that is generated is an s-record file that can be used to program the EEPROM.

1.5 UPM Programming Tool

The UPM Programming Tool (LBCUPMIBCG) features a GUI for a user-friendly programming interface. It allows programming of all three of the MPC8533E's UPM machines. The GUI consists of a wave editor, a table editor, and a report generator. The user can edit the waveform directly or the RAM array directly. At the end of programming, the report generator will print out the UPM RAM array that can be used in a C-program.

1.6 Available Training

Our third-party partners are part of an extensive Design Alliance Program. The current training partners can be found on our website under Design Alliance Program at www.freescale.com/alliances.

Training material from past Smart Network Developer's Forums and Freescale Technology Forums are also available. These trainings modules are a valuable resource for understanding the MPC8533E. This material is available at our website listed on the back cover of this document.

1.7 Product Revisions

Table 1 lists the processor version register (PVR) and system version register (SVR) values for the various MPC8533E derivatives of silicon.

Table 1. MPC8533E PowerQUICC III Product Revisions

Device Number	Device Revision	e500 v2 Core Revision	Processor Version Register Value	System Version Register Value	Note
MPC8533E	1.0	2.1	0x8021_0021	0x803C_0010	With Security
MPC8533	1.0	2.1	0x8021_0021	0x8034_0010	Without Security
MPC8533E	1.1/1.1.1	2.2	0x8021_0022	0x803C_0011	With Security
MPC8533	1.1/1.1.1	2.2	0x8021_0022	0x8034_0011	Without Security

2 Power

This section provides design considerations for the power supplies and power sequencing. For information on AC and DC electrical specifications and thermal characteristics, refer to the MPC8533EEC Hardware Specification document.

2.1 Power Supplies

The MPC8533E has a core voltage V_{DD} and SerDes voltages SV_{DD} and XV_{DD} that operate at a lower voltage than the I/O voltages BV_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and TV_{DD}. The core voltage, 1.0 V (±5%), is supplied across V_{DD} and GND.

The I/O blocks are supplied with the following:

- 1.8 V (±5%) or 2.5 V (±5%) or 3.3 V (±5%) across BV_{DD} and GND
- 1.8 V (±5%) or 2.5 V (±5%) across GV_{DD} and GND
- 2.5 V (±5%) or 3.3 V (±5%) across LV_{DD} and GND
- 3.3 V (±5%) across OV_{DD} and GND
- 1.0 V (±5%) across SV_{DD} and GND
- 2.5 V (±5%) or 3.3 V (±5%) across TV_{DD} and GND
- 1.0 V (±5%) across XV_{DD} and GND

Both LV_{DD} and TV_{DD} are used to supply the eTSEC interfaces on the device: LV_{DD} manages eTSEC1, and TV_{DD} manages eTSEC3. For the respective eTSEC, LV_{DD}/TV_{DD} equals the following:

- 3.3 V or 2.5 V for GMII, MII, RMII, TBI, or FIFO modes of operation
- 2.5 V for RGMII or RTBI modes of operation

2.2 Power Consumption

Operating mode power dissipation numbers (typical) are provided in the MPC8533EEC Hardware Specification. Typical and thermal numbers are provided to assist in the thermal design for the device. If the targeted junction temperature (T_J) of the MPC8533E in the system is not one of these two temperatures, a linear extrapolation of these two TYPICAL dissipation values can be used to estimate the power dissipation at the targeted junction temperature.

The maximum assists with the power supply design selection.

2.2.1 Low Power Modes Power Dissipation

A low-power mode estimates provided in Table 2 for applications concerned about minimizing power consumption when the MPC8533E core is not active.

Table 2. Low-Power Estimates

Low Power Modes	Core/CCB Frequency			
	667/333 MHz	800/400 MHz	1000/400 MHz	1067/533 MHz
SLEEP	1.50 W	1.55 W	1.55 W	1.6 W
NAP	1.75 W	1.80 W	1.90 W	2.0 W
DOZE	2.20 W	2.35 W	2.6 W	2.7 W

NOTE

The typical, thermal, and maximum power numbers are based on the power dissipation on the 1.0 V nominal V_{DD} supply only. Typical power dissipation estimates on the peripheral supplies (BV_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, TV_{DD}, and XV_{DD}) are provided in MPC8533EEC.

2.2.2 I/O Power Dissipation

Because I/O usage varies from design to design, power dissipation estimates for the I/O supplies are provided in Table 3.

Table 3. Estimated I/O Power Dissipation

Interface	Parameters	1.0 V (XV_{DD})	1.8 V (GV_{DD})	2.5 V ($B/G/LV_{DD}$)	3.3 V ($B/L/OV_{DD}$)	Comments
DDR	333 MHz data	—	0.38 W	0.73 W	—	—
	400 MHz data	—	0.46 W	—	—	
	533 MHz data	—	0.60 W	—	—	
PCI Express	x4, 2.5 G-baud	0.36 W	—	—	—	—
PCI	32-bit, 66 MHz	—	—	—	0.07 W	Power per PCI port
	32-bit, 33 MHz	—	—	—	0.04 W	
Local bus	32-bit, 133 MHz	—	—	0.14 W	0.24 W	—
	32-bit, 66 MHz	—	—	0.07 W	0.13 W	
	32-bit, 33 MHz	—	—	0.04 W	0.07 W	
eTSEC (10/100/1000 Ethernet)	MII	—	—	—	0.01 W	Power per eTSEC used
	GMII	—	—	—	0.07 W	
	TBI	—	—	—	0.07 W	
	RGMII	—	—	0.04 W	—	
	RTBI	—	—	0.04 W	—	
eTSEC (packet FIFO)	8-bit, 200 MHz	—	—	0.11 W	—	Power per FIFO interface used
	8-bit, 155 MHz	—	—	0.08 W	—	

2.3 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. Per the MPC8533EEC document, the requirements for power-up are as follows:

1. V_{DD}, AV_{DD}_n, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD}, TV_{DD}, XV_{DD}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

The purpose of the sequence is to guarantee the state of the DDR signals at reset. In order to guarantee MCKE low during power-up (as should be *attempted* per the JEDEC JESD79-2C specification), the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing of GV_{DD} is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

2.4 PLL Power Supply Filtering

Each of the PLLs is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_PCI, AV_{DD}_LBIU, and AV_{DD}_SRDS respectively). Preferably these voltages will be derived directly from V_{DD} through a low-frequency filter scheme.

While there are a number of ways to reliably provide power to the PLLs, the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 2, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. If the PCI is run in synchronous mode, no filter is required for AV_{DD}_PCI.

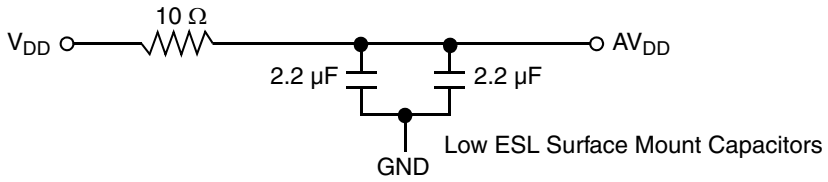
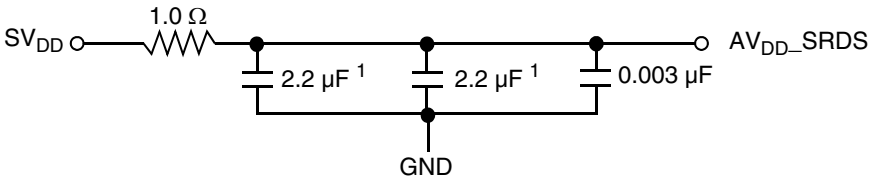


Figure 2. PLL Power Supply Filter Circuit

The AV_{DD}_SRDSn signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 3. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDSn balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDSn balls. The 0.003-µF capacitor is closest to the balls, followed by the 1-µF capacitor, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDSn to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. If the SerDes is not used, a filter for AV_{DD}_SRDS is not required.



1. An 0805 sized capacitor is recommended for system initial bring-up.
2. AVDD_SRDS should be a filtered version of SVDD.
3. Signals on the SerDes interface are fed from the XVDD power plane.

Figure 3. SerDes PLL Power Supply Filter

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits.

These filters are a necessary extension of the PLL circuitry and are to what the device is specified. Any deviation from the recommended filters are done at the customer's risk.

2.5 Power Supply Decoupling

The MPC8533E requires a clean, tightly regulated source of power. The system designer should place at least one decoupling capacitor at each V_{DD} and B/G/L/O/TV_{DD} pin of the device. These decoupling capacitors should have a value of 0.01 or 0.1 µF and receive their power from separate V_{DD}, B/G/L/O/TV_{DD} and GND power planes in the PCB, utilizing short traces to minimize inductance.

In addition, several bulk storage capacitors should be distributed around the PCB to feed the V_{DD} and B/G/L/O/TV_{DD} planes, to enable quick recharging of the smaller chip capacitors.

The capacitors should be placed as close as possible to the processor. The capacitors need to be selected to work well with the power-supply so as to be able to handle the MPC8533E's dynamic load requirements. The customer should work closely with their power-supply vendor to choose for the correct value and type of capacitors for good and clean power.

If the SerDes is used, it requires a clean, tightly-regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver:

- The board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device.
- There should be a 1-µF ceramic chip capacitor from each SerDes supply (SV_{DD} and XV_{DD}) to the board ground plane on each side of the device.
- Between the device and any SerDes voltage regulator there should be a 10-µF, low ESR SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

2.6 Power Supplies Checklist

Table 4 provides a summary power supply checklist for the designer.

Table 4. Power Supplies Checklist

Item	Description	Completed
1	All power supplies have a voltage tolerance no greater than 5% from the nominal value.	
2	eTSEC supplies are chosen according to the mode of operation used.	
3	Power supply selected is based on MAXIMUM power dissipation.	
4	Thermal design is based on TYPICAL power dissipation.	
5	Power-up sequence is less than 50 ms.	
6	Power sequencing is understood and based on whether or not latch-up or garbage data written to DDR is a concern	
7	Recommended PLL filter circuit is applied to AV_{DD}_PLAT, AV_{DD}_CORE, and AV_{DD}_LBIU.	
8	If PCI is used in asynchonous mode, then the recommended PLL filter circuit is applied to AV_{DD}_PCI. However, If the PCI is used in synchronous mode, no filter is required for AV_{DD}_PCI.	
9	If SerDes is used, then the recommended PLL filter circuit is applied to AV_{DD}_SRDS. However, If the SerDes is not used, a filter for AV_{DD}_SRDS is not required	
10	PLL filter circuits are placed as close to the respective AV_{DD} pin as possible.	

Table 4. Power Supplies Checklist (continued)

Item	Description	Completed
11	Decoupling capacitors of 0.01 or 0.1 µF are placed at each V_{DD}, B/G/L/O/TV_{DD} pin.	
12	Bulk capacitors are placed on each V_{DD}, B/G/L/O/TV_{DD} plane.	
13	If SerDes is used, the recommended decoupling for S/XV_{DD} is used.	

3 Power-on Reset and Reset Configurations

This section discusses reset configurations.

3.1 Configuration and Timing

Various device functions are initialized by sampling certain signals during the assertion of HRESET. These power-on reset (POR) inputs are either pulled high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while HRESET is asserted. HRESET must be asserted for a minimum on 100 µs. When HRESET de-asserts, the configuration pins are sampled and latched into registers and the pins then take on their normal output circuit characteristics.

Most of the configuration pins have an internally gated 20 kΩ pull-up resistor, enabled only during HRESET. For those configurations in which the default state is desired, no external pull-up is required. Otherwise, a 4.7 kΩ pull-down resistor is recommended to pull the configuration pin to a valid logic low level. In the case where a configuration pin has no default, 4.7 kΩ pull-up or pull-down resistors are recommended for appropriate configuration of the pin.

An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device which drives the configuration signals to the MPC8533E when HRESET is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of HRESET (PLL configuration inputs must meet a 100 µs set-up time to HRESET), hold their values for at least 2 SYSCLK cycles after the de-assertion of HRESET, and then release the pins to high impedance afterward for normal device operation.

3.2 Configuration Settings

The following table summarizes the customer configurable device settings. Refer to the MPC8533ERM for a more detailed description of each configuration option.

Table 5. User Configuration Options

Configuration Type	Functional Pins	Comments
Device	DMA_DACK[0:1]	Refer to Table 7 for POR and Reset Configurations
CCB Clock PLL Ratio	LA[28:31]	There is no default value for this PLL ratio; these signals must be pulled to the desired value. Refer to Section 5.1, “System PLL Ratio.”
e500 Core PLL Ratio	LBCTL, LALE, LGPL2/LOE/LSDRAS	There is no default value for this PLL ratio; these signals must be pulled to the desired value. Refer to Section 5.2, “e500 Core PLL Ratio.”

Table 5. User Configuration Options (continued)

Configuration Type	Functional Pins	Comments
SEC Frequency Ratio	$\overline{\text{LWE}}$[0]	Default: SEC in 3:1 (CCB CLK:SEC CLK). Refer to Section 5.3, "Security Controller PLL Ratio."
Boot ROM Location	TSEC1_TXD[6:4]	Default: Local Bus GPCM (32-bit ROM)
Host/Agent	$\overline{\text{LWE}}$[1:3]/$\overline{\text{LBS}}$[1:3]	Default: MPC8533E acts as the host processor/root complex on all interfaces.
I/O Port Selection	TSEC3_TXD[6:4]	Default: All three PCI Express ports active
CPU Boot	LA27	Default: e500 core is allowed to boot without waiting for configuration by an external master.
Boot Sequencer	LGPL3/$\overline{\text{LSDCAS}}$, LGPL5	Default: Boot sequencer is disabled. No I^2C ROM is accessed.
DDR SDRAM Type	LGPL[0:1]	Default: DDR controller is configured for DDR2.
eTSEC1 Serial	TSEC1_TXD[2]	Default: eTSEC1 Ethernet interface uses parallel interface according to POR config inputs of eTSEC1 width and eTSEC1 protocol.
eTSEC3 Serial	TSEC3_TXD[2]	Default: eTSEC3 Ethernet interface uses parallel interface according to POR config inputs of eTSEC3 width and eTSEC3 protocol.
eTSEC1 Width	TSEC1_TX_ER	Default: eTSEC1 interface operates in standard width TBI, GMII, MII, or 8-bit FIFO mode.
eTSEC3 Width	TSEC3_TX_ER	Default: eTSEC3 Ethernet interface operates in standard TBI, GMII, MII, or 8-bit FIFO mode.
eTSEC1 Protocol	TSEC1_TXD[0:1]	Default: The eTSEC1 controller operates using the TBI protocol (or RTBI if configured in reduced mode).
eTSEC3 Protocol	TSEC3_TXD[0:1]	Default: The eTSEC3 controller operates using the TBI protocol (or RTBI if configured in reduced mode).
PCI Clock Select	$\overline{\text{PCI1\_GNT}}$[4]	Default: Synchronous mode. SYSCLK is used as the clock for the PCI interface.
PCI Speed	$\overline{\text{PCI1\_GNT}}$[3]	Default: PCI frequency above 33 MHz.
PCI I/O Impedance	$\overline{\text{PCI1\_GNT}}$[1]	Default: 42 Ω I/O drivers are used on the PCI interface.
PCI Arbiter	$\overline{\text{PCI1\_GNT}}$[2]	Default: The on-chip PCI arbiter is enabled.
Memory Debug	MSRCID[0]	Default: Debug information from the DDR SDRAM controller is driven on the MSRCID and MDVAL signals.
DDR Debug	MSRCID[1]	Default: Debug information is not driven on ECC pins. ECC pins function in their normal mode.
General Purpose POR	LAD[0:31]	There is no default value for this general purpose POR.

3.3 Internal Test Modes

Several pins double as test mode enables. These test modes are for internal use only, and if enabled during reset may result in the MPC8533E not coming out of reset. Table 6 lists these pins and how they should be addressed during the reset sequence.

Table 6. Internal Test Mode Pins

Pin Group	Pins	Guideline for Reset
DDR	TEST_IN	Connect directly to ground
	TEST_OUT	This pin may be left floating.
Debug	TRIG_OUT/READY/ $\overline{\text{QUIESCE}}$	Because these pins have an internal pull-up enabled only at reset, they may be left floating if unconnected. Otherwise, they may need to be driven high (that is, by a PLD) if the device to which they are connected does not release to high impedance during reset.
	MSRCID[2]	
	MSRCID[3]	
	MSRCID[4	

Table 6. Internal Test Mode Pins (continued)

Pin Group	Pins	Guideline for Reset
Design For Test	LSSD_MODE	These pins must be pulled to OV_{DD} via a 100 Ω–1 kΩ resistor.
	L1_TSTCLK	
	L2_TSTCLK	
	TEST_SEL	
eTSEC	EC_MDC	Since these pins have an internal pull-up enabled only at reset, they may be left floating if unconnected. Otherwise, they may need to be driven high (that is, by a PLD) if the device to which they are connected does not release to high impedance during reset.
	TSEC1_TXD[7]	
	TSEC1_TXD[3]	
	TSEC3_TXD[7]	
Power Management	ASLEEP	
System Control	HRESET_REQ	

3.4 Reset Checklist

Table 7 provides a summary MPC8533E POR and reset checklist for the designer.

Table 7. Checklist for POR and Reset Configurations

Item	Description	Completed
1	HRESET is asserted for a minimum of 100 μs.	
2	SRESET is asserted for a minimum of 3 SYSCLKs.	
3	DMA_DACK[0:1]—For proper state of these signals during reset, these pins can be left without any pulldowns, thus relying on the internal pullup to get the values to the require 2'b11.However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed.	
4	Configuration pins are either appropriately tied-off with a 4.7 kΩ resistor, or driven by an external device (meeting their required setup and hold times).	
5	PLL configurations are defined and meet the required set-up and hold times.	
6	Internal test mode pins are guaranteed not to be low during reset.	

4 Device Pins

This section discusses the recommended test points and provides a device pin map.

4.1 Recommended Test Points

For easier debug, it is recommended that the test points on the board include the following pins:

- CLK_OUT (This helps to verify the CCB clock.)
- TRIG_OUT (This helps to verify the end of the reset sequence.)
- ASLEEP (This helps to verify the end of the reset sequence.)

- SENSEVDD (This helps to verify power plane VDD.)
- SENSEVSS (This helps to verify ground plane VSS.)
- HRESET_REQ (This helps to verify proper boot sequencer functions and reset requests.)

4.2 Pin Map

Figure 4 provides a top view of the device's pin map. Figure 5–Figure 8 provide detailed quadrant views.

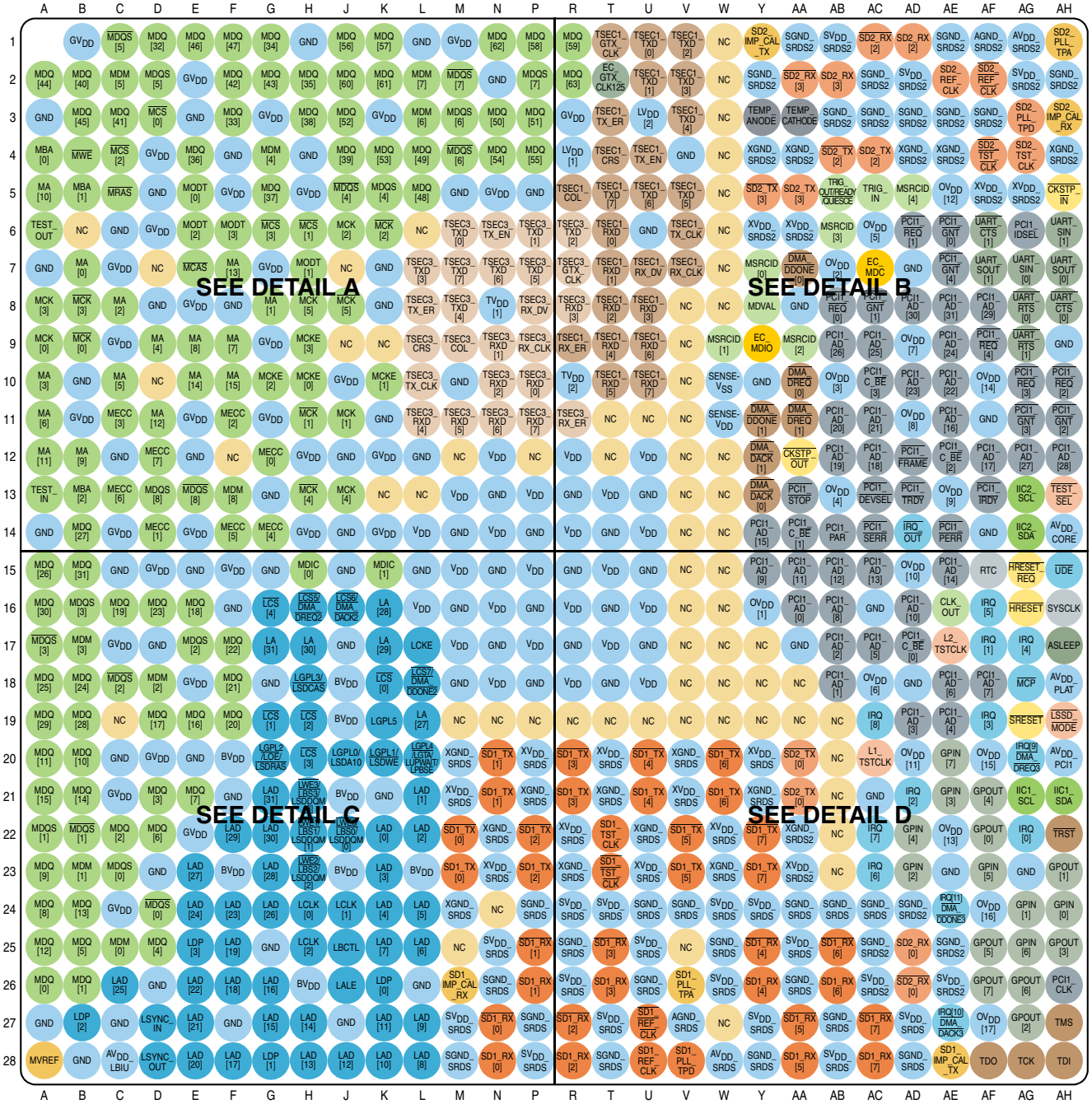


Figure 4. MPC8533E Pin Map Top View

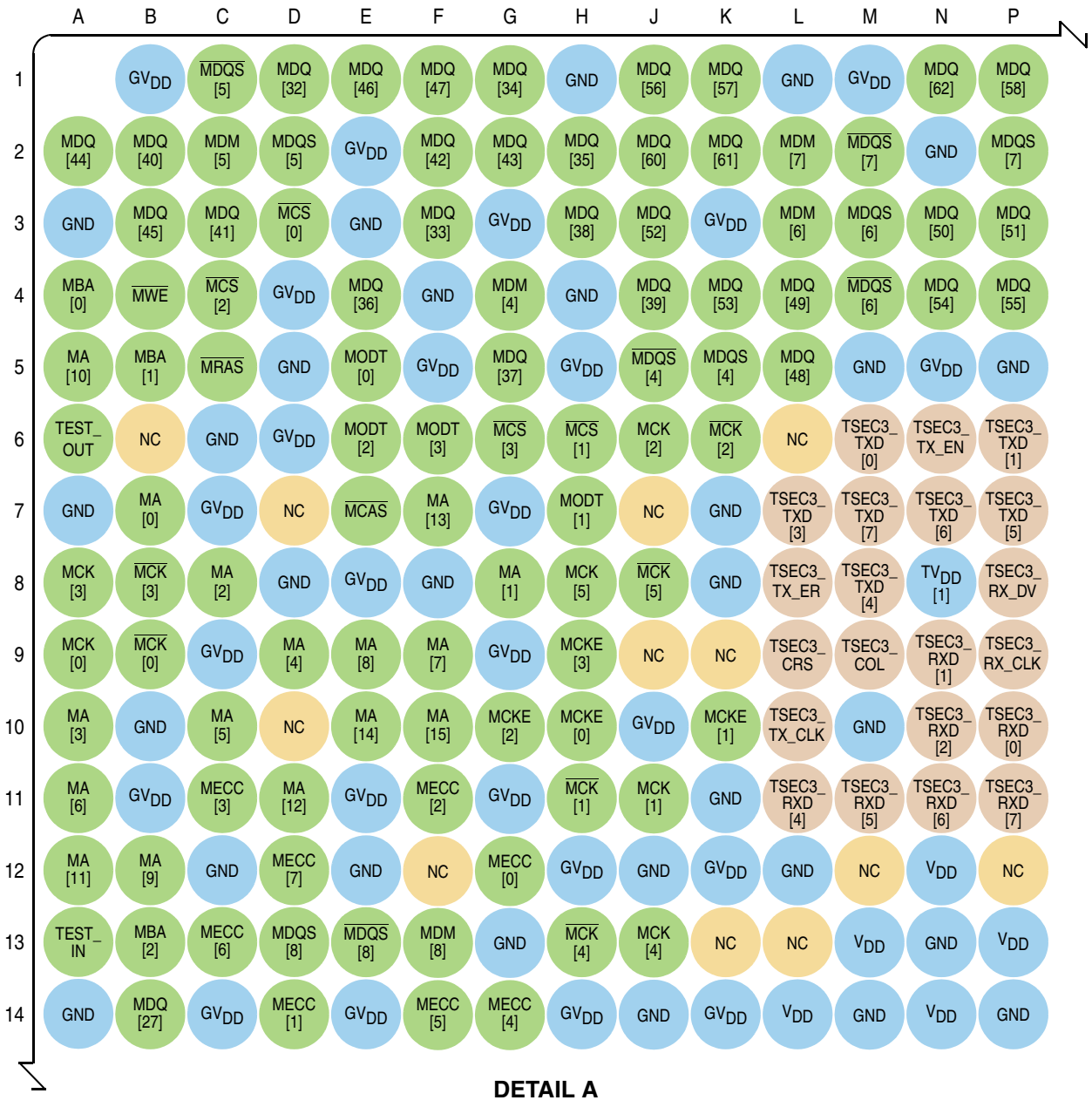
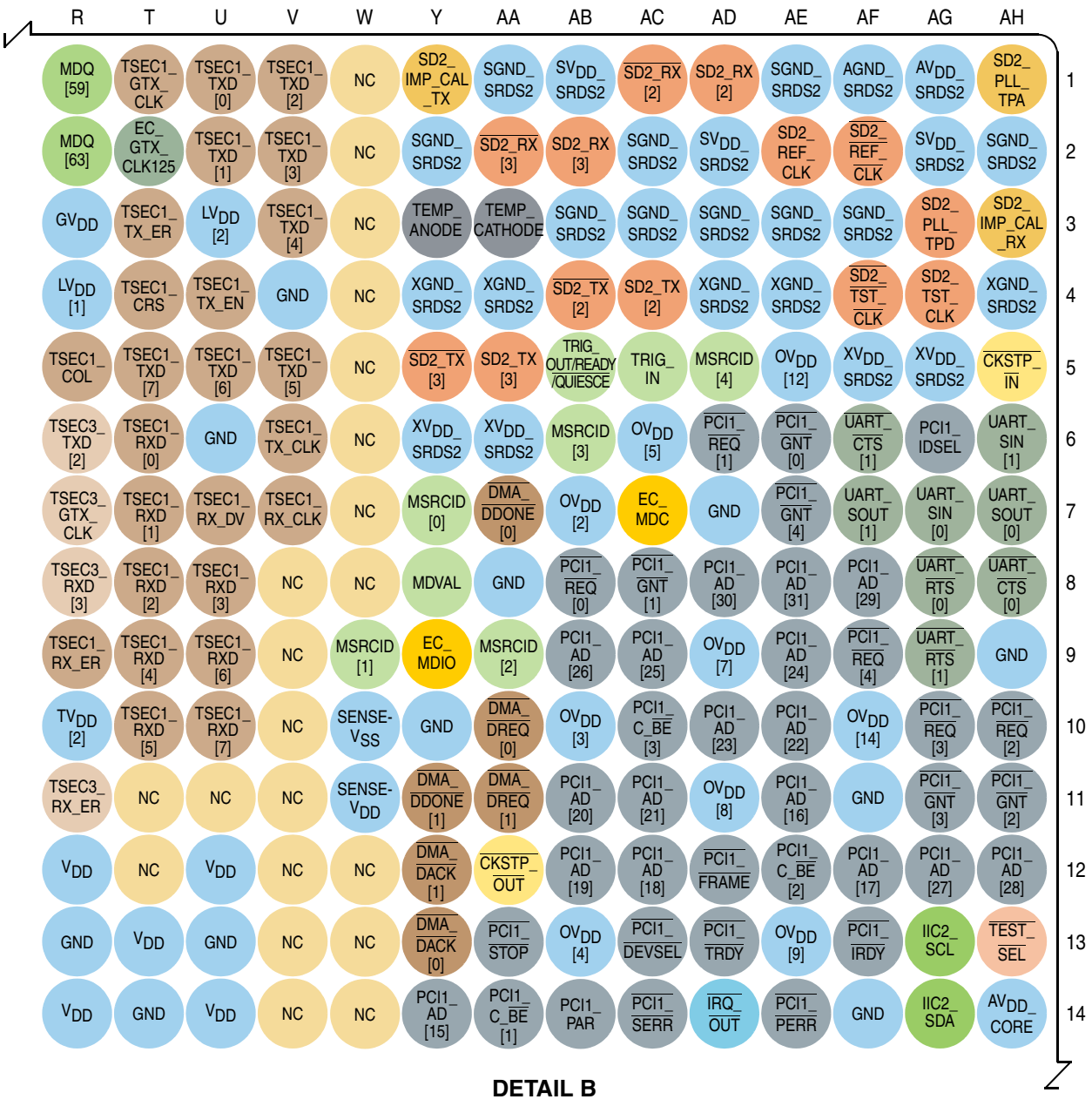


Figure 5. MPC8533E Pin Map Detail A



DETAIL B

Figure 6. MPC8533E Pin Map Detail B

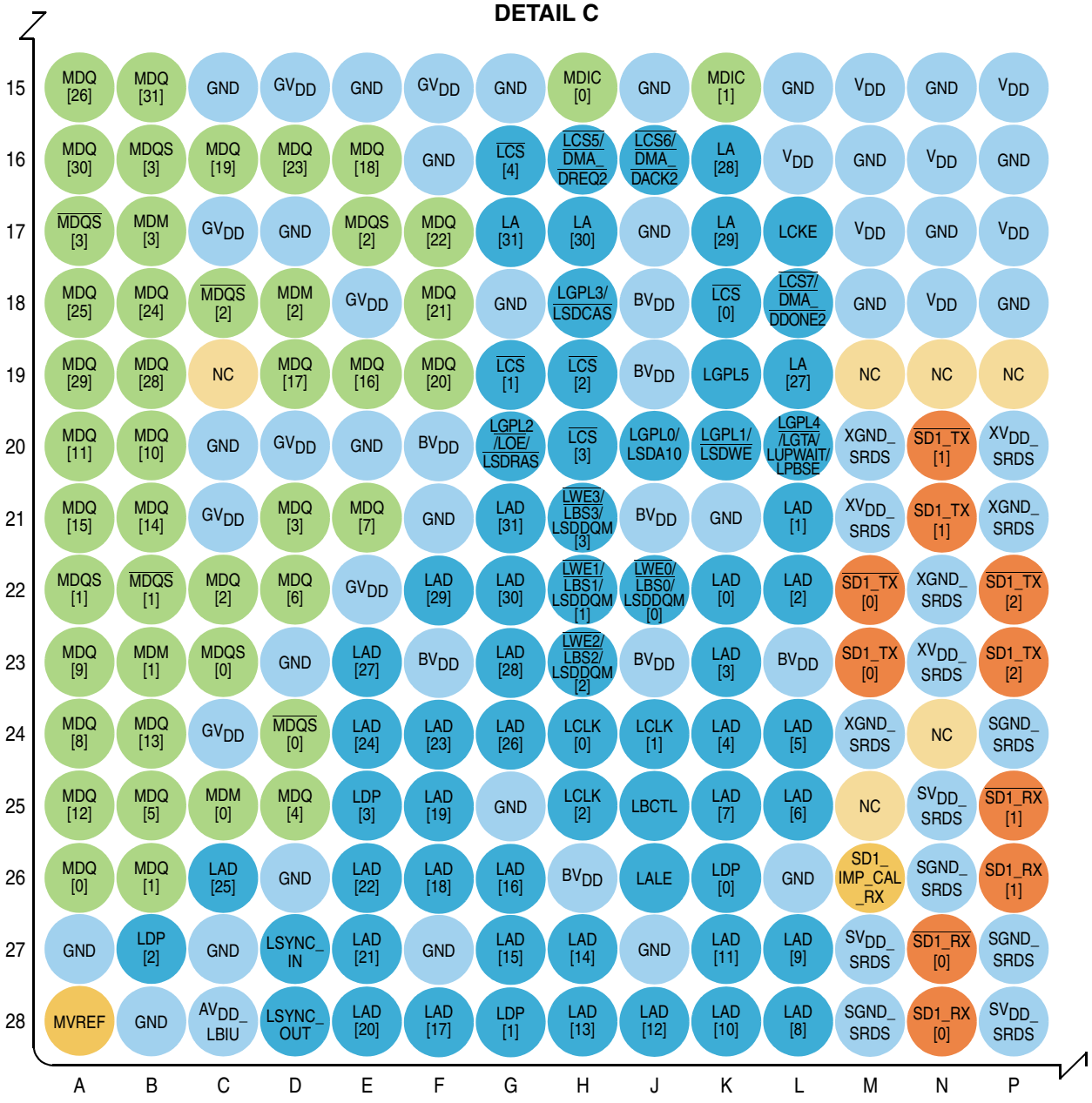


Figure 7. MPC8533E Pin Map Detail C

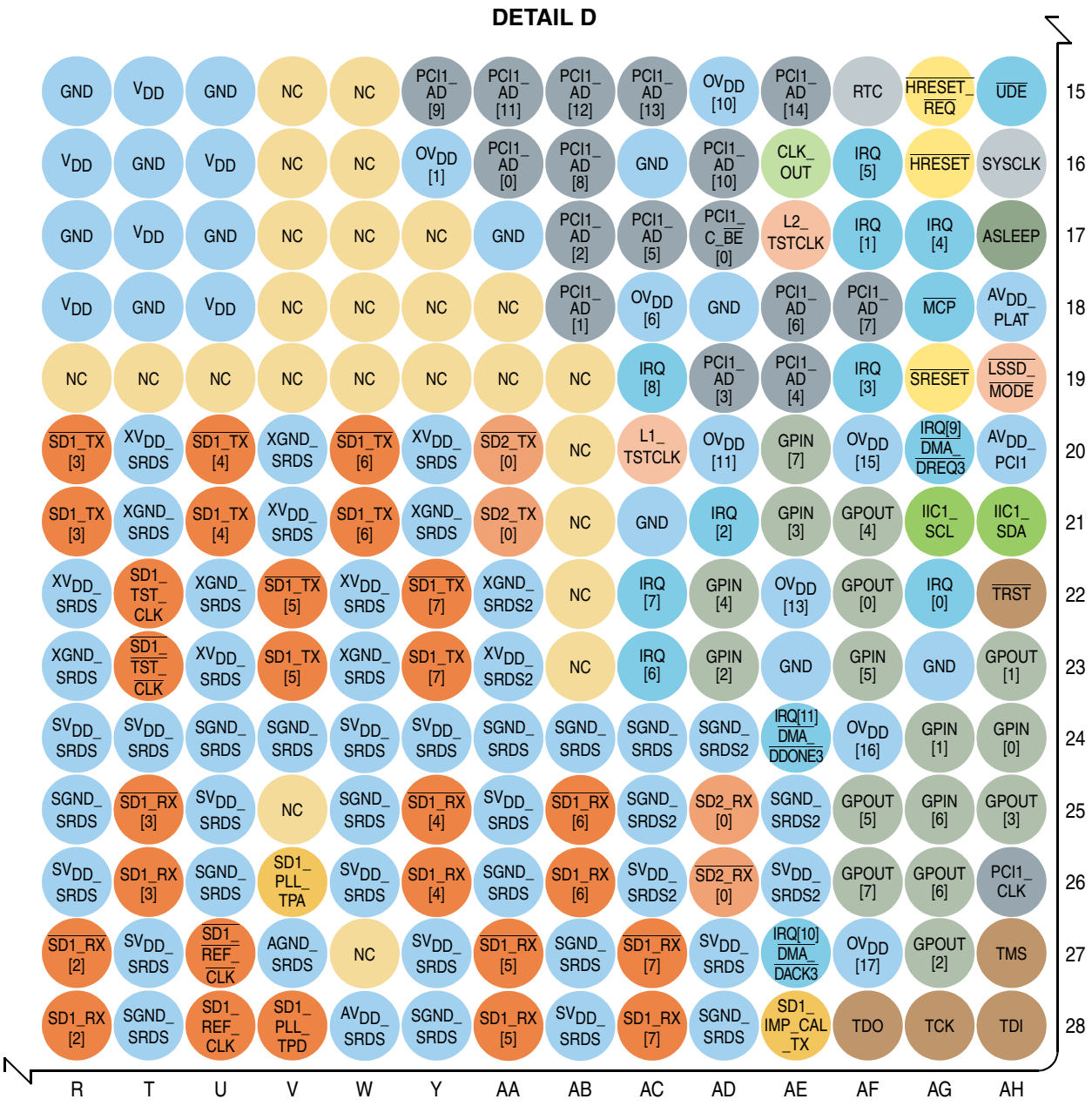


Figure 8. MPC8533E Pin Map Detail D

Figure 9 provides a ball map.

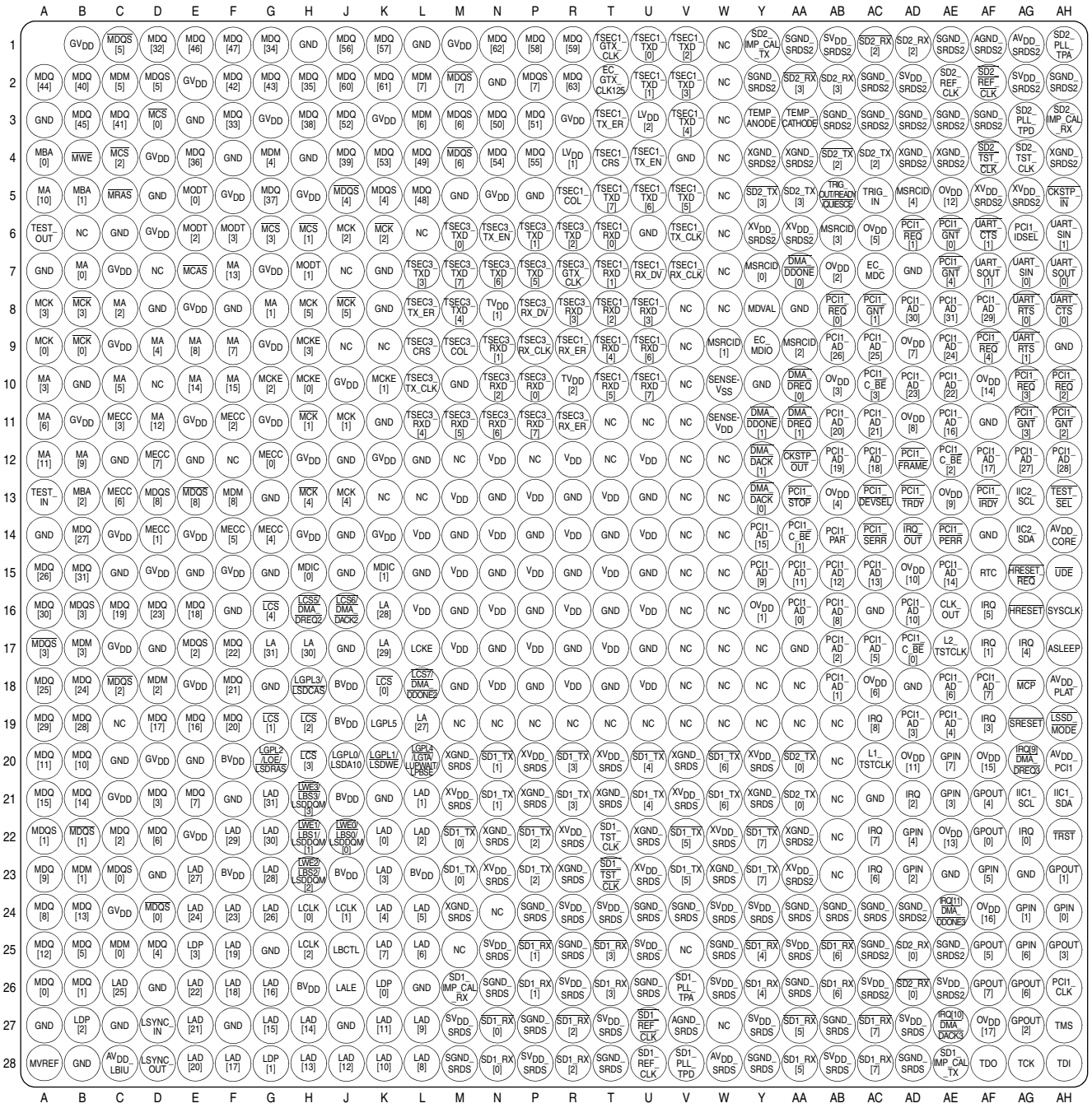


Figure 9. MPC8533E Ball Map

4.3 Pin Listings

Table 8 provides a pin list organized by bus. A downloadable version of the pin list is available in the file AN3641SW.zip on Freescale.com.

Table 8. Pin List—By Bus

Signal	Pin
PCI	
PCI1_AD[31]	AE8
PCI1_AD[30]	AD8
PCI1_AD[29]	AF8
PCI1_AD[28]	AH12
PCI1_AD[27]	AG12
PCI1_AD[26]	AB9
PCI1_AD[25]	AC9
PCI1_AD[24]	AE9
PCI1_AD[23]	AD10
PCI1_AD[22]	AE10
PCI1_AD[21]	AC11
PCI1_AD[20]	AB11
PCI1_AD[19]	AB12
PCI1_AD[18]	AC12
PCI1_AD[17]	AF12
PCI1_AD[16]	AE11
PCI1_AD[15]	Y14
PCI1_AD[14]	AE15
PCI1_AD[13]	AC15
PCI1_AD[12]	AB15
PCI1_AD[11]	AA15
PCI1_AD[10]	AD16
PCI1_AD[9]	Y15
PCI1_AD[8]	AB16
PCI1_AD[7]	AF18
PCI1_AD[6]	AE18
PCI1_AD[5]	AC17
PCI1_AD[4]	AE19
PCI1_AD[3]	AD19

Table 8. Pin List—By Bus (continued)

Signal	Pin
PCI1_AD[2]	AB17
PCI1_AD[1]	AB18
PCI1_AD[0]	AA16
$\overline{\text{PCI1\_C\_BE}}$[3]	AC10
$\overline{\text{PCI1\_C\_BE}}$[2]	AE12
$\overline{\text{PCI1\_C\_BE}}$[1]	AA14
$\overline{\text{PCI1\_C\_BE}}$[0]	AD17
$\overline{\text{PCI1\_GNT}}$[4]	AE7
$\overline{\text{PCI1\_GNT}}$[3]	AG11
$\overline{\text{PCI1\_GNT}}$[2]	AH11
$\overline{\text{PCI1\_GNT}}$[1]	AC8
$\overline{\text{PCI1\_GNT}}$[0]	AE6
$\overline{\text{PCI1\_IRDY}}$	AF13
PCI1_PAR	AB14
$\overline{\text{PCI1\_PERR}}$	AE14
$\overline{\text{PCI1\_SERR}}$	AC14
$\overline{\text{PCI1\_STOP}}$	AA13
$\overline{\text{PCI1\_TRDY}}$	AD13
$\overline{\text{PCI1\_REQ}}$[4]	AF9
$\overline{\text{PCI1\_REQ}}$[3]	AG10
$\overline{\text{PCI1\_REQ}}$[2]	AH10
$\overline{\text{PCI1\_REQ}}$[1]	AD6
$\overline{\text{PCI1\_REQ}}$[0]	AB8
PCI1_CLK	AH26
$\overline{\text{PCI1\_DEVSEL}}$	AC13
$\overline{\text{PCI1\_FRAME}}$	AD12
PCI1_IDSEL	AG6
DDR SDRAM Memory Interface	
MDQ[0]	A26
MDQ[1]	B26
MDQ[2]	C22
MDQ[3]	D21
MDQ[4]	D25

Table 8. Pin List—By Bus (continued)

Signal	Pin
MDQ[5]	B25
MDQ[6]	D22
MDQ[7]	E21
MDQ[8]	A24
MDQ[9]	A23
MDQ[10]	B20
MDQ[11]	A20
MDQ[12]	A25
MDQ[13]	B24
MDQ[14]	B21
MDQ[15]	A21
MDQ[16]	E19
MDQ[17]	D19
MDQ[18]	E16
MDQ[19]	C16
MDQ[20]	F19
MDQ[21]	F18
MDQ[22]	F17
MDQ[23]	D16
MDQ[24]	B18
MDQ[25]	A18
MDQ[26]	A15
MDQ[27]	B14
MDQ[28]	B19
MDQ[29]	A19
MDQ[30]	A16
MDQ[31]	B15
MDQ[32]	D1
MDQ[33]	F3
MDQ[34]	G1
MDQ[35]	H2
MDQ[36]	E4
MDQ[37]	G5

Table 8. Pin List—By Bus (continued)

Signal	Pin
MDQ[38]	H3
MDQ[39]	J4
MDQ[40]	B2
MDQ[41]	C3
MDQ[42]	F2
MDQ[43]	G2
MDQ[44]	A2
MDQ[45]	B3
MDQ[46]	E1
MDQ[47]	F1
MDQ[48]	L5
MDQ[49]	L4
MDQ[50]	N3
MDQ[51]	P3
MDQ[52]	J3
MDQ[53]	K4
MDQ[54]	N4
MDQ[55]	P4
MDQ[56]	J1
MDQ[57]	K1
MDQ[58]	P1
MDQ[59]	R1
MDQ[60]	J2
MDQ[61]	K2
MDQ[62]	N1
MDQ[63]	R2
MECC[0]	G12
MECC[1]	D14
MECC[2]	F11
MECC[3]	C11
MECC[4]	G14
MECC[5]	F14
MECC[6]	C13

Table 8. Pin List—By Bus (continued)

Signal	Pin
MECC[7]	D12
MDM[0]	C25
MDM[1]	B23
MDM[2]	D18
MDM[3]	B17
MDM[4]	G4
MDM[5]	C2
MDM[6]	L3
MDM[7]	L2
MDM[8]	F13
$\overline{\text{MDQS}}$[0]	D24
$\overline{\text{MDQS}}$[1]	B22
$\overline{\text{MDQS}}$[2]	C18
$\overline{\text{MDQS}}$[3]	A17
$\overline{\text{MDQS}}$[4]	J5
$\overline{\text{MDQS}}$[5]	C1
$\overline{\text{MDQS}}$[6]	M4
$\overline{\text{MDQS}}$[7]	M2
$\overline{\text{MDQS}}$[8]	E13
MDQS[0]	C23
MDQS[1]	A22
MDQS[2]	E17
MDQS[3]	B16
MDQS[4]	K5
MDQS[5]	D2
MDQS[6]	M3
MDQS[7]	P2
MDQS[8]	D13
MA[0]	B7
MA[1]	G8
MA[2]	C8
MA[3]	A10
MA[4]	D9

Table 8. Pin List—By Bus (continued)

Signal	Pin
MA[5]	C10
MA[6]	A11
MA[7]	F9
MA[8]	E9
MA[9]	B12
MA[10]	A5
MA[11]	A12
MA[12]	D11
MA[13]	F7
MA[14]	E10
MA[15]	F10
MBA[0]	A4
MBA[1]	B5
MBA[2]	B13
$\overline{\text{MWE}}$	B4
$\overline{\text{MCAS}}$	E7
$\overline{\text{MRAS}}$	C5
MCKE[0]	H10
MCKE[1]	K10
MCKE[2]	G10
MCKE[3]	H9
$\overline{\text{MCS}}$[0]	D3
$\overline{\text{MCS}}$[1]	H6
$\overline{\text{MCS}}$[2]	C4
$\overline{\text{MCS}}$[3]	G6
MCK[0]	A9
MCK[1]	J11
MCK[2]	J6
MCK[3]	A8
MCK[4]	J13
MCK[5]	H8
$\overline{\text{MCK}}$[0]	B9
$\overline{\text{MCK}}$[1]	H11

Table 8. Pin List—By Bus (continued)

Signal	Pin
$\overline{\text{MCK}}$[2]	K6
$\overline{\text{MCK}}$[3]	B8
$\overline{\text{MCK}}$[4]	H13
$\overline{\text{MCK}}$[5]	J8
MODT[0]	E5
MODT[1]	H7
MODT[2]	E6
MODT[3]	F6
MDIC[0]	H15
MDIC[1]	K15
TEST_IN	A13
TEST_OUT	A6
Local Bus Controller Interface	
LAD[0]	K22
LAD[1]	L21
LAD[2]	L22
LAD[3]	K23
LAD[4]	K24
LAD[5]	L24
LAD[6]	L25
LAD[7]	K25
LAD[8]	L28
LAD[9]	L27
LAD[10]	K28
LAD[11]	K27
LAD[12]	J28
LAD[13]	H28
LAD[14]	H27
LAD[15]	G27
LAD[16]	G26
LAD[17]	F28
LAD[18]	F26
LAD[19]	F25

Table 8. Pin List—By Bus (continued)

Signal	Pin
LAD[20]	E28
LAD[21]	E27
LAD[22]	E26
LAD[23]	F24
LAD[24]	E24
LAD[25]	C26
LAD[26]	G24
LAD[27]	E23
LAD[28]	G23
LAD[29]	F22
LAD[30]	G22
LAD[31]	G21
LDP[0]	K26
LDP[1]	G28
LDP[2]	B27
LDP[3]	E25
LA[27]	L19
LA[28]	K16
LA[29]	K17
LA[30]	H17
LA[31]	G17
$\overline{\text{LCS}}$[0]	K18
$\overline{\text{LCS}}$[1]	G19
$\overline{\text{LCS}}$[2]	H19
$\overline{\text{LCS}}$[3]	H20
$\overline{\text{LCS}}$[4]	G16
$\overline{\text{LCS5}}$/DMA_DREQ2	H16
$\overline{\text{LCS6}}$/DMA_DACK2	J16
$\overline{\text{LCS7}}$/DMA_DDONE2	L18
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/LSDDQM[0]	J22
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$/LSDDQM[1]	H22
$\overline{\text{LWE2}}$/$\overline{\text{LBS2}}$/LSDDQM[2]	H23
$\overline{\text{LWE3}}$/$\overline{\text{LBS3}}$/LSDDQM[3]	H21

Table 8. Pin List—By Bus (continued)

Signal	Pin
LALE	J26
LBCTL	J25
LGPL0/LSDA10	J20
LGPL1/$\overline{\text{LSDWE}}$	K20
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$	G20
LGPL3/$\overline{\text{LSDCAS}}$	H18
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	L20
LGPL5	K19
LCKE	L17
LCLK[0]	H24
LCLK[1]	J24
LCLK[2]	H25
LSYNC_IN	D27
LSYNC_OUT	D28
DMA	
$\overline{\text{DMA\_DACK}}$[0]	Y13
$\overline{\text{DMA\_DACK}}$[1]	Y12
$\overline{\text{DMA\_DREQ}}$[0]	AA10
$\overline{\text{DMA\_DREQ}}$[1]	AA11
$\overline{\text{DMA\_DDONE}}$[0]	AA7
$\overline{\text{DMA\_DDONE}}$[1]	Y11
Programmable Interrupt Controller	
$\overline{\text{UDE}}$	AH15
$\overline{\text{MCP}}$	AG18
IRQ[0]	AG22
IRQ[1]	AF17
IRQ[2]	AD21
IRQ[3]	AF19
IRQ[4]	AG17
IRQ[5]	AF16
IRQ[6]	AC23
IRQ[7]	AC22
IRQ[8]	AC19

Table 8. Pin List—By Bus (continued)

Signal	Pin
IRQ[9]/DMA_DREQ3	AG20
IRQ[10]/DMA_DACK3	AE27
IRQ[11]/DMA_DDONE3	AE24
IRQ_OUT	AD14
Ethernet Management Gigabit Reference Clock	
EC_MDC	AC7
EC_MDIO	Y9
EC_GTX_CLK125	T2
Three-Speed Ethernet Controller (Gigabit Ethernet 1)	
TSEC1_RXD[7]	U10
TSEC1_RXD[6]	U9
TSEC1_RXD[5]	T10
TSEC1_RXD[4]	T9
TSEC1_RXD[3]	U8
TSEC1_RXD[2]	T8
TSEC1_RXD[1]	T7
TSEC1_RXD[0]	T6
TSEC1_TXD[7]	T5
TSEC1_TXD[6]	U5
TSEC1_TXD[5]	V5
TSEC1_TXD[4]	V3
TSEC1_TXD[3]	V2
TSEC1_TXD[2]	V1
TSEC1_TXD[1]	U2
TSEC1_TXD[0]	U1
TSEC1_COL	R5
TSEC1_CRS	T4
TSEC1_GTX_CLK	T1
TSEC1_RX_CLK	V7
TSEC1_RX_DV	U7
TSEC1_RX_ER	R9
TSEC1_TX_CLK	V6
TSEC1_TX_EN	U4

Table 8. Pin List—By Bus (continued)

Signal	Pin
TSEC1_TX_ER	T3
Three-Speed Ethernet Controller (Gigabit Ethernet 3)	
TSEC3_RXD[7]	P11
TSEC3_RXD[6]	N11
TSEC3_RXD[5]	M11
TSEC3_RXD[4]	L11
TSEC3_RXD[3]	R8
TSEC3_RXD[2]	N10
TSEC3_RXD[1]	N9
TSEC3_RXD[0]	P10
TSEC3_TXD[7]	M7
TSEC3_TXD[6]	N7
TSEC3_TXD[5]	P7
TSEC3_TXD[4]	M8
TSEC3_TXD[3]	L7
TSEC3_TXD[2]	R6
TSEC3_TXD[1]	P6
TSEC3_TXD[0]	M6
TSEC3_COL	M9
TSEC3_CRS	L9
TSEC3_GTX_CLK	R7
TSEC3_RX_CLK	P9
TSEC3_RX_DV	P8
TSEC3_RX_ER	R11
TSEC3_TX_CLK	L10
TSEC3_TX_EN	N6
TSEC3_TX_ER	L8
DUART	
$\overline{\text{UART\_CTS}}$[0]	AH8
$\overline{\text{UART\_CTS}}$[1]	AF6
$\overline{\text{UART\_RTS}}$[0]	AG8
$\overline{\text{UART\_RTS}}$[1]	AG9
UART_SIN[0]	AG7

Table 8. Pin List—By Bus (continued)

Signal	Pin
UART_SIN[1]	AH6
UART_SOUT[0]	AH7
UART_SOUT[1]	AF7
I^2C Interface	
IIC1_SCL	AG21
IIC1_SDA	AH21
IIC2_SCL	AG13
IIC2_SDA	AG14
SerDes1	
SD1_RX[0]	N28
SD1_RX[1]	P26
SD1_RX[2]	R28
SD1_RX[3]	T26
SD1_RX[4]	Y26
SD1_RX[5]	AA28
SD1_RX[6]	AB26
SD1_RX[7]	AC28
$\overline{\text{SD1\_RX}}$[0]	N27
$\overline{\text{SD1\_RX}}$[1]	P25
$\overline{\text{SD1\_RX}}$[2]	R27
$\overline{\text{SD1\_RX}}$[3]	T25
$\overline{\text{SD1\_RX}}$[4]	Y25
$\overline{\text{SD1\_RX}}$[5]	AA27
$\overline{\text{SD1\_RX}}$[6]	AB25
$\overline{\text{SD1\_RX}}$[7]	AC27
SD1_TX[0]	M23
SD1_TX[1]	N21
SD1_TX[2]	P23
SD1_TX[3]	R21
SD1_TX[4]	U21
SD1_TX[5]	V23
SD1_TX[6]	W21
SD1_TX[7]	Y23

Table 8. Pin List—By Bus (continued)

Signal	Pin
$\overline{\text{SD1\_TX}}$[0]	M22
$\overline{\text{SD1\_TX}}$[1]	N20
$\overline{\text{SD1\_TX}}$[2]	P22
$\overline{\text{SD1\_TX}}$[3]	R20
$\overline{\text{SD1\_TX}}$[4]	U20
$\overline{\text{SD1\_TX}}$[5]	V22
$\overline{\text{SD1\_TX}}$[6]	W20
$\overline{\text{SD1\_TX}}$[7]	Y22
SD1_PLL_TPD	V28
SD1_REF_CLK	U28
$\overline{\text{SD1\_REF\_CLK}}$	U27
SD1_TST_CLK	T22
$\overline{\text{SD1\_TST\_CLK}}$	T23
SerDes2	
SD2_RX[0]	AD26
SD2_RX[2]	AD1
SD2_RX[3]	AB2
$\overline{\text{SD2\_RX}}$[0]	AD25
$\overline{\text{SD2\_RX}}$[2]	AC1
$\overline{\text{SD2\_RX}}$[3]	AA2
SD2_TX[0]	AA21
SD2_TX[2]	AC4
SD2_TX[3]	AA5
$\overline{\text{SD2\_TX}}$[0]	AA20
$\overline{\text{SD2\_TX}}$[2]	AB4
$\overline{\text{SD2\_TX}}$[3]	Y5
SD2_PLL_TPD	AG3
SD2_REF_CLK	AE2
$\overline{\text{SD2\_REF\_CLK}}$	AF2
SD2_TST_CLK	AG4
$\overline{\text{SD2\_TST\_CLK}}$	AF4
General-Purpose Output	
GPOUT[0]	AF22

Table 8. Pin List—By Bus (continued)

Signal	Pin
GPOUT[1]	AH23
GPOUT[2]	AG27
GPOUT[3]	AH25
GPOUT[4]	AF21
GPOUT[5]	AF25
GPOUT[6]	AG26
GPOUT[7]	AF26
General-Purpose Input	
GPIN[0]	AH24
GPIN[1]	AG24
GPIN[2]	AD23
GPIN[3]	AE21
GPIN[4]	AD22
GPIN[5]	AF23
GPIN[6]	AG25
GPIN[7]	AE20
System Control	
$\overline{\text{HRESET}}$	AG16
$\overline{\text{HRESET\_REQ}}$	AG15
$\overline{\text{SRESET}}$	AG19
$\overline{\text{CKSTP\_IN}}$	AH5
$\overline{\text{CKSTP\_OUT}}$	AA12
Debug	
TRIG_IN	AC5
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	AB5
MSRCID[0]	Y7
MSRCID[1]	W9
MSRCID[2]	AA9
MSRCID[3]	AB6
MSRCID[4]	AD5
MDVAL	Y8
CLK_OUT	AE16
Clock	

Table 8. Pin List—By Bus (continued)

Signal	Pin
RTC	AF15
SYSCLK	AH16
JTAG	
TCK	AG28
TDI	AH28
TDO	AF28
TMS	AH27
$\overline{\text{TRST}}$	AH22
DFT	
L1_TSTCLK	AC20
L2_TSTCLK	AE17
$\overline{\text{LSSD\_MODE}}$	AH19
$\overline{\text{TEST\_SEL}}$	AH13
Thermal Management	
TEMP_ANODE	Y3
TEMP_CATHODE	AA3
Power Management	
ASLEEP	AH17
Power and Ground Signals	
GND	D5
GND	M10
GND	F4
GND	D26
GND	D23
GND	C12
GND	C15
GND	E20
GND	D8
GND	B10
GND	E3
GND	J14
GND	K21
GND	F8

Table 8. Pin List—By Bus (continued)

Signal	Pin
GND	A3
GND	F16
GND	E12
GND	E15
GND	D17
GND	L1
GND	F21
GND	H1
GND	G13
GND	G15
GND	G18
GND	C6
GND	A14
GND	A7
GND	G25
GND	H4
GND	C20
GND	J12
GND	J15
GND	J17
GND	F27
GND	M5
GND	J27
GND	K11
GND	L26
GND	K7
GND	K8
GND	L12
GND	L15
GND	M14
GND	M16
GND	M18
GND	N13

Table 8. Pin List—By Bus (continued)

Signal	Pin
GND	N15
GND	N17
GND	N2
GND	P5
GND	P14
GND	P16
GND	P18
GND	R13
GND	R15
GND	R17
GND	T14
GND	T16
GND	T18
GND	U13
GND	U15
GND	U17
GND	AA8
GND	U6
GND	Y10
GND	AC21
GND	AA17
GND	AC16
GND	V4
GND	AD7
GND	AD18
GND	AE23
GND	AF11
GND	AF14
GND	AG23
GND	AH9
GND	A27
GND	B28
GND	C27

Table 8. Pin List—By Bus (continued)

Signal	Pin
OVDD	Y16
OVDD	AB7
OVDD	AB10
OVDD	AB13
OVDD	AC6
OVDD	AC18
OVDD	AD9
OVDD	AD11
OVDD	AE13
OVDD	AD15
OVDD	AD20
OVDD	AE5
OVDD	AE22
OVDD	AF10
OVDD	AF20
OVDD	AF24
OVDD	AF27
LVDD	R4
LVDD	U3
TVDD	N8
TVDD	R10
GVDD	B1
GVDD	B11
GVDD	C7
GVDD	C9
GVDD	C14
GVDD	C17
GVDD	D4
GVDD	D6
GVDD	R3
GVDD	D15
GVDD	E2
GVDD	E8

Table 8. Pin List—By Bus (continued)

Signal	Pin
GVDD	C24
GVDD	E18
GVDD	F5
GVDD	E14
GVDD	C21
GVDD	G3
GVDD	G7
GVDD	G9
GVDD	G11
GVDD	H5
GVDD	H12
GVDD	E22
GVDD	F15
GVDD	J10
GVDD	K3
GVDD	K12
GVDD	K14
GVDD	H14
GVDD	D20
GVDD	E11
GVDD	M1
GVDD	N5
BVDD	L23
BVDD	J18
BVDD	J19
BVDD	F20
BVDD	F23
BVDD	H26
BVDD	J21
BVDD	J23
VDD	L16
VDD	L14
VDD	M13

Table 8. Pin List—By Bus (continued)

Signal	Pin
VDD	M15
VDD	M17
VDD	N12
VDD	N14
VDD	N16
VDD	N18
VDD	P13
VDD	P15
VDD	P17
VDD	R12
VDD	R14
VDD	R16
VDD	R18
VDD	T13
VDD	T15
VDD	T17
VDD	U12
VDD	U14
VDD	U16
VDD	U18
SVDD_SRDS	M27
SVDD_SRDS	N25
SVDD_SRDS	P28
SVDD_SRDS	R24
SVDD_SRDS	R26
SVDD_SRDS	T24
SVDD_SRDS	T27
SVDD_SRDS	U25
SVDD_SRDS	W24
SVDD_SRDS	W26
SVDD_SRDS	Y24
SVDD_SRDS	Y27
SVDD_SRDS	AA25

Table 8. Pin List—By Bus (continued)

Signal	Pin
SVDD_SRDS	AB28
SVDD_SRDS	AD27
SVDD_SRDS2	AB1
SVDD_SRDS2	AC26
SVDD_SRDS2	AD2
SVDD_SRDS2	AE26
SVDD_SRDS2	AG2
XVDD_SRDS	M21
XVDD_SRDS	N23
XVDD_SRDS	P20
XVDD_SRDS	R22
XVDD_SRDS	T20
XVDD_SRDS	U23
XVDD_SRDS	V21
XVDD_SRDS	W22
XVDD_SRDS	Y20
XVDD_SRDS2	Y6
XVDD_SRDS2	AA6
XVDD_SRDS2	AA23
XVDD_SRDS2	AF5
XVDD_SRDS2	AG5
XGND_SRDS	M20
XGND_SRDS	M24
XGND_SRDS	N22
XGND_SRDS	P21
XGND_SRDS	R23
XGND_SRDS	T21
XGND_SRDS	U22
XGND_SRDS	V20
XGND_SRDS	W23
XGND_SRDS	Y21
XGND_SRDS2	Y4
XGND_SRDS2	AA4

Table 8. Pin List—By Bus (continued)

Signal	Pin
XGND_SRDS2	AA22
XGND_SRDS2	AD4
XGND_SRDS2	AE4
XGND_SRDS2	AH4
SGND_SRDS	M28
SGND_SRDS	N26
SGND_SRDS	P24
SGND_SRDS	P27
SGND_SRDS	R25
SGND_SRDS	T28
SGND_SRDS	U24
SGND_SRDS	U26
SGND_SRDS	V24
SGND_SRDS	W25
SGND_SRDS	Y28
SGND_SRDS	AA24
SGND_SRDS	AA26
SGND_SRDS	AB24
SGND_SRDS	AB27
SGND_SRDS	AC24
SGND_SRDS	AD28
AGND_SRDS	V27
SGND_SRDS2	Y2
SGND_SRDS2	AA1
SGND_SRDS2	AB3
SGND_SRDS2	AC2
SGND_SRDS2	AC3
SGND_SRDS2	AC25
SGND_SRDS2	AD3
SGND_SRDS2	AD24
SGND_SRDS2	AE3
SGND_SRDS2	AE1
SGND_SRDS2	AE25

Table 8. Pin List—By Bus (continued)

Signal	Pin
SGND_SRDS2	AF3
SGND_SRDS2	AH2
AGND_SRDS2	AF1
AVDD_LBIU	C28
AVDD_PCI1	AH20
AVDD_CORE	AH14
AVDD_PLAT	AH18
AVDD_SRDS	W28
AVDD_SRDS2	AG1
SENSEVDD	W11
SENSEVSS	W10
Analog Signals	
MVREF	A28
SD1_IMP_CAL_RX	M26
SD1_IMP_CAL_TX	AE28
SD1_PLL_TPA	V26
SD2_IMP_CAL_RX	AH3
SD2_IMP_CAL_TX	Y1
SD2_PLL_TPA	AH1
No Connect Pins	
NC	C19
NC	D7
NC	D10
NC	K13
NC	L6
NC	K9
NC	B6
NC	F12
NC	J7
NC	M19
NC	M25
NC	N19
NC	N24

Table 8. Pin List—By Bus (continued)

Signal	Pin
NC	P19
NC	R19
NC	AB19
NC	T12
NC	W3
NC	M12
NC	W5
NC	P12
NC	T19
NC	W1
NC	W7
NC	L13
NC	U19
NC	W4
NC	V8
NC	V9
NC	V10
NC	V11
NC	V12
NC	V13
NC	V14
NC	V15
NC	V16
NC	V17
NC	V18
NC	V19
NC	W2
NC	W6
NC	W8
NC	T11
NC	U11
NC	W12
NC	W13

Table 8. Pin List—By Bus (continued)

Signal	Pin
NC	W14
NC	W15
NC	W16
NC	W17
NC	W18
NC	W19
NC	W27
NC	V25
NC	Y17
NC	Y18
NC	Y19
NC	AA18
NC	AA19
NC	AB20
NC	AB21
NC	AB22
NC	AB23
NC	J9

5 Clocks

Figure 10 shows the internal distribution of clocks within the MPC8533E.

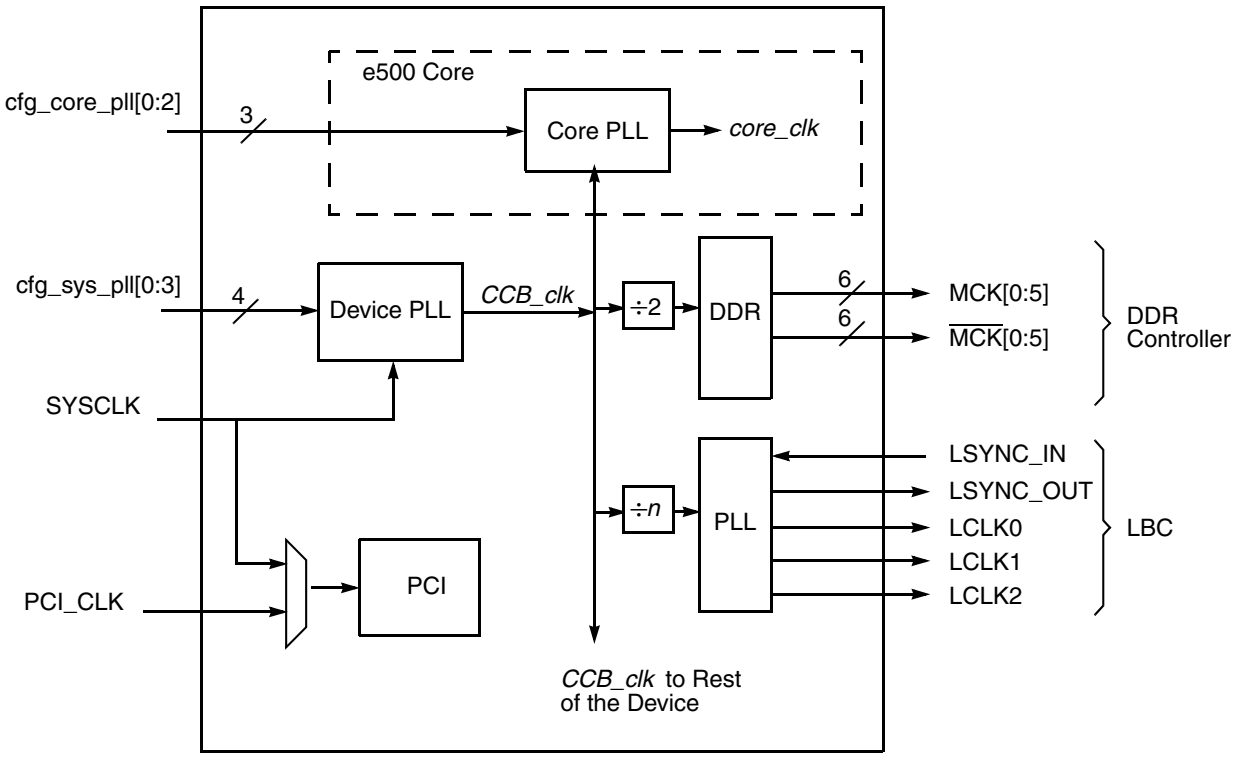


Figure 10. Clock Subsystem Block Diagram

The clock inputs for the MPC8533E are the EC_GTX_CLK125, PCI1_CLK, RTC, SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$, and SYSCLK. The EC_GTX_CLK125 input is used by the eTSEC controller as a reference clock for gigabit Ethernet modes. The PCI1_CLK input are PCI clock input if the PCI controller is configured in asynchronous mode. SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are the reference clocks for PCI-Express operating modes. SYSCLK is the primary clock input to the device.

Table 10 shows how the clock pins should be connected.

Table 10. Clock Pin Recommendations

Pin Name	Pin Used	Pin Not Used
EC_GTX_CLK125	If any of the eTSECs are used in gigabit mode, connect to a 125 MHz clock.	Pull high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively.
PCI1_CLK	If PCI1 is configured for PCI and asychronous mode, connect to a 16–66 MHz clock. If PCI1 is configured for PCI-X and asychronous mode, connect to a 66–133 MHz clock.	Pull high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
RTC	If used, connect to a clock that runs no greater than 1/4 the platform CCB_clk.	Pull high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.

Table 10. Clock Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
SD_REF_CLK/ SD_REF_CLK	If the SerDes is enabled at POR, connect to a clock at the frequency specified per the POR I/O Port Selection.	These pins must be connected to GND.
SYSCLK	This must always be connected to an input clock of 16–133 MHz	

5.1 System PLL Ratio

The system PLL inputs, shown in Table 11, establish the clock ratio between the SYSCLK input and the platform clock used by the MPC8533E.

Table 11. CCB Clock Ratio

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	16:1	1000	8:1
0001	Reserved	1001	9:1
0010	Reserved	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1
0101	5:1	1101	Reserved
0110	6:1	1110	Reserved
0111	Reserved	1111	Reserved

5.2 e500 Core PLL Ratio

Table 12 describes the e500 core clock PLL inputs that program the core PLL and establish the ratio between the e500 core clock and the e500 core complex bus (CCB) clock.

Table 12. e500 Core to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1	100	2:1
001	Reserved	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

5.3 Security Controller PLL Ratio

The SEC mode frequency configuration allows for CCB CLK:SEC_CLK ratio of 2:1 or 3:1. Depending on the SEC PLL ratio of 2:1 or 3:1, the serial bit clock frequency of I^2C (SCL) can be either one-half or one-third of the CCB clock respectively.

Table 13. SEC Frequency Ratio

Pin Name	Value (Binary)	CCB CLK:SEC CLK
$\overline{\text{LWE}}$	0	2:1[1]
	1	3:1[2]

Notes:
1. In 2:1 mode the CCB frequency must be operating ≤ 400 MHz.
2. In 3:1 mode any valid CCB can be used. The 3:1 mode is the default ratio for security block.

6 DDR Interface

This section discusses the termination of DDR pins on the device. Table 14 shows how the DDR pins should be connected.

Table 14. DDR Pin Recommendations

Pin Name	Pin Used	Pin Not Used
MA[0:15]	Auto-precharge for DDR signaled on A10 when DDR_SDRAM_CFG[PCHB8] = 0. Auto-precharge for DDR signaled on A8 when DDR_SDRAM_CFG[PCHB8] = 1.	These pins may be left unconnected.
MBA[0:2]	—	
MCAS	—	
MCK/$\overline{\text{MCK}}$[0:5]	—	
MCKE[0:3]	These pins are actively driven instead of being tri-stated during reset.	
MCS[0:3]	—	
MDIC[0:1]	MDIC0 is grounded through an 18.2-Ω precision 1% resistor and MDIC1 is connected to GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR I/Os.	
MDM[0:8]	—	These pins may be left unconnected.
MDQ[0:63]	—	
MDQS[0:8]/MDQS[0:8]	—	
MECC[0:7]	—	These pins should be pulled high or low via a 2–10 kΩ resistor.

Table 14. DDR Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
MODT[0:3]	—	These pins may be left unconnected.
MRAS	—	
MWE	—	

7 Debug and Test Interface

This section discusses the termination of debug and test pins on the device. Table 15 shows how the Debug and Test pins should be connected.

Table 15. Debug and Test Pin Recommendations

Pin Name	Pin Used	Pin Not Used
ASLEEP	This pin must NOT be pulled down during power-on reset.	This pin may be left unconnected.
CLK_OUT	**Note:** This output is actively driven during reset rather than being three-stated during reset.	This pin may be left unconnected.
MDVAL	—	This pin must be left unconnected.
L1_TSTCLK	These signals must be pulled up via a 100–1000 Ω resistor to OV_{DD} for normal machine operation.	
L2_TSTCLK		
LSSD_MODE		
MSRCID[0:1]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	This pin must be left unconnected.
MSRCID[2:4]	These pins must NOT be pulled down during power-on reset.	This pin must be left unconnected.
SD1_IMP_CAL_RX	This pin must be pulled down through a 200 Ω resistor.	
SD1_IMP_CAL_TX	This pin must be pulled down through a 100 Ω resistor.	
SD1_PLL_TPA	Do not connect.	
SD2_IMP_CAL_RX	This pin must be pulled down through a 200 Ω resistor.	
SD2_IMP_CAL_TX	This pin must be pulled down through a 100 Ω resistor.	
SD2_PLL_TPA	Do not connect.	
TEST_SEL	This signal must be pulled up via a 100-1000 Ω resistor to OV_{DD} for normal machine operation.	
TEMP_ANODE, TEMP_CATHODE	TEMP_ANODE, TEMP_CATHODE are temperature diode pins on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™).	These pins may be left unconnected.

Table 15. Debug and Test Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
TRIG_IN	—	Tie low through a 2–10 kΩ resistor to GND.
TRIG_OUT/READY	This pin must NOT be pulled down during power-on reset.	This pin must be left unconnected.

8 DMA Interface

This section discusses the termination of DMA pins on the device. Table 16 shows how the DMA pins should be connected.

Table 16. DMA Pin Recommendations

Pin Name	Pin Used	Pin Not Used
$\overline{\text{DMA\_DACK}}$[0:1]	This pin is a reset configuration pin that sets the device derivative. These pins require 4.7 kΩ pull-up or pull-down resistors.	
$\overline{\text{DMA\_DACK2}}$/$\overline{\text{LCS6}}$	—	If the Local Bus function of this pin is not used, this output pin may be left floating.
$\overline{\text{DMA\_DACK3}}$/IRQ10	—	Pull high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
$\overline{\text{DMA\_DREQ}}$[0:1]	—	Pull high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{DMA\_DREQ2}}$/$\overline{\text{LCS5}}$	—	If the Local Bus function of this pin is not used, this output pin may be left floating.
$\overline{\text{DMA\_DREQ3}}$/IRQ9	—	Pull high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
$\overline{\text{DMA\_DDONE}}$[0:1]	—	These output pins may be left floating.
$\overline{\text{DMA\_DDONE2}}$/$\overline{\text{LCS7}}$	—	If the Local Bus function of this pin is not used, this output pin may be left floating.
$\overline{\text{DMA\_DDONE3}}$/IRQ11	—	Pull high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.

9 DUART Interface

This section discusses the termination of DUART pins on the device. Table 17 shows how the DUART pins should be connected.

Table 17. DUART Pin Recommendations

Pin Name	Pin Used	Pin Not Used
$\overline{\text{UART\_CTS}}$[0:1]	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{UART\_RTS}}$[0:1]	—	These output pins may be left floating.
UART_SIN[0:1]	—	Tie low through a 2–10 kΩ resistor to GND.
UART_SOUT[0:1]	—	These output pins may be left floating.

10 Ethernet Management Interface

This section discusses the termination of the Ethernet Management pins on the device. Table 18 shows how the Ethernet Management pins should be connected.

Table 18. Ethernet Management Pin Recommendations

Pin Name	Pin Used	Pin Not Used
EC_MDC	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
EC_MDIO	—	Tie high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.

11 eTSEC Interface

This section discusses the termination of the Ethernet pins on the device. Table 19 shows how the Ethernet pins should be connected.

Table 19. Ethernet Pin Recommendations

Pin Name	Pin Used	Pin Not Used
TSEC1_COL	—	Tie low through a 2–10 kΩ resistor to GND.
TSEC3_COL	—	
TSEC1_CRS	—	
TSEC3_CRS	—	
TSEC1_GTX_CLK	—	These output pins may be left floating.
TSEC3_GTX_CLK	—	
TSEC1_RX_CLK	—	Tie high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively
TSEC3_RX_CLK	—	Tie high or low through a 2–10 kΩ resistor to TV_{DD} or GND, respectively.
TSEC1_RX_DV	—	Tie low through a 2–10 kΩ resistor to GND.
TSEC3_RX_DV	—	
TSEC1_RX_ER	—	
TSEC3_RX_ER	—	
TSEC1_RXD[7:0]	—	Tie high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively.
TSEC3_RXD[7:0]	—	Tie high or low through a 2–10 kΩ resistor to TV_{DD} or GND, respectively.
TSEC1_TX_CLK	—	Tie high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively

Table 19. Ethernet Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
TSEC3_TX_CLK	—	Tie high or low through a 2–10 kΩ resistor to TV_{DD} or GND, respectively.
TSEC1_TX_EN	These pins require an external 4.7 kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven (during reset).	These output pins may be left floating.
TSEC3_TX_EN		
TSEC1_TX_ER	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
TSEC3_TX_ER		
TSEC1_TXD[7:0]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
TSEC3_TXD[7:0]		

12 I^2C Interface

This section discusses the termination of I^2C pins on the device. Table 20 shows how the I^2C pins should be connected.

Table 20. I^2C Pin Recommendations

Pin Name	Pin Used	Pin Not Used
IIC1_SCL	Tie these open-drain signals high through a 1 kΩ resistor to OV_{DD}.	Tie high through a 2–10 kΩ resistor to OV_{DD}.
IIC2_SCL		
IIC1_SDA		
IIC2_SDA		

13 JTAG Interface

The correct operation of the JTAG interface requires that a group of system control pins be configured as demonstrated in Figure 12. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP

interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 12 allows the COP port to independently assert HRESET or TRST, while ensuring that the target can drive HRESET as well.

The COP interface has a standard header, shown in Figure 11, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 11 is common to all known emulators.

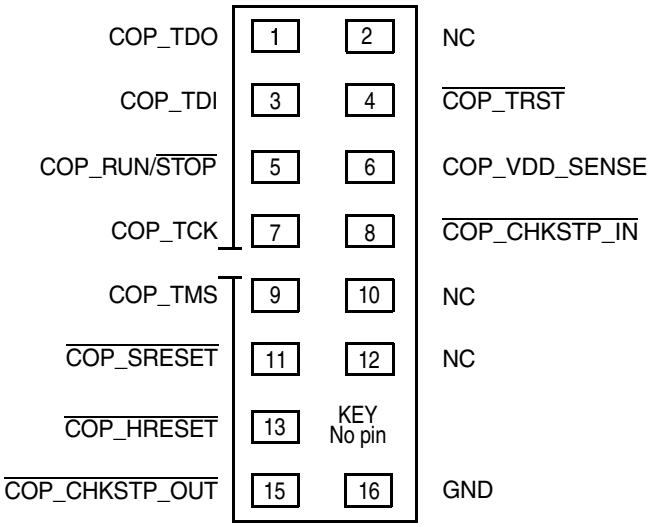
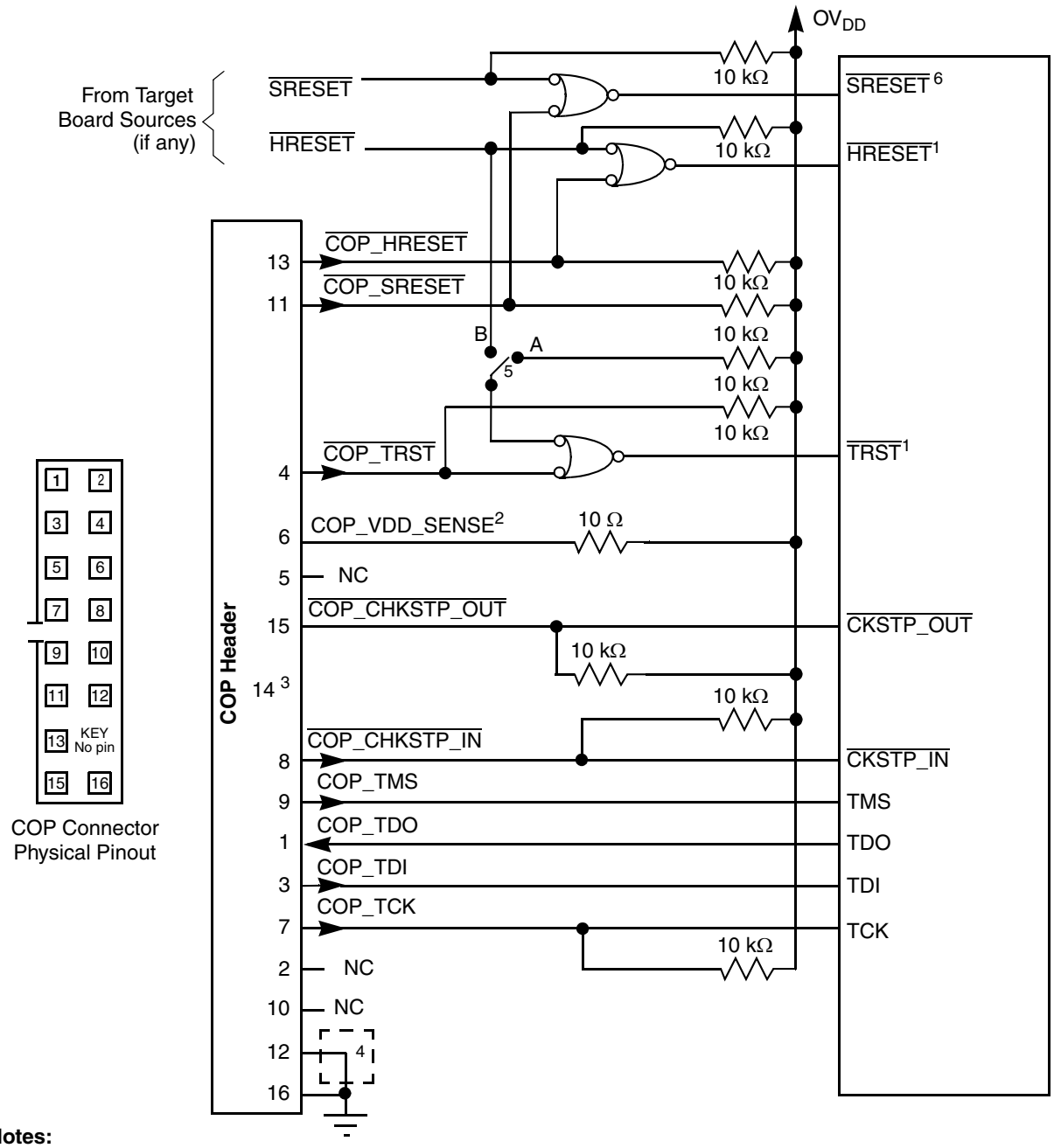


Figure 11. COP Connector Physical Pinout



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10-Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 12. JTAG Interface Connection

13.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 12. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, or TDO.

13.2 JTAG Pins

Table 21 shows how the JTAG pins should be connected.

Table 21. JTAG Pin Recommendations

Pin Name	Pin Used	Pin Not Used
TCK	If COP is used then connect as needed plus strap to OVDD via 10K pullup.	If COP is unused; Tie TCK to OVDD through a 10 kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
TDI	This pin has a weak internal pull-up P-FET that are always enabled. Connect to Pin3 of the COP connector	This pin may be left unconnected.
TDO	Connect to Pin1 of the COP connector	This pin may be left unconnected.
TMS	This pin has a weak internal pull-up P-FET that are always enabled. Connect to Pin9 of the COP connector	This pin may be left unconnected.
TRST	This pin has a weak internal pull-up P-FET that are always enabled. Connect to Pin4 of the COP connector and $\overline{\text{HRESET}}$ from the board	$\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 Ω resistor.

13.3 JTAG Checklist

Table 22 provides a summary POR and reset checklist for the designer.

Table 22. Checklist for JTAG

Item	Description	Completed
3.	Connect the JTAG pins to the COP header as shown in Figure 12.	

14 Local Bus Interface

This section discusses the termination of Local Bus pins on the device. Table 23 shows how the Local Bus pins should be connected.

Table 23. Local Bus Pin Recommendations

Pin Name	Pin Used	Pin Not Used
LA27	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LA[28:31]	This pin is a reset configuration pin that sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors.	
LAD[0:31]	Note that the LSB for the address = LAD[24:31]; however, the MSB for the data is on LAD[0:7].	Tie high or low through a 2–10 kΩ resistor to BV_{DD} or GND, respectively, if the general purpose POR configuration is not used.
LALE	This pin is a reset configuration pin that sets the e500 core clock to CCB Clock PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors.	
LBCTL		
LCLK[0:2]	—	These output pins may be left floating.
LCKE	—	
$\overline{\text{LCS}}$[0:4]	—	
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	—	If the DMA functions of these pins are not used, these output pins may be left floating.
$\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$	—	
$\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$	—	
LGPL0/LSDA10	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR defaults are acceptable, these output pins may be left floating.
LGPL1/$\overline{\text{LSDWE}}$		
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$	This pin is a reset configuration pin that sets the e500 core clock to CCB Clock PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors.	
LGPL3/$\overline{\text{LSDCAS}}$	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LPBSE	—	This pin either needs to be pulled-up via a 2–10 kΩ resistor to BV_{DD} or needs to be reconfigured as LPBSE prior to boot-up.
LGPL5	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LSYNC_IN	LSYNC_IN needs to be connected via a trace to LSYNC_OUT of length equal to the longest LCK*n* signal used.	LSYNC_IN needs to be directly connected to LSYNC_OUT.
LSYNC_OUT		

Table 23. Local Bus Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/$\overline{\text{LSDDQM0}}$	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR defaults are acceptable, these output pins may be left floating.
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$/$\overline{\text{LSDDQM1}}$		
$\overline{\text{LWE2}}$/$\overline{\text{LBS2}}$/$\overline{\text{LSDDQM2}}$		
$\overline{\text{LWE3}}$/$\overline{\text{LBS3}}$/$\overline{\text{LSDDQM3}}$		

15 PCI Interface

This section discusses the termination of PCI pins on the device.

15.1 Unrealized $\overline{\text{RST}}$ Pin

The MPC8533E does not implement for the PCI interface a specific RST pin separate from the rest of the device pins. Instead, the PCI $\overline{\text{RST}}$ is realized with the $\overline{\text{HRESET}}$ input.

15.2 PCI Pins

Table 24 shows how the PCI pins should be connected. Unless otherwise noted, unused inputs need be tied to their inactive state through a 2–10 kΩ resistor, and unused I/Os need be tied high or low through a 2–10 kΩ resistor to OV_{DD} and GND, respectively.

Table 24. PCI Pin Recommendations

Pin Name	Pin Used	Pin Not Used
PCI1_AD[31:0]	—	If PCI arbiter is enabled during POR, All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating. If PCI arbiter is disabled during POR, All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OVdd through a single (or multiple) 10K ohm resistor(s)
PCI1_AD[31:0]	—	
PCI1_C_$\overline{\text{BE}}$[3:0]	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
PCI1_CLK	If PCI1 is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI1_CLK, otherwise the processor will not boot up.	Tie high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively,
$\overline{\text{PCI1\_DEVSEL}}$	A weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.	
$\overline{\text{PCI1\_FRAME}}$		
$\overline{\text{PCI1\_GNT0}}$	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.

Table 24. PCI Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
$\overline{\text{PCI1\_GNT}}$[4:1]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI*n*_AD pins as "No Connect" or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the PCIn_AD pins are not connected to any other PCI device. The PCI block will drive the PCIn_AD pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.	If the POR defaults are acceptable, these output pins may be left floating.
PCI1_IDSEL	—	Tie low through a 2–10 kΩ resistor to GND.
$\overline{\text{PCI1\_IRDY}}$	A weak pull-up resistor (2–10 kΩ) need be placed on this pin to OV_{DD}.	
PCI1_PAR	—	Tie low through a 2–10 kΩ resistor to GND.
—	—	
$\overline{\text{PCI1\_PERR}}$	A weak pull-up resistor (2–10 kΩ) need be placed on this pin to OV_{DD}.	
$\overline{\text{PCI1\_REQ0}}$	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{PCI1\_REQ}}$[4:1]	—	
$\overline{\text{PCI1\_SERR}}$	A weak pull-up resistor (2–10 kΩ) need be placed on this pin to OV_{DD}.	
$\overline{\text{PCI1\_STOP}}$		
$\overline{\text{PCI1\_TRDY}}$		

16 PIC Interface

This section discusses the termination of programmable interrupt controller pins on the device. Table 25 shows how the PIC pins should be connected.

Table 25. PIC Pin Recommendations

Pin Name	Pin Used	Pin Not Used
IRQ[0:8]	A weak pull-up or pull-down may be needed to the inactive state.	Tie high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively,
IRQ9/$\overline{\text{DMA\_DREQ3}}$		
IRQ10/$\overline{\text{DMA\_DACK3}}$		
IRQ11/$\overline{\text{DMA\_DDONE3}}$		

Table 25. PIC Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
IRQ_OUT	Pull high through a 2–10 kΩ resistor to OV_{DD}.	
MCP		
UDE		

17 SerDes Interface

This section discusses the termination of SerDes pins on the device. Table 26 and Table 27 show how the SerDes pins should be connected. Note that the SerDes must always have power applied to its supply pins.

Table 26. SerDes1 Pin Recommendations

Pin Name	Pin Used	Pin Not Used
SD1_PLL_TPD	Do not connect.	
SD1_PLL_TPA		
SD1_RX[0:7]	—	These pins must be connected to GND.
$\overline{\text{SD1\_RX}}$[0:7]		
SD1_TX[0:7]	—	These pins must be left unconnected.
$\overline{\text{SD1\_TX}}$[0:7]		
SD1_IMP_CAL_RX	This pin must be pulled down through a 200 Ω resistor.	
SD1_IMP_CAL_TX	This pin must be pulled down through a 100 Ω resistor.	
SD1_REF_CLK	—	These pins must be connected to GND.
SD1_REF_CLK	—	These pins must be connected to GND.
SD1_TST_CLK	Do not connect.	
SD1_TST_CLK	Do not connect.	

Table 27. SerDes2 Pin Recommendations

Pin Name	Pin Used	Pin Not Used
SD2_PLL_TPD	Do not connect.	
SD2_PLL_TPA	Do not connect.	
SD2_RX[0]	—	These pins must be connected to GND.
SD2_RX[2]	These pins must be connected to GND.	
SD2_RX[3]	These pins must be connected to GND.	
SD2_RX[0]	—	These pins must be connected to GND.
SD2_RX[2]	These pins must be connected to GND.	
SD2_RX[3]	These pins must be connected to GND.	

Table 27. SerDes2 Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
SD2_TX[0]	—	These pins must be left unconnected.
SD2_TX[2]	These pins must be left unconnected.	
SD2_TX[3]	These pins must be left unconnected.	
SD2_TX[0]	—	These pins must be left unconnected.
SD2_TX[2]	These pins must be left unconnected.	
SD2_TX[3]	These pins must be left unconnected.	
SD2_IMP_CAL_RX	This pin must be pulled down through a 200 Ω resistor.	
SD2_IMP_CAL_TX	This pin must be pulled down through a 100 Ω resistor.	
SD2_REF_CLK	—	These pins must be connected to GND.
SD2_REF_CLK	—	These pins must be connected to GND.
SD2_TST_CLK	Do not connect.	
SD2_TST_CLK	Do not connect.	

18 System Control

This section discusses the termination of system control pins on the device. Table 28 shows how the system control pins should be connected.

Table 28. System Control Pin Recommendations

Pin Name	Pin Used	Pin Not Used
CKSTP_IN	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin7 of the COP connector (refer to Figure 12).	Pull high through a 2–10 kΩ resistor to OV_{DD}.
CKSTP_OUT	Pull this open-drain signal high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin15 of the COP connector (refer to Figure 12).	Pull high through a 2–10 kΩ resistor to OV_{DD}
HRESET	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin13 of the COP connector (refer to Figure 12).	
HRESET_REQ	Pull high through a 2–10 kΩ resistor to OV_{DD}. This pin must NOT be pulled down during power-on reset.	This pin must NOT be pulled down during power-on reset.
SRESET	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin11 of the COP connector (refer to Figure 12).	Pull high through a 2–10 kΩ resistor to OV_{DD}.

19 Spare Configuration Pins

Several pins on the MPC8533E are marked per configuration as shown in Table 29. The spare pins are unused POR config pins. It is highly recommended that the customer provide the capability of setting these

pins low (that is, pull-down resistor which is not currently stuffed) in order to support new config options should they arise between revisions.

Table 29. RESERVED Pin Recommendations

Pin Name	Pin Number	Comment
EC_MDC	AC7	cfg_spare[0]
TSEC1_TXD[7]	T5	cfg_spare[1]
TSEC1_TXD[3]	V2	cfg_spare[2]
TSEC3_TXD[7]	M7	cfg_spare[3]

20 Power and Ground Signals

The MPC8533E has several power supplies. Table 30 shows how the SerDes pins should be connected.

Table 30. Power and Ground Pin Recommendations

Pin	Comment
AV_{DD}_CORE	Power supply for e500 PLL (1.0 V through a filter).
AV_{DD}_LBIU	Power supply for Local Bus PLL (1.0 V through a filter).
AV_{DD}_PCI1	Power supply for PCI1 PLL (1.0 V through a filter).
AV_{DD}_PLAT	Power supply for core complex bus PLL. (1.0 V through a filter)
AV_{DD}_SRDS	Power supply for SerDes PLL (1.0 V through a filter).
AV_{DD}_SRDS2	Power supply for SerDes PLL (1.0 V through a filter).
BV_{DD}	Power supply for the Local Bus I/Os (1.8 V, 2.5 V / 3.3 V).
GND	—
GV_{DD}	Power supply for the DDR I/Os (1.8 V / 2.5 V).
LV_{DD}	Power supply for the TSEC1 I/Os (2.5 V / 3.3 V).
MVREF	DDR input reference voltage equal to approximately half of GV_{DD}
OV_{DD}	Power supply for PCI and other standards' I/Os (3.3 V).
SENSEVDD	This pin is connected to the V_{DD} plane internally and may be used by the core power supply to improve tracking and regulation.
SENSEVSS	This pin is connected to the GND plane internally and may be used by the core power supply to improve tracking and regulation.
SV_{DD}_SRDS	Power supply for the SerDes 1 transceivers (1.0 V).
SV_{DD}_SRDS2	Power supply for the SerDes 2 transceivers (1.0 V).
XV_{DD}_SRDS	Pad Power for SerDes 1 transceivers (1.0 V)
XV_{DD}_SRDS2	Pad Power for SerDes 2 transceivers (1.0 V)
XGND_SRDS	SerDes 1 GND

Table 30. Power and Ground Pin Recommendations (continued)

Pin	Comment
XGND_SRDS2	SerDes 2 GND
AGND_SRDS	SerDes 1 PLL GND
AGND_SRDS2	SerDes 2 PLL GND
TV_{DD}	Power supply for the TSEC3 I/Os (2.5 V / 3.3 V).
XV_{DD}	Power supply for the SerDes I/Os (1.0 V).
V_{DD}	Power supply the core I/Os (1.0 V).

21 Documentation History

Table 31 provides a revision history for this application note.

Table 31. Document Revision History

Revision	Date	Substantive Change(s)
3	3/2011	• Updated introductory paragraph in Section 4.2, “Pin Map.” • Removed duplicate pin lists.
2	2/2009	• Added Table 3, “Estimated I/O Power Dissipation.” • Updated Table 28, “System Control Pin Recommendations.”
1	10/2008	• In Section 4.2, “Pin Map,” changed “top view of the pin map” to “bottom view of the pin map.”
0	7/2008	• Initial Release

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