Freescale Semiconductor
Application Note

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SGTL5000 I²S DSP Mode

Contents

1 Description

SGTL5000 supports multiple forms of I^2S communication for digital input/output. Along with the more typical Left- or Right-justified configuration, SGTL5000 includes support for a mode aimed at signals as seen in digital signal processing (DSP) applications, e.g. Bluetooth transceivers. This document will help explain the usage and configuration of SGTL5000's I^2S DSP mode.

2 DSP Mode

The purpose of the I^2S DSP Mode (A/B) is to interface with various external devices, such as Bluetooth transceivers. Where it differs from standard I2S is that the frame clock does not represent a different channel when high or low, but is a bit-wide pulse that marks the start of a frame. Data is aligned such that the left channel data is immediately followed by right channel data. Zero padding is filled in for the remaining bits. The data and frame clock may be configured to clock in on the rising or falling edge of Bit Clock.

SGTL5000 supports LRCLK frequencies of as low as 8kHz, for Bluetooth-type applications by accepting an input clock, and dividing down to the necessary LRCLK.

To specify the proper rate, the following should be written to RATE_MODE (bits 5:4) in CHIP_CLK_CTRL:

0x0 = SYS_FS specifies the rate

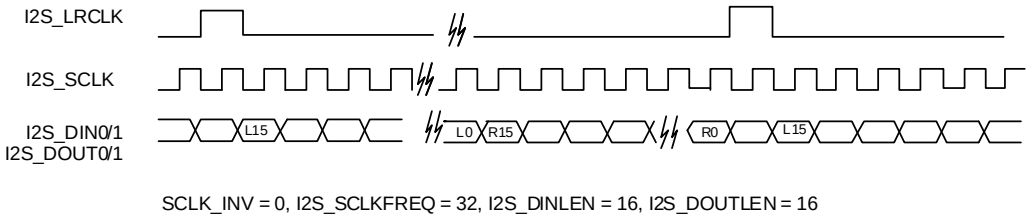
0x1 = Rate is 1/2 of the SYS_FS rate

0x2 = Rate is 1/4 of the SYS_FS rate

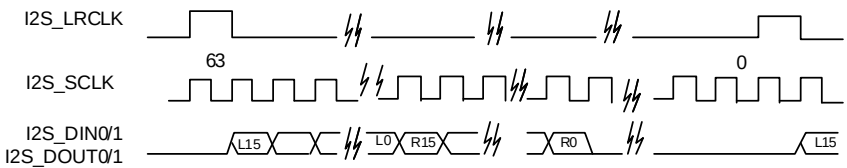
0x3 = Rate is 1/6 of the SYS_FS rate

e.g. to get an 8kHz Bluetooth sample rate from an incoming 48kHz clock, 0x3 must be written to RATE_MODE.

The following are functional diagrams of DSP mode with 32 and 64 SCLKFREQ, respectively:



SCLK_INV = 0, I2S_SCLKFREQ = 32, I2S_DINLEN = 16, I2S_DOUTLEN = 16



SCLK_INV = 1, I2S_SCLKFREQ = 64, I2S_DINLEN = 16, I2S_DOUTLEN = 16

To enable DSP Mode in SGTL5000, write 0x2 to I2S_MODE (bits 3:2) in CHIP_I2S0_CTRL. Data alignment is crucial. Both the sender and receiver of data must be set up identically to properly transmit information. For example, in order to transmit to an Audio Precision 2700, the data must be aligned on the falling edge of I2S_SCLK, therefore, SCLK_INV (bit 6:6) in CHIP_I2S0_CTRL must be set.

Figure 1, Figure 2 and Figure 3, following, show oscilloscope outputs of DSP Mode.

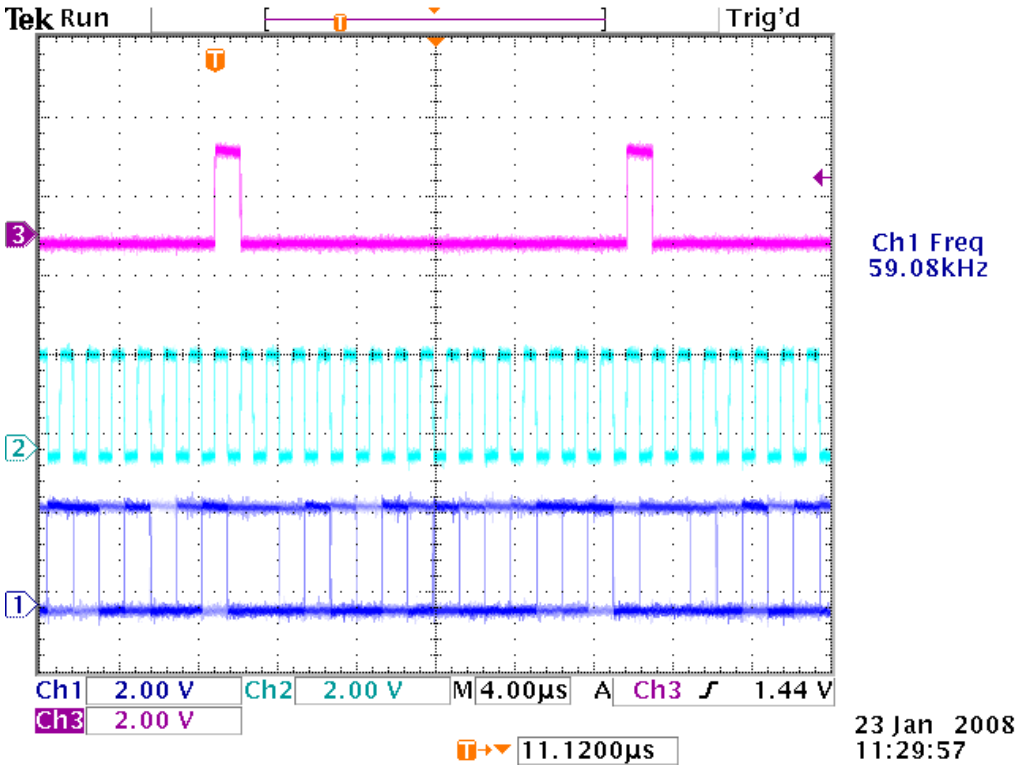


Figure 1. Here, showing a 32-bit frame, with left- and right-channel data being transmitted

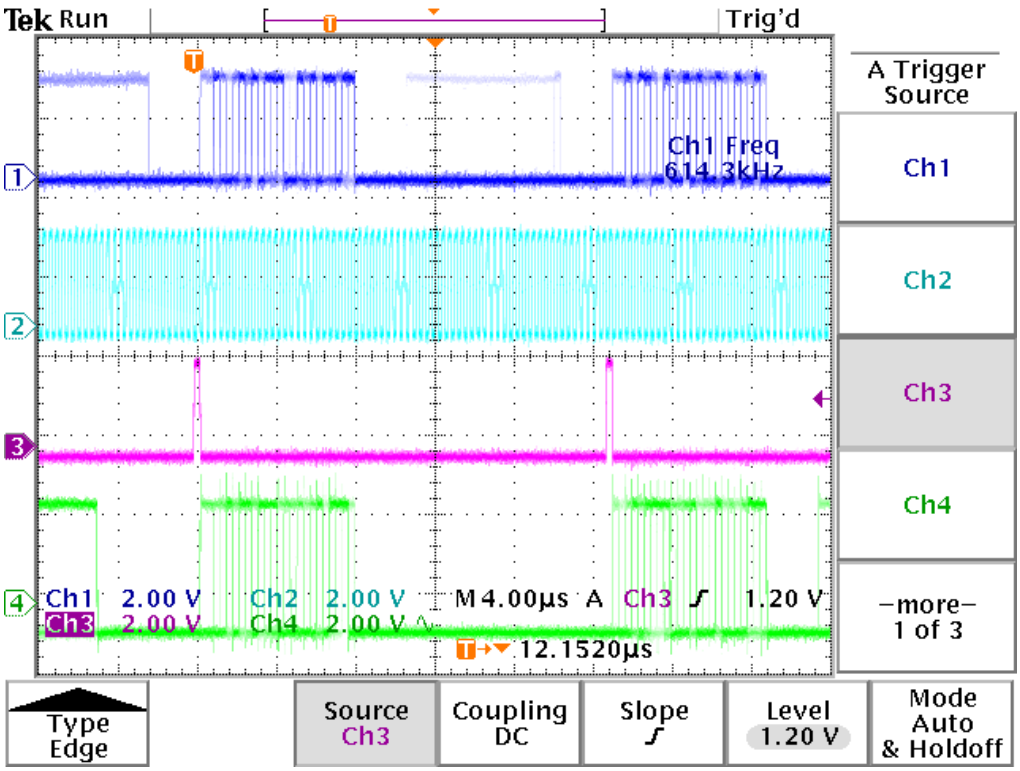


Figure 2. SGTL5000 also supports 32-bit-per-channel data, using a 64-SCLK frame

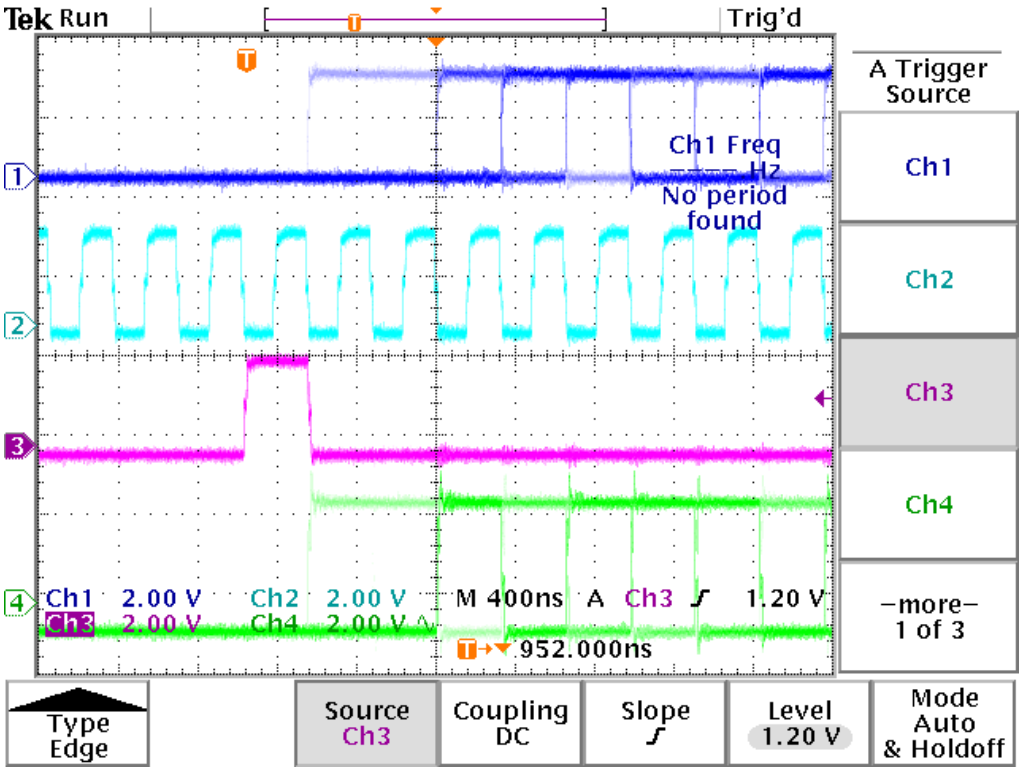


Figure 3. Close-up of data alignment in reference to the LR bit-pulse (Ch 3)

3 Conclusion

SGTL5000 offers compatibility with many different digital I/O schemes in order to provide support to as many applications as possible. Understanding the use of DSP mode will ensure proper communication between a Bluetooth-type device and SGTL5000.

4.0 Revision History

REVISION	DESCRIPTION
2.0	25 November 2008 - Initial release. 11 November 2011 - Deleted "Preliminary—Subject to Change Without Notice" - Updated Freescale form and style.

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