Freescale Semiconductor
Application Note

Document Number:AN4554
Rev. 0, 7/2012

Interfacing MC33903/4/5 With MC9S08DZ60

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Contents

1 Introduction

System Basis Chip (SBC) combines several popular functions typically used in automotive microcontroller unit (MCU) based systems and utilize Freescale's SMARTMOS technology.

The SBC devices contain a combination of low-dropout (LDO) voltage regulator(s), switching voltage regulator(s), high-side switches, and one or more physical layer transceivers such as CAN, LIN, and PSI5. These devices are controlled by an MCU through a SPI interface. The prominent features of SBCs include:

- Can operate in various power-saving modes such as Standby, Sleep, and Stop
- Configurable wake-up sources
- In-built voltage regulator
- One or more high-side switches
- Configurable watchdog timer
- Overcurrent detection
- Undervoltage protection

The MC33903/4/5 is the second generation family of the SBCs. It combines several features and enhances present module designs. The device works as an advanced power management unit for the MCU with additional integrated circuits such as sensors and CAN transceivers. It has a built-in enhanced high-speed CAN interface complying to the ISO11898-2 and ISO1198-5 standards with local and bus failure diagnostics, protection, and Fail-safe operation modes.

The SBCs may include up to two LIN 2.1 interfaces and up to four wake-up input pins that can also be configured as output drivers for flexibility. The block diagram of the second generation SBC (SBC Gen2) family is shown in Figure 1.

MC33903 implements multiple Low-Power (LP) modes, with very low-current consumption. In addition, the device is a part of the family concept where pin-compatibility adds versatility to module design.

This application note describes how to interface MC33903 with the MC9S08DZ60. The same can be extended to MC33903/4/5 complete Gen2 family.

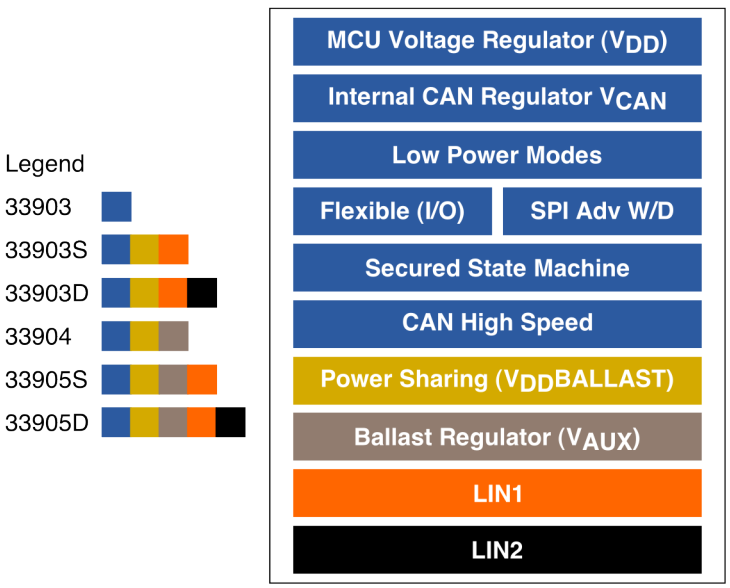


Figure 1. MC33903/4/5 block diagram

2 Hardware interface description

The MC33903 features one Voltage Regulator with power management, which can be either 5V or 3.3V compatible, CAN transceiver (ISO11898-2 and 11898-5 compliant) with 5V-CAN regulator for CAN driver supply, configurable I/O with wake-up functionalities, watchdog capabilities and secured SPI interface for configuring the SBC. The internal block diagram of MC33903 is shown in Figure 2 with all the pin connections. The description of each pin is given in Table 1.

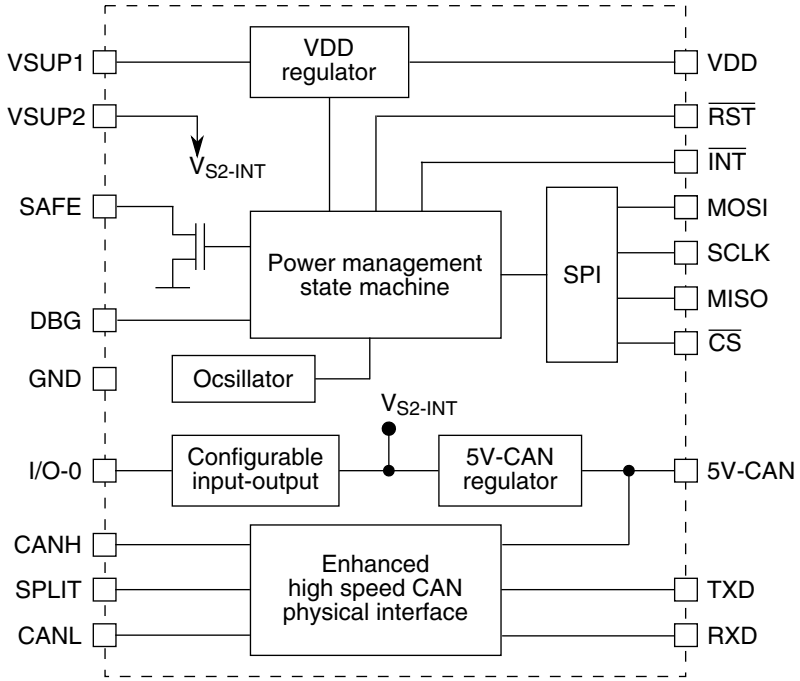


Figure 2. MC33903 internal block diagram

Table 1. MC33903 pin definitions

Pin Number	Pin Name	Pin Function	Formal Name	Definition
3-4,11-13, 17-21, 31, 32	N/C	No connect	-	No connection
1	VSUP1	Power	Battery Voltage Supply 1	Supply input for the device internal supplies, power on reset circuitry and the V_{DD} regulator.
2	VSUP2	Power	Battery Voltage Supply 2	Supply input for 5 V-CAN regulator, VAUX regulator, I/O and LIN pins.
5	SAFE	Output	Safe Output (Active LOW)	Output of the safe circuitry. The pin is asserted LOW in case of a safe condition is detected (e.g.: software watchdog is not triggered, VDD low, issue on the RESET pin, etc.). Open drain structure.
6	5 V-CAN	Output	5V-CAN	Output voltage for the embedded CAN interface. A capacitor must be connected to this pin.
7	CANH	Output	CAN High	CAN high output
8	CANL	Output	CAN Low	CAN low output
9	GND-CAN	Ground	GND-CAN	Power GND of the embedded CAN interface
10	SPLIT	Output	SPLIT Output	Output pin for connection to the middle point of the split CAN termination

Table continues on the next page...

Table 1. MC33903 pin definitions (continued)

Pin Number	Pin Name	Pin Function	Formal Name	Definition
15	IO-0	Input/Output	Input/Output 0	Configurable pin as an input or output, for connection to external circuitry (switched or small load). The voltage level can be read by the SPI and via the MUX output pin. The input can be used as a programmable wake-up input in Low Power mode. In low power, when used as an output, the high side or low side can be activated for a cyclic sense function.
16	DBG	Input	Debug	Input to activate the Debug mode. In Debug mode, no watchdog refresh is necessary. Outside of Debug mode, connection of a resistor between DBG and GND allows the selection of Safe mode functionality.
22	RST	Output	Reset Output (Active LOW)	This is the device reset output whose main function is to reset the MCU. This pin has an internal pullup to V_{DD}. The reset input voltage is also monitored in order to detect external reset and safe conditions
23	INT	Output	Interrupt Output (Active LOW)	This output is asserted low when an enabled interrupt condition occurs. This pin is a open drain structure with an internal pullup resistor to V_{DD}.
24	CS	Input	Chip Select (Active LOW)	Chip select pin for the SPI. When the CS is low, the device is selected. In Low Power mode with V_{DD} ON, a transition on CS is a wake-up condition
25	SCLK	Input	Serial Data Clock	Clock input for the Serial Peripheral Interface (SPI) of the device
26	MOSI	Input	Master Out / Slave In	SPI data received by the device
27	MISO	Output	Master In / Slave Out	SPI data sent to the MCU. When theCS is high, MISO is high-impedance.
28	VDD	Output	Voltage Digital Drain	5.0 or 3.3 V output pin of the main regulator for the Microcontroller supply.
29	TXD	Input	Transmit Data	CAN bus transmit data input. Internal pullup to V_{DD}
30	RXD	Output	Receive Data	CAN bus receive data output
EXPAD	GND	Ground	Ground	Ground

Interfacing MC33903 with an MC9S08DZ60 is very simple and easy. The application block diagram is shown in Figure 3.

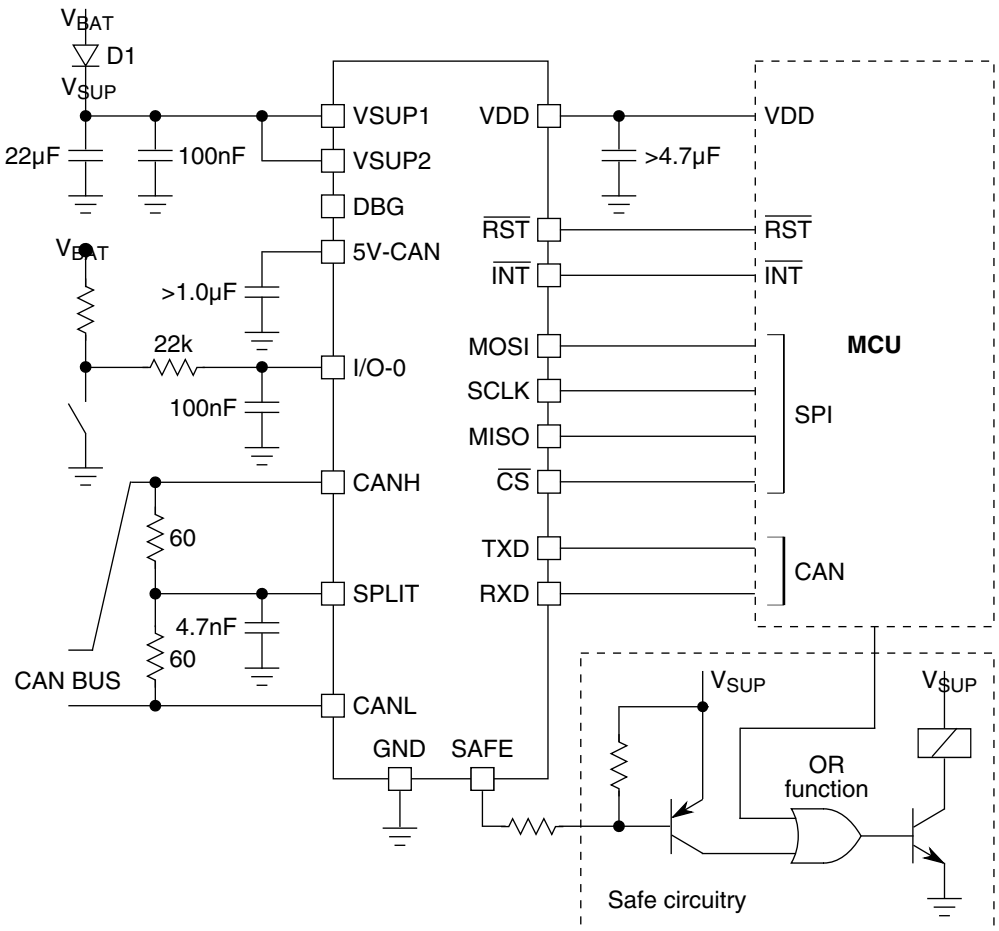


Figure 3. Application block diagram

Following is the description of MC33903 pins.

- **VSUP1** is the input pin for the device internal supply and the V_{DD} regulator. It is connected to the vehicle battery (V_{BAT}) with surge protection using a Zener diode; this allows guaranteed reset free operation of the MC9S08DZ60 during the cranking pulse, and temporary (50 ms) loss of the V_{BAT} supply.
- **V_{DD}**is the output pin of the voltage regulator for the MC9S08DZ60. The maximum DC capability of the V_{DD} is 150 mA[1]
- **RST** pin is connected to the MC9S08DZ60, generally through a strong pullup, to provide a reset pulse under various failure conditions, like, undervoltage at the V_{DD} pin, failure in watchdog refresh operation.
- **INT** pin is the output of the SBC. It is asserted low or generates a low pulse when an interrupt condition occurs. This pin has an internal pullup structure to V_{DD}, as is the case with RST pin, but it is recommended to have an external pullup.
- **DBG** is an input pin, and has a dual functionality. When voltage between 8.0–10.0 V is applied, it forces the SBC to enter Debug mode and when it is pull-GND through a resistor, Fail-safe mode operation may be selected depending on the values of the resistor. See Table 2 for more details. Flexibility is provided to the user to select various modes configurable through SPI commands, which will have a higher priority than the circuitry present at the DBG pin.

1. This is the maximum current, when the device is in NORMAL mode.

- MC33903 has a CAN physical transceiver, whose inputs, **TXD** and **RXD**, are connected to the MC9S08DZ60's CAN interface, **TXCAN** and **RXCAN** respectively. **CANH** and **CANL** are the differential signals of the high-speed CAN bus, compliant with **ISO 11898-5**.
- **SBC** can be configured using the SPI bus, which is the basic interface required to make it operational.

Table 2. Fail-safe options

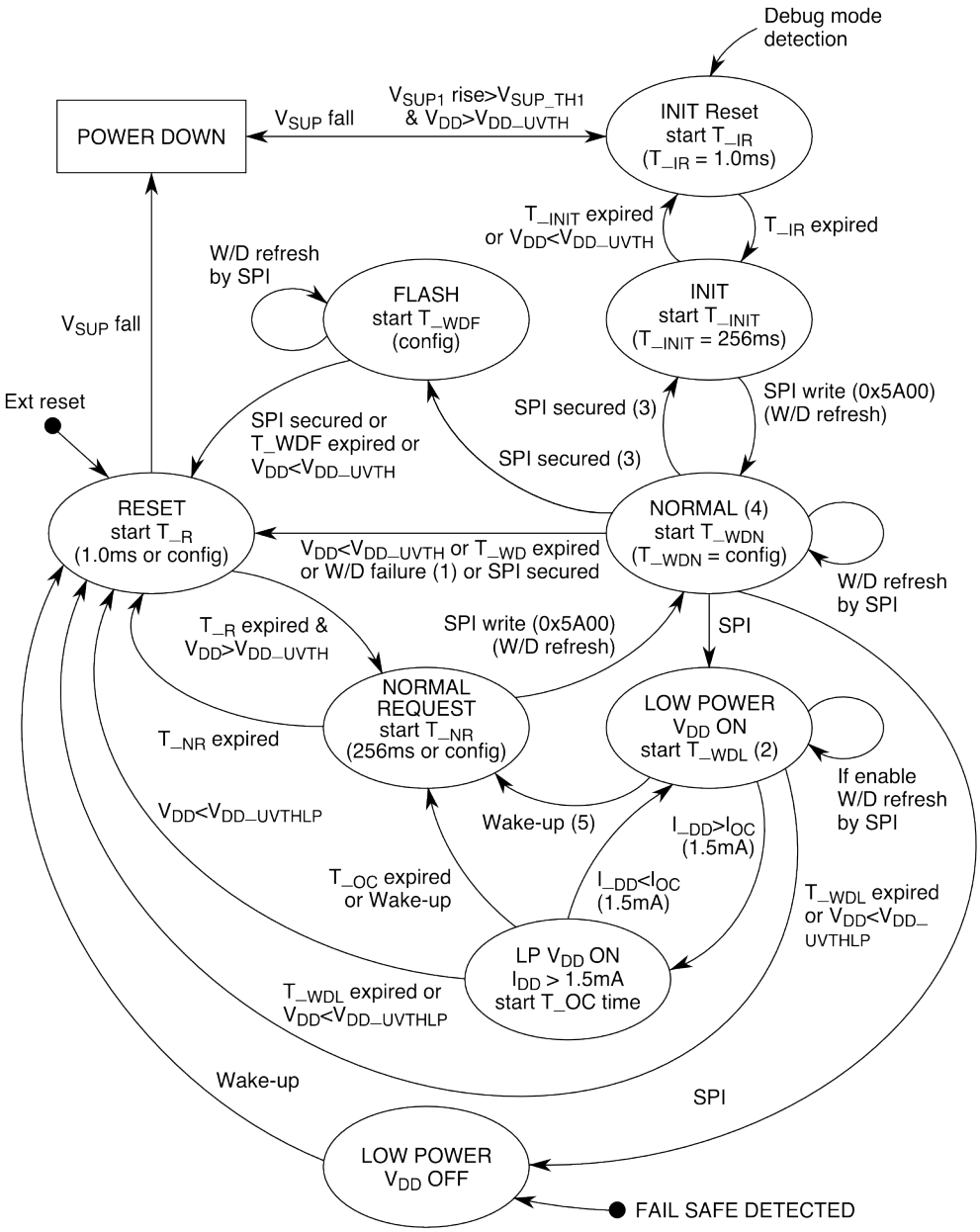
Resistor at DBG pin	Safe mode code	Mode description	V_{DD} status
<6.0 kΩ	A	MCU remains powered, until the failure condition is recovered through S/W	Remains ON
15 kΩ	B1	Disables the MCU supply and continues to monitor external event like CAN traffic	Turn OFF 8.0 s after CAN traffic bus idle detection

3 Software interface description

This section describes in detail, the software interface required for interfacing MC9S08DZ60.

3.1 Functional modes

MC33903 can be configured to operate in different modes by using the SPI commands. In order to understand the SBC, the user must be well-versed with the different modes of SBC, which are summarized in Figure 4.



(1) W/D refresh in closed windows or enhanced W/D refresh failure.
(2) If enable by SPI, prior to enter LP V_{DD} ON mode.
(3) V_{DD} external PNP is disable in all mode except Normal and Flash modes.
(4) Wake-up from LP Vnn ON mode by SPI command is done by a SPI mode change: 0x5C10.

Figure 4. State diagram

1. When the SBC is powered-up, it transitions to INIT RESET mode automatically, during which the RST pin is asserted low for duration of typically 1.0 ms ($T_{\_IR}$). BATFAIL flag will be set to indicate the device is coming from an unpowered condition, and all previous device configurations will be lost.
2. After INIT RESET, the SBC automatically transitions to INIT mode, in which it must be configured through SPI, within 256 ms ($T_{\_INIT}$), and a Watchdog (W/D) refresh command must be issued on MOSI, failing which SBC transitions back to INIT RESET mode and if successful, it will transition to NORMAL mode.

   W/D refresh command must be issued periodically by the MCU in NORMAL mode, within the specified time ($T_{\_WDN}$), as was configured via SPI.
3. If the MCU does not issue the W/D refresh command, SBC will transition to RESET mode, in which the RST pin is asserted low, for duration of typically 1.0 ms ($T_{\_R}$), and will transition to NORMAL REQUEST mode. A W/D refresh

command is necessary to transition to NORMAL mode from NORMAL REQUEST mode. The duration of the NORMAL REQUEST mode is 256 ms ($T_{\_NR}$).

There are two low-power modes which can be entered on request by MCU, via SPI commands.

- LOW POWER V_{DD} ON mode: As the name suggests, in this mode, the internal regulator will remain ON and will supply 5.0 V to MCU, through its V_{DD} pin.
- LOW POWER V_{DD} OFF mode: In this mode, no power is supplied to the MCU.

In each of these modes, wake-up sources can be configured via SPI, and after receiving any one of the wake-ups, the SBC will transition to the modes as shown in Figure 4.

3.2 SPI commands

For configuring the SBC, MC9S08DZ60 must read all the flags, using the SPI Read command, to check the source of the wake-up, reset or the interrupt, and then configure the corresponding register for wake-up (WU)/reset (RST)/interrupt (INT) source(s) according to the requirement.

When the SBC status flags are read at power-up, they will show that INT/WU/RST source is from a regulator event. At this moment, if VREG flags are read, by issuing 0xDF00 or 0xDF80 on MOSI, MISO will show that the VSUP_BATFAIL bit (bit 1 of the return status) is set, indicating that the SBC is coming out of the POWER DOWN mode. Wait for SBC to transition to INIT mode, 1.0 ms from the time the SBC is powered-up, and then configure INIT Registers, INIT Wdog, INIT REG, INIT LIN I/O, and INIT MISC, as they can only be set when the SBC is in INIT mode. On MOSI, issue a command 0x5A00, W/D refresh command, so that SBC transitions from INIT mode to NORMAL mode.

NOTE

One must check the mode of the SBC by issuing 0xDD80 on MOSI and monitor the bits 7–3 on MISO as shown in Table 3,[2] and if the mode is not INIT, then reissue the command 0x5A00, till SBC transitions to NORMAL mode and whole process must be completed with 256 ms, otherwise the SBC will transition to INIT RESET mode.

Table 3. MISO bits 7–3 (SBC current mode)

b7	b6	b5	b4	b3	Mode
0	0	0	0	0	INIT
0	0	0	0	1	FLASH
0	0	0	1	0	NORMAL REQUEST
0	0	0	1	1	NORMAL mode
1	x	x	x	x	Low-Power mode

The user must configure the CAN, voltage regulator, and the Interrupt Source register as per the requirement of the application.

4 Conclusion

This application note has described the hardware and software aspects of interfacing the MC33903, SBC Gen2 with MC9S08DZ60, and HCS08 CPU.

2. Please refer to MC33903_4_5, System Basis Chip Gen2 with High Speed CAN and LIN Interface, available on http://www.freescale.com

5 References

The following reference materials are available on http://www.freescale.com.

- S08D: 8-bit Cost-Effective with CAN D MCUs
- MC33903: System Basis Chip Gen2 with High-speed CAN and LIN Interfaces
- MC33903_4_5 : MC33903_4_5, System Basis Chip Gen2 with High Speed CAN and LIN Interface
- MC33903_4_5FS : MC33903_4_5FS, System Basis Chip Gen2 with High Speed CAN and LIN Interface
- MC9S08DZ60 : MC9S08DZ60, MC9S08DZ48, MC9S08DZ32, MC9S08DZ16–Data Sheet

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Document Number: AN4554
Rev. 0, 7/2012