Freescale Semiconductor
Application Note

Document Number: AN4576
Rev. 1, 3/2013

i.MX 6DualLite Power Consumption Measurement

This application note helps the user design power management systems. Through several use cases, this report illustrates current drain measurements of the i.MX 6DualLite applications processors taken on the Freescale SABRE SD Platform. The reader will be enabled to choose the appropriate power supply domains for the i.MX 6DualLite chips and become familiar with the expected chip power in different scenarios.

NOTE

Because the data presented in this application note is based on empirical measurements on a small sample size, the results presented are not guaranteed.

Contents

1 Overview of i.MX 6DualLite voltage supplies

The i.MX 6DualLite processors have several power supply domains (voltage supply rails) and several internal power domains. Figure 1 shows the connectivity of these supply rails and the distribution of the internal power domains.

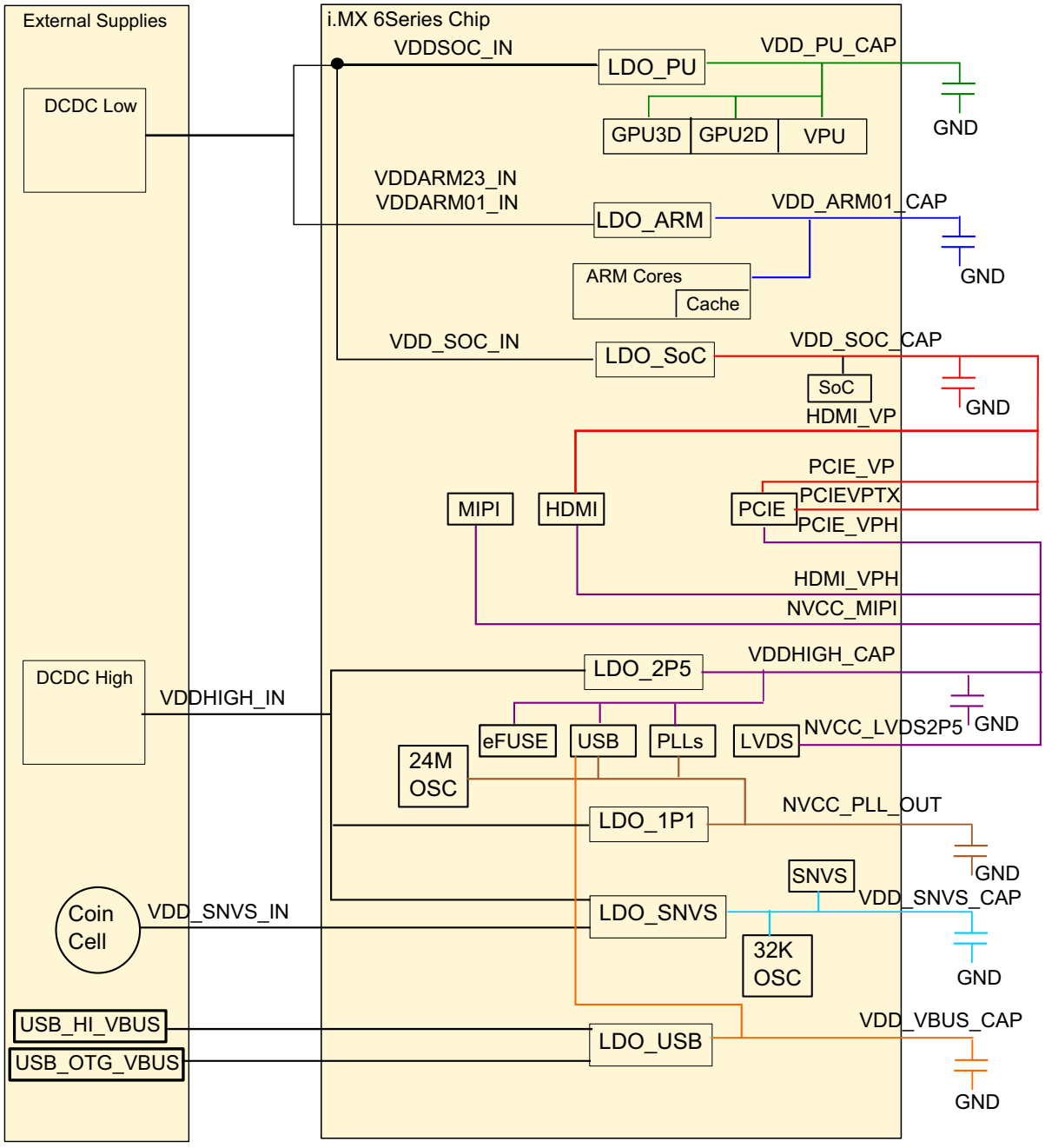

Figure 1. i.MX 6DualLite power rails

NOTE

See the *i.MX 6Solo/6DualLite Applications Processors for Consumer Products* datasheet (IMX6SDLCEC) for the recommended operating conditions of each supply rail and for a detailed description of the groups of I/Os (pins) each I/O voltage supply powers.

For more details regarding the i.MX 6DualLite power rails, see Chapter 51, “Power Management Unit (PMU),” in the *i.MX 6Solo/6DualLite Applications Processors Reference Manual* (IMX6SDLRM).

2 Internal power measurement of the i.MX 6DualLite processor

Several use cases (described in Section 3, “Use cases and measurement results”) are run on the SABRE SD Platform. The measurements are taken mainly for the following power supply domains:

- VDD_ARM_IN—ARM platform’s supply
- VDD_SOC_IN—Peripheral supply
- VDD_HIGH_IN—Source for PLLs, DDR pre-drives, PHYs, and some other circuitry

These supply domains consume the majority of the internal power of the processor. For the relevant use cases, the power of additional supply domains is added. However, the power of these supply domains does not depend on specific use cases, but whether these modules are used or not. The power consumption of SNVS is comparatively negligible except in Deep-Sleep mode.
The NVCC_* power consumption depends primarily on the board level configuration and the components. Therefore, it is not included in the i.MX 6DualLite internal power analysis. The power of NVCC_DRAM is added for reference.

The power consumption for these supplies, in different use cases, is provided in Table 3 through Table 13.

NOTE

Unless stated otherwise, all the measurements were taken on typical process silicon, at room temperature (26 °C approximately).

2.1 VDDHIGH power

The voltage VDDHIGH domain is generated from the 2.5-V LDO (LDO_2P5).

This domain powers the following circuits:

- On-chip LDOs
- Bandgap
- MLB
- eFUSE
- Analog part of the PLLs
- Pre-drivers of the DDR IOs (NVCC_LVDS_2P5)

It may also power the following domains (depends on board connectivity):

- PCIe, MIPI, and HDMI PHYs
- LVDS bridge
- Differential input buffers of the DDR IO

2.2 DDR I/O power

The DDR I/O is supplied from NVCC_DRAM which provides the power for the DDR I/O pads. The target voltage for this supply depends on the DDR interface being used. The target voltages for the different DDR interfaces are as follows:

- 1.5 V for DDR3
- 1.2 V for LPDDR2
- 1.35 V for DDR3L

The power consumption for the NVCC_DRAM supply is affected by various factors, including the following:

- Amount of activity of the DDR interface
- On-die termination (ODT)—Enabled/disabled, termination value, which is used for the DDR controller and DDR memories
- Board termination for DDR control and address bus
- Configuration of the DDR pads (such as, drive strength)
- Board layout
- Load of the DDR memory devices

NOTE

- Due to the above mentioned reasons, the measurements provided in the following tables would vary from one system to another. The data provided is for guidance only and should not be treated as a specification.
- The measured current on the Freescale SABRE SD Platform also includes the current of the onboard DDR3 memory devices. This board (on which the measurements were taken) includes four DDR3 devices, having a total capacity of 1 GB. For power-optimized systems that use LPDDR2 memories, the power consumed by the DDR I/O and DDR memories would be significantly lower. The SABRE SD Platform utilizes a “T” topology for board memory routing that does not require board-level resistor terminations. This further reduces the DDR I/O power usage.

2.2.1 On-die termination (ODT) settings

On-die termination (ODT) is a feature of the DDR3/DDR3L SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, DQS#, and DM signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

Using weaker ODT settings can greatly reduce the power of the DDR I/O. The required ODT settings are system dependent and may vary among different board designs. These settings should be carefully selected for power optimization while ensuring that JEDEC requirements for the DDR parameters are still met.

Thus, the default settings that are used in the Linux BSP release may need to be modified by the system designer to fit different systems.

Table 1 shows the differences between the test parameters in revisions 0 and 1 of this document.

2.3 Voltage levels and DVFS usage in measurement process

Table 1. Test Parameters—Differences between revision 1 and revision 0[1]

Test Parameters	Rev. 0	Rev. 1
Board used for testing[2]	SABRE SD, rev. B4	SABRE SD, rev. C2
On-die termination (ODT)—memory	120 Ω	120 Ω [3]
ODT—DDR I/O	Disabled	120 Ω [3]

1 ODT values used are indicated in the measurement result tables, Table 3 through Table 13.

2 For more details regarding the differences between the SABRE SD revisions B4 and C2, see the “Revision History” of the i.MX6 SABRE SDP DESIGN FILES, available on the Freescale website at http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=RDIMX6SABREPLAT&fpsp=1&tab=Design_Tools_Tab

3 In revision 1 of this document, the ODT values have been optimized for performance improvement.

The voltage levels of all the supplies, except for VDDARM and VDDSOC, are set to the typical voltage levels as defined in *i.MX 6Solo/6DualLite Applications Processors for Consumer Products* datasheet (IMX6SDLCEC).

The VDDARM and VDDSOC supplies require special explanation. To save power, VDDARM voltage is changed using DVFS (dynamic voltage and frequency scaling), during the run time of the use cases. The voltage levels of these supplies can be changed to standby voltage levels in low-power modes.

2.3.1 VDDARM voltage levels

The target voltage levels for VDDARM can vary according to the DVFS setpoint used, which is selected by the DVFS (also named CPUFREQ) driver. There are several factors that contribute to the setpoint decisions, CPU load being the most important. Other factors are CPU latency requirements, thermal restrictions, and peripheral I/O performance requirements. The voltage and frequency setpoints used for the measurements are given in Table 2.

NOTE

See the “Operating Ranges” table in the *i.MX 6Solo/6DualLite Applications Processors for Consumer Products* datasheet (IMX6SDLCEC) for the official operating points.

Most of the measurements are performed using these voltage levels, and the power data that appears in this document is according to these values. If the measurement is done at different voltage levels, the power consumption scales with the voltage change. In real applications when DVFS is applied, the software, in conjunction with the hardware, automatically adjusts the voltage and frequency values based on the use case requirements.

The voltage used for the power calculation is the average voltage between those setpoints. It depends on the amount of time spent at each setpoint.

2.3.2 VDDSOC voltage levels

The approximate nominal target voltage levels for VDD_SOC_IN is 1.425 V when LDO_SOC is used, and varies according to the VDD_SOC_CAP/VDD_PU_CAP setpoint when LDO_SOC is bypassed. See Table 2 for the VDD_SOC_CAP and VDD_PU_CAP settings used in the measurements. See the "Operating Ranges" table in *i.MX 6Solo/6DualLite Applications Processors for Consumer Products* datasheet (IMX6SDLCEC) for the official operating points.

Table 2. VDDARM, VDDSOC, and VDDPU voltage levels (for reference only)

ARM Frequency	LDO State	VDD_ARM_IN	VDD_ARM_CAP	VDD_SOC_IN	VDD_SOC_CAP/ VDD_PU_CAP
996MHz	Enabled	1.425V	1.25V	1.425V	1.25V
792MHz	Enabled		1.15V		1.175V
396MHz	Enabled		0.95V		1.175V

2.4 Temperature measurements

In some of the use cases, the die temperature is measured. The temperature measurements were taken using the on-chip thermal sensor on a thermally calibrated part. While measuring temperature, it is recommended to wait until the temperature stabilizes.

NOTE

The measured temperatures are for reference only and will vary on different systems, due to differences in board, enclosure, heat spreading techniques, and more. Even when using the same board type, the measured temperature may vary due to factors, such as environment, silicon variations, and measurement error.

For more details on thermal aspects, see the application note *Thermal Management Guidelines for the i.MX 6Dual/6Quad* (AN4579).

2.5 Hardware and software used

The software versions used for the measurements are as follows:

- Gnome rootfs (Linux Release version: L3.0.35_3.0.0), Linux Kernel version: 3.0.35.
- The board used for the measurements is the Freescale SABRE SD Platform.
- The measurements were performed using Agilent 34401A 6 ½ Digit Multimeter.

2.6 Board setup used for power measurements

The power measurements are taken using the default voltages of the supplies.

The default input voltages are as follows:

- VDD_ARM_IN and VDD_SOC_IN at 1.425 V

- VDD_HIGH_IN at 3.0 V
- NVCC_DRAM at 1.5 V

Also, the on-chip LDOs are used, which are the recommended settings for simplified and cost effective system. The ARM voltage scaling is done through configuring LDO_ARM.

Thus, by using a different setup, such as a configurable and separated DC switcher for ARM, the system power may be further optimized by reducing the VDD_ARM_IN input voltage level and may thus achieve the desired operation point. Such a setup would likely result in a higher system cost, so there is a trade-off between cost and system power.

2.7 Measuring points on the Freescale SABRE SD platform

The power data is obtained by measuring the average voltage drop over the measurement points and dividing it by the resistor value to determine the average current. The tolerance of the 0.02-Ω resistors on the SD board is 1%. The measuring points for the various supply domains are as follows:

- VDDSOC—The chip domain current is measured on R21 and the recommended resistance value for this measurement is 0.02 Ω.
- VDDCORE—The ARM domain current is measured on R27 and the recommended resistance value for this measurement is 0.02 Ω.
- VDDHIGH—The VDDHIGH domain current is measured on SH17 and the recommended resistance value for this measurement is 0.1 Ω.
- DDR3 I/O plus Memories—The current in this domain includes the NVCC_DRAM current and the overall current of the onboard DDR3 memory devices. The current in this domain is measured on R25 and the recommended resistance value for this measurement is 0.02 Ω

3 Use cases and measurement results

3.1 Use cases—overview

The main use cases and subtypes, which form the benchmarks for the i.MX 6DualLite internal power measurements on the SABRE SD Platform, are as follows:

- Low power mode (Section 3.2, “Low-power mode use cases”):
  - Deep-Sleep mode (Section 3.2.1, “Use case 1—Deep-Sleep mode (DSM)”)
  - System Idle mode (Section 3.2.2, “Use case 2—System Idle mode”)
  - User Idle mode (Section 3.2.3, “Use case 3—User Idle mode”)
- Audio playback: MP3 Audio Playback (Section 3.3, “Audio playback use case—MP3 Audio Playback”)
- Video Playback (Section 3.4, “Video Playback use cases”):
  - H.264 1080p Video Playback, on HDMI LCD (Section 3.4.1, “Use case 1—H.264 1080p Video Playback, on HDMI LCD”)
  - H.264 1080p Video Playback, on XGA LVDS LCD (Section 3.4.2, “Use case 2—H.264 1080p Video Playback, on XGA LVDS LCD”)
- Dhrystone benchmark (Section 3.5, “Dhrystone benchmark”):
  - Dual-core Dhrystone benchmark (Section 3.5.1, “Use case 1—dual-core Dhrystone benchmark”)
  - Single-core Dhrystone benchmark (Section 3.5.2, “Use case 2—single-core Dhrystone benchmark”)
- Graphics (Section 3.6, “Graphics use cases”)
  - 3D gaming benchmark, MM06 (OpenGL ES 1.1) (Section 3.6.1, “Use case 1— 3D gaming benchmark, MM06”)
  - 3D gaming benchmark, MM07 (OpenGL ES 2.0) (Section 3.6.2, “Use case 2—3D gaming benchmark, MM07”)
- Typical Max Power: Dhrystone, graphics plus 1080p Video Playback (Section 3.7, “Typical max power—Dhrystone, graphics plus 1080p Video Playback
- Non-multimedia: USB-to-eMMC file transfer (Section 3.8, “Non-multimedia use case—USB-to-eMMC file transfer”)

3.2 Low-power mode use cases

3.2.1 Use case 1—Deep-Sleep mode (DSM)

This mode is called either “Dormant mode” or “Suspend-To-RAM” in the Linux BSP. This is the lowest possible power state where external supplies are still on.

The use case is as follows:

- ARM platform is power gated.
- L1 Cache periphery is power gated.
- PU regulator is disabled (means that GPUs and VPU are power gated).
- SoC regulator is bypassed.
- All PLLs (phase locked loop) and CCM (clock controller module) generated clocks are off.
- CKIL (32 kHz) input is on.
- All the modules are disabled.
- Well bias is applied.
- All analog PHYs are powered down.
- External high frequency crystal and on chip oscillator are powered down (by asserting SBYOS bit in CCM).
- VDD_ARM_IN and VDD_SOC_IN are dropped to 0.975 V by asserting the PMIC_STBY_REQ.

In this mode, no current flow is caused by external resistive loads.

Table 3 shows the measurement results when this use case is applied on the i.MX 6DualLite processor.

Table 3. Deep-Sleep mode (DSM) measurement results

Supply Domain	Voltage (V)	Linux 3.0.0 GA		Android—R13.4.1	
		P (mW)	I (mA)	P (mW)	I (mA)
VDD_ARM_IN	0.98	0.098	0.1	0.049	0.05
VDD_SOC_IN	0.988	2.717	2.75	4.199	4.25
VDD_HIGH_IN	2.988	1.101	0.37[1]	7.171	2.4[2]
Total Power (without DDR3 I/O + Memories)	—	**3.916**	—	**11.419**	—
DDR3 I/O + Memories[3]	1.5	21.75	14.5	21.75	14.5
Total Power	—	**25.666**	—	**33.169**	—

1 In case wake-up from USB is enabled, the STOP_MODE_CONFIG bit in Miscellaneous Control Register in CCM should be set, and the VDD_HIGH_IN current would be 1.2 mA. There is no impact on the current of the other power rails mentioned here.

2 In DSM mode, if the USB remote wake-up function is not used, LDO_1P1 can be shut down manually to reduce VDD_HIGH_IN current.

[3] The current in this domain includes the NVCC_DRAM current and I/O and memories current of the on-board DDR3 devices. The current for the i.MX 6DualLiteDDR I/O (NVCC_DRAM supply) can be reduced to nearly zero by floating all DDR pins and maintaining CKE0/1 driven low.

NOTE

For additional details on this use case and settings, see Section 5, "Use case configuration and usage guidelines."

3.2.2 Use case 2—System Idle mode

The use case is as follows:

- ARM is in WFI mode most of the time.
- Some PLLs are on.
- Operating system is on.
- LCD is turned off.
- Screen is not refreshed.

This use cases simulates the situation when the device is left idle for some time and the display is turned off after the timer expires.

Table 4 shows the measurement results when this use case is applied on the i.MX 6DualLite processor.

Table 4. System Idle mode measurement results

Supply Domain	Linux—3.0.0 GA		
	Voltage (V)	P (mW)	I (mA)
VDD_ARM_IN	1.425	9.975	7
VDD_SOC_IN	1.42	43.736	30.8
VDD_HIGH_IN	2.988	97.708	32.7
Total Power (without DDR3 I/O + Memories)	—	**151.419**	—
DDR3 I/O + Memories[1]	1.5	38.25	25.5
Total Power	—	**189.669**	—

[1] The ODT settings are 120 Ω for the memory and 120 Ω for the i.MX 6DualLite DDR I/O.

NOTE

For additional details on this use case and settings, see Section 5, "Use case configuration and usage guidelines."

3.2.3 Use case 3—User Idle mode

The use case is as follows:

- ARM is in WFI mode most of the time.
- Some PLLs are on.
- Operating system and LCD are on, but cores are almost not in operation
- The XGA screen refresh is done by IPU through LVDS.

The use case simulates the situation when the device is left idle and no application is performed on the screen (like reading from the screen).

Table 5 shows the measurement results when this use case is applied on the i.MX 6DualLite processor.

Table 5. User Idle mode measurement results

Supply Domain	Linux—3.0.0 GA			Android—R13.4.1	
	Voltage (V)	P (mW)	I (mA)	P (mW)	I (mA)
VDD_ARM_IN	1.425	11.258	7.9	15.105	10.6
VDD_SOC_IN	1.42	278.32	196	274.415	193.25
VDD_HIGH_IN	2.988	160.904	53.85	184.957	61.9[1]
Total Power (without DDR3 I/O + Memories)	—	**450.482**	—	**474.477**	—
DDR3 I/O +[2] Memories	1.5	116.25	77.5	118.875	79.25
Total Power	—	**566.732**	—	**593.352**[3]	—

1 In User Idle mode, if the USB remote wake-up function is not used, LDO_1P1 can be shut down manually to reduce VDD_HIGH_IN current.
2 The ODT settings are 120 Ω for the memory and 120 Ω for the i.MX 6DualLite DDR I/O.
3 The measured die temperature is 36°C.

NOTE

For additional details on this use case and settings, see Section 5, “Use case configuration and usage guidelines.”

3.3 Audio playback use case—MP3 Audio Playback

The use case procedure is as follows:

1. MP3 (MPEG-1 audio layer 3) decoding is done by ARM.
2. Audio playback is run through SSI (serial synchronous interface).
3. The stream, an mp3 file with bit rate 128 kbps and sampling frequency of 44100 Hz, is taken from the SD (secure digital) card.

The LCD is turned off after the timer expires. The figures are measured when LCD is off.

Table 6 shows the measurement results when this use case is applied on the i.MX 6DualLite processor.

Table 6. MP3 Audio Playback measurement results

Supply Domain	Linux—3.0.0 GA			Android—R13.4.1	
	Voltage (V)	P (mW)	I (mA)	P (mW)	I (mA)
VDD_ARM_IN	1.425	37.62	26.4	33.844	23.75
VDD_SOC_IN	1.42	77.731	54.74	79.094	55.7
VDD_HIGH_IN	2.988	96.811	32.4	161.501	54.05
Total Power (without DDR3 I/O + Memories)	—	**212.162**	—	**274.439**	—
DDR3 I/O +[1] Memories	1.5	63.75	42.5	60.825	40.55
Total Power	—	**275.912**	—	**335.264**[2]	—

[1] The ODT settings are 120 Ω for the memory and 120 Ω for the i.MX 6DualLite DDR I/O.
[2] The measured die temperature is 32°C.

NOTE

For additional details on this use case and settings, see Section 5, “Use case configuration and usage guidelines.”

3.4 Video Playback use cases

3.4.1 Use case 1—H.264 1080p Video Playback, on HDMI LCD

This use case has the following features:

- The video source is H.264, 1080p resolution, 30-fps, 3.6-Mbps bit rate.
- The audio source is AAC, 125-kbps bit rate and 44100-Hz sampling frequency.
- The display is 1080-p resolution using HDMI.

The video/audio stream is loaded from the SD card into the DDR (double data rate) memory and then demuxed by Cortex-A9. The demuxed video signal is decoded by the VPU. It is then taken by the IPU and displayed on the LCD display (through HDMI) with a refresh rate of 60 Hz. In parallel, the demuxed audio signal is decoded using Cortex-A9 and is played back through the SSI.

Table 7 shows the measurement results when this use case is applied on the i.MX 6DualLite processor.

Table 7. 1080P Video Playback measurement results on HDMI LCD

Supply Domain	Linux—3.0.0 GA		
	Voltage (V)	P (mW)	I (mA)
VDD_ARM_IN	1.425	47.88	33.6
VDD_SOC_IN	1.42	484.788	341.4
VDD_HIGH_IN	2.988	239.3388	80.1
Total Power (without DDR3 I/O + Memories)	—	**772.0068**	—
DDR3 I/O +[1] Memories	1.5	504.9	336.6
Total Power	—	**1276.907**	—

[1] The ODT settings are 120 Ω for the memory and 120 Ω for the i.MX 6DualLite DDR I/O.

For additional details on this use case and settings, see Section 5, “Use case configuration and usage guidelines.”

3.4.2 Use case 2—H.264 1080p Video Playback, on XGA LVDS LCD

This use case has the following features:

- The video source is H.264, 1080p resolution, 30-fps, 3.6-Mbps bit rate.
- The audio source is AAC, 125-kbps bit rate and 44100-Hz sampling frequency.
- The display is XGA resolution using LVDS.

The video stream is loaded from the SD card into the DDR (double data rate) memory and then demuxed by Cortex-A9. The demuxed video signal is decoded by the VPU. It is then taken by the IPU and displayed on the LCD display (through LVDS) with a refresh rate of 60 Hz. In parallel, the demuxed audio signal is decoded using Cortex-A9 and is played back through the SSI.

Table 8 shows the measurement results when this use case is applied on the i.MX 6DualLite processor.

Table 8. 1080P Video Playback measurement results on LVDS LCD

Supply Domain	Linux—3.0.0 GA			Android—R13.4.1	
	Voltage (V)	P (mW)	I (mA)	P (mW)	I (mA)
VDD_ARM_IN	1.425	47.025	33	47.95125	33.65
VDD_SOC_IN	1.42	440.484	310.2	440.413	310.15
VDD_HIGH_IN	2.988	168.2244	56.3	186.4512	62.4
Total Power (without DDR3 I/O + Memories)	—	**655.7334**	—	**674.8155**	—
DDR3 I/O +[1] Memories	1.5	504.9	336.6	503.475	335.65
Total Power	—	**1160.633**	—	**1178.29**[2]	—

1 The ODT settings are 120 Ω for the memory and 120 Ω for the i.MX 6DualLite DDR I/O.
2 The measured die temperature is 44°C.

NOTE

For additional details on this use case and settings, see Section 5, “Use case configuration and usage guidelines.”

3.5 Dhrystone benchmark

Dhrystone is a synthetic benchmark used to measure the integer computational performance of processors and compilers. The small size of the Dhrystone benchmark allows it to fit into the L1 cache and thus minimizes accesses to the L2 cache and DDR.

3.5.1 Use case 1—dual-core Dhrystone benchmark

In this use case, the Dhrystone test is performed by two cores. The ARM processor runs the test in a loop at a frequency of 1 GHz.

Table 9 shows the measurement results when this use case is applied on the i.MX 6DualLite processor.

Table 9. Dual-core Dhrystone benchmark measurement results

Supply Domain	Voltage (V)	Linux—3.0.0 GA	
		P (mW)	I (mA)
VDD_ARM_IN	1.425	1201.988	843.5
VDD_SOC_IN	1.42	234.3	165
VDD_HIGH_IN	2.988	106.3728	35.6
Total Power (without DDR3 I/O + Memories)	—	**1542.66**	—
DDR3 I/O + Memories[1]	1.5	39.45	26.3
Total Power	—	**1582.11**[2]	—

1 The ODT settings are 120 Ω for the memory and 120 Ω for the i.MX 6DualLite DDR I/O.
2 The measured die temperature (at 10 minutes) is 48°C.

3.5.2 Use case 2—single-core Dhrystone benchmark

In this use case, the Dhrystone test is performed by a single core. The ARM processor runs the test in a loop at a frequency of 1 GHz. The other core is idle. Run power of ARM is measured.

Table 10 shows the measurement results when this use case is applied on the i.MX 6DualLite processor.

Table 10. Single-core Dhrystone benchmark measurement results

Supply Domain	Voltage (V)	Linux- 3.0.0 GA	
		P (mW)	I (mA)
VDD_ARM_IN	1.425	658.065	461.8
VDD_SOC_IN	1.42	225.922	159.1
VDD_HIGH_IN	2.988	104.8788	35.1
Total Power (without DDR3 I/O + Memories)	—	**988.8658**	—
DDR3 I/O + Memories[1]	1.5	39.45	26.3
Total Power	—	**1028.316[2]**	—

1 The ODT settings are 120 Ω for the memory and 120 Ω for the i.MX 6DualLite DDR I/O.
2 The measured die temperature (10 minutes) is 38°C.

3.6 Graphics use cases

3.6.1 Use case 1— 3D gaming benchmark, MM06

This use case has the following features:

- VGA resolution, using MM06 (Samurai) benchmark.
- The frame rate is 161.52 fps.
- The display is of XGA resolution using LVDS

The graphics are loaded from the SD card into the DDR (double data rate) memory, processed by the GPU3D, then copied to the display buffer in the DDR. They are then processed by the IPU and displayed on the LCD display (through LVDS) with a refresh rate of 60 Hz.

Table 11 shows the measurement results when this use case is applied on the i.MX 6DualLite processor. In this case, measurements were taken with DVFS disabled and CPU speed set to 396 MHz.

Table 11. 3D gaming MM06 benchmark measurement results—DVFS disabled

Supply Domain	Linux—3.0.0 GA		
	Voltage (V)	P (mW)	I (mA)
VDD_ARM_IN	1.425	216.9563	152.25
VDD_SOC_IN	1.42	803.152	565.6
VDD_HIGH_IN	2.988	173.6028	58.1
Total Power (without DDR3 I/O + Memories)	—	**1193.711**	—
DDR3 I/O +[1] Memories	1.5	848.25	565.5
Total Power	—	**2041.961**	—

[1] The ODT settings are 120 Ω for the memory and 120 Ω for the i.MX 6DualLite DDR I/O.

NOTE

For additional details on this use case and settings, see Section 5, “Use case configuration and usage guidelines.”

3.6.2 Use case 2—3D gaming benchmark, MM07

This use case has the following features:

- VGA resolution, using MM07 (Taiji) benchmark.
- The frame rate is 15.242 fps
- The display is of XGA resolution using LVDS

The graphics are loaded from the SD card into the DDR (double data rate) memory, processed by the GPU3D, then copied to display buffer in the DDR. It is then taken by IPU and displayed on the LCD display (through LVDS) with a refresh rate of 60 Hz.

In this use case, measurements were taken with DVFS disabled and CPU speed set to 396 MHz.

Table 12. 3D gaming MM07 benchmark measurement results—DVFS disabled

Supply Domain	Linux—3.0.0 GA		
	Voltage (V)	P (mW)	I (mA)
VDD_ARM_IN	1.425	153.1875	107.5
VDD_SOC_IN	1.42	759.7	535
VDD_HIGH_IN	2.988	167.7762	56.15
Total Power (without DDR3 I/O + Memories)	—	**1080.664**	—
DDR3 I/O +[1] Memories	1.5	395.1	263.4
Total Power	—	**1475.764**	—

[1] The ODT settings are 120 Ω for the memory and 120 Ω for the i.MX 6DualLite DDR I/O.

NOTE

For additional details on this use case and settings, see Section 5, “Use case configuration and usage guidelines.”

3.7 Typical max power—Dhrystone, graphics plus 1080p Video Playback

The purpose of this use case is to provide the power consumption of a very intensive use case, which is highly atypical, but perhaps could be relevant for some systems when planning to work under extreme conditions.

This use case is running concurrently on two displays:

- One 1080p Video Playback, through HDMI.
- 3D graphics through LVDS port with XGA resolution.

This use case has the following features:

- The video source is H.264, 1080p resolution, 30-fps, 3.6-Mbps bit rate.
- The audio source is AAC, 125-kbps bit rate and 44100-Hz sampling frequency.
- The graphics are 3D gaming benchmark—MM06.
- Both ARM cores are heavily loaded.
- Maximum frequencies are used for ARM, IPU, VPU, GPUs, and DDR clocks.

The video stream is loaded from the SD card into the DDR memory. The video input is decoded by the VPU (but not displayed on the screen). In addition, one Cortex-A9 core is used to perform concurrent software decoding of the input audio stream. VPU decoding is done here in as a background activity to consume power.

The decoded stream is then taken by IPU and displayed on the LCD displays (through HDMI) with a refresh rate of 60 Hz. The GPU3D is used to render the graphics. Then, the graphics are displayed by the IPU through LVDS on XGA display. The other core is running Dhrystone pattern in a loop in the background. Table 13 shows the typical maximum power measurement results on the SABRE SD Platform.

Table 13. Typical max power measurement results on SABRE SD platform

Supply Domain	Linux—3.0.0 GA[1]		
	Voltage (V)	P (mW)	I (mA)
VDD_ARM_IN	1.425	982.2525 (1145.13 max.)	689.3 (803.6 max[2])
VDD_SOC_IN	1.42	1161.702 (1246.76 max.)	818.1 (878 max)
VDD_HIGH_IN	2.988	248.004 (248.9004 max.)	83 (83.3 max)
Total Power (without DDR3 I/O + Memories)	—	**2391.9585 (2640.7904 max.)**	—
DDR3 I/O +[3] Memories	1.5	1063.05 (1114.95 max.)	708.7 (743.3 max)
Total Power	—	**3455.0085 (3755.7404 max)**	—

1 The current also depends on the silicon temperature, which depends on the heat dissipation in the system. The measured die temperature for this use case is approximately 80°C.

2 This is a maximum current measured over a small period of time to present the sustained peak current for the supply in this measurement. Still, there would be variations from part to part under different PVT conditions.

[3] The ODT (On Die Termination) that was used for measurements is 120 Ω for the memory and 120 Ω for the i.MX 6DualLiteDDR IO. The DDR IO power may be further reduced by using optimized ODT settings of the i.MX 6DualLite DDR IO and the DDR memory IO. Optimization needs to be done per system.

3.8 Non-multimedia use case—USB-to-eMMC file transfer

In this use case, 1 GB total of data is transferred from a USB device to an eMMC device. A data size of 1 MB is copied each time, repeatedly, 1000 times. The SDMA is used to perform the data transfer to the eMMC host controller. Table 14 shows the transfer measurement results.

Table 14. USB-to-eMMC file transfer measurement results

Supply Domain	Voltage (V)	Linux—3.0.0 GA	
		P (mW)	I (mA)
VDD_ARM_IN	1.425	33.345	23.4
VDD_SOC_IN	1.42	274.06	193
VDD_HIGH_IN	2.988	131.1732	43.9
Total Power (without DDR3 I/O + Memories)	**—**	**438.5782**	**—**
DDR3 I/O + Memories	1.5	224.7	149.8
Total Power	**—**	**663.2782**	**—**

4 Reducing power consumption

The overall system power consumption depends on both software optimization and how the system hardware is implemented. Below is a list of suggestions that may help reduce system power. Some of these are already implemented in Linux BSP. Further optimizations can be done on the individual customer's system.

NOTE

Further power optimizations are planned for future BSP releases. See the Freescale website to obtain the latest BSP release.

- Apply clock gating whenever clocks or modules are not used, by configuring CCGR registers in the CCM (Clock Controller Module).
- Reduce the number of operating PLLs—Applicable mainly in Audio Playback mode or Idle modes.
- Core DVFS and system bus scaling—Applying DVFS for ARM and scaling the frequencies of the AXI, AHB, and IPG bus clocks can significantly reduce the power consumption of the VDDARM and VDDSOC domains. However, due to the reduced operation frequency, the accesses to the DDR take longer, which increases the power consumption of the DDR I/O and memories. This trade-off needs to be taken into account for each mode, to quantify the overall affect on system power.
- Put i.MX 6DualLite into low power modes (WAIT, STOP) whenever possible. See Chapter 18, "Clock Controller Module (CCM)," of the *i.MX 6Solo/6DualLite Applications Processor Reference Manual* (IMX6SDLRM) for details.
- DDR interface optimization:
  - Use careful board routing of the DDR memories, maintaining PCB trace lengths as short as possible.
  - Use a reduced ODT (On-Die Termination) setting, as possible. The termination used greatly influences the power consumption of the DDR interface pins.
  - Use the proper output driver impedance for DDR interface pins that provides good impedance matching. Select the lowest possible drive strength that provides the required performance, in order to save current through DDR I/O pins.
  - Carefully choose onboard resistors so the least amount of current is wasted—for example, when selecting impedance matching resistors between CLK and CLK_B (when using DDR3 memories).
  - When possible, in lower performance use cases, switching to DLL Off mode allows for greatly reducing DDR frequency. This disables or reduces termination, and it reduces the drive strength. Thus, power consumption of the DDR interface pins could be significantly reduced.
  - Float i.MX 6DualLite DDR interface pins (set to high Z) when DDR memory is in Self-Refresh mode, and keep DDR_SDCKE0 and DDR_SDCKE1 at low value. If DDR_SDCKE0 and DDR_SDCKE1 are kept at low value by using external pull-down, make sure there is no onboard termination on these pins during this mode.
  - If possible (depending on system stability), configure DDR input pins to CMOS mode, instead of Differential mode. This can be done by clearing the DDR_INPUT bit in the corresponding

registers in IOMUXC. This setting is mostly recommended when operating at low frequencies, such as in DLL Off mode.

— Use of DDR3L memory devices, operating at low I/O voltage, can further reduce the I/O power by 20%.

— Use of DDR memory offerings in the latest process technology can significantly reduce the power consumption of the DDR devices and the DDR I/O.

The various steps involved in floating the i.MX 6DualLite DDR interface pins are given below.

NOTE

All the above programming steps are performed when the code is running from the internal RAM rather than from the DDR memory. The code is non-cacheable.

Steps to be performed before entering Suspend (Deep-Sleep mode):

1. Read the power saving status in MMDC in the MAPSR register, because automatic power saving is enabled, to make sure that DDR is in Self-Refresh.
2. Do the following:
   a) In case there is no onboard termination for DDR control and address bus, set the DSE (drive strength selection, in IOMUXC) for all DDR IF I/O to 0 (High Z), except for CKE0 and CKE1.
   b) In case DDR control and address bus have onboard termination resistors connected to VTT, such as in the case where SODIMM is used:
   — Option 1
      – As for (a), keep SDCKE0/1 active, this causes some extra current from the pins sharing the same DSE control in IOMUXC_SW_PAD_CTL_GRP_CTLDS register. The pins are DRAM_CS0, DRAM_CS1, DRAM_SDBA2, DRAM_SDCKE0, DRAM_SDCKE1, and DRAM_SDWE.
   — Option 2 (requires onboard pull down resistor on DRARM_SDCKE0/1 pins)
      – Set the supply of the termination resistor to be floated (can be done through some pins with GPIO capability on it).
      – Set the DSE (drive strength selection, in IOMUXC) for all DDR IF I/O to 0 (High Z).
3. Go into the Suspend mode.

Steps to be performed after exiting Suspend:

1. Restore all the settings for the DDR I/O to the required value.
2. System proceeds to Run mode.

NOTE

If the system can ensure there are no masters accessing the DDR, the following may be applied to other scenarios besides Deep-Sleep mode: DDR pins can be floated in the same manner, even when Suspend is not entered, and DDR can be manually put into Self-Refresh to save power. This happens when the CPU is not running, or it is running from the internal RAM.

5 Use case configuration and usage guidelines

5.1 HDMI 1080P playback

5.1.1 HDMI 1080P playback—clock configuration

Clock configuration in Table 15 is aligned with release 3.0.0 GA.

Table 15. HDMI 1080P playback clock configuration

Clock Name	Frequency (MHz)
AXI	270
AHB	132
CPU	396
GPU2D	off
GPU3D Core	off
GPU3D Shader	off
VPU	270
IPU1	270
MMDC CH0	396
MMDC CH1	off

5.1.2 HDMI 1080P playback—PLL configuration

PLL configuration in Table 16 is aligned with release 3.0.0 GA.

Table 16. HDMI 1080P playback PLL configuration

PLL Name	Frequency (MHz)
PLL1—System PLL	396
PLL2—System Bus PLL	528
pll2 396m pfd	396
pll2 352m pfd	off
pll2 594m pfd	off
PLL3—OTG USB PLL	480
pll3 508m pfd	508
pll3 454m pfd	off
pll3 720m Pfd	off
pll3 540m pfd	540
PLL4—Audio PLL	176

Table 16. HDMI 1080P playback PLL configuration (continued)

PLL Name	Frequency (MHz)
PLL5—Video PLL	297
PLL6—ENET PLL	off
PLL7—Host USB PLL	off
PLL8—MLB PLL	off

5.1.3 HDMI 1080P playback—system setup

1. Disconnect LVDS.
2. Input video used for measuring is
   `Avatar_1920x1080_30fpsH264_2x44100AAC_3.6Mbps_246sec.mp4.`

5.1.4 HDMI 1080P playback—steps

1. Power on the board and in the serial console press any key to stop autoboot.
2. `setenv bootargs 'console=ttymxc0,115200 vmalloc=256M'`
3. `setenv bootargs_base 'bootargs ${bootargs} fec_mac=${ethaddr} ${hdmi_mode}'`
4. `setenv hdmi_mode 'video=mxcfb0:dev=hdmi,1920x1080M@60,if=RGB24'`
5. `saveenv`
6. Restart the board.
7. Run the script below to set the system into right work point.

```
#!/bin/sh
echo 1 > /sys/class/graphics/fb0/blank
echo 1 > /sys/class/graphics/fb1/blank
echo 1 > /sys/class/graphics/fb2/blank
echo 1 > /sys/class/graphics/fb3/blank
echo 1 > /sys/class/graphics/fb4/blank
ifconfig eth0 down
echo userspace > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
echo 396000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
echo 0 > /sys/class/graphics/fb0/blank
```

8. Run `gplay <path to your video>`
9. Use case is running, measurements can be taken now.

5.2 Deep-Sleep mode

In this use case all clocks and PLLs are turned off except 32 kHz clock which is for system wake up.

1. `echo mem > /sys/power/state`

2. Use case is running, measurements can be taken now.

5.3 User Idle mode

5.3.1 User Idle mode—clock configuration

Clock configuration in Table 17 is aligned with release 3.0.0 GA.

Table 17. User Idle mode clock configuration

Clock Name	Frequency (MHz)
AXI	270
AHB	132
CPU	396
GPU2D	off
GPU3D Core	off
GPU3D Shader	off
VPU	off
IPU1	270
MMDC CH0	396
MMDC CH1	off

5.3.2 User Idle mode—PLL configuration

PLL configuration in Table 18 is aligned with release 3.0.0 GA.

Table 18. User Idle mode PLL configuration

PLL Name	Frequency (MHz)
PLL1—System PLL	396
PLL2—System Bus PLL	528
pll2 396m pfd	396
pll2 352m pfd	452
pll2 594m pfd	off
PLL3—OTG USB PLL	480
pll3 508m pfd	off
pll3 454m pfd	off
pll3 720m pfd	off
pll3 540m pfd	540
PLL4—Audio PLL	off

Table 18. User Idle mode PLL configuration (continued)

PLL Name	Frequency (MHz)
PLL5—Video PLL	off
PLL6—ENET PLL	off
PLL7—Host USB PLL	off
PLL8—MLB PLL	off

5.3.3 User Idle mode—system setup

Disconnect everything except the SD and LVDS, using the following procedure.

1. Power on the board and in the serial console press any key to stop autoboot
2. `setenv bootargs_base 'setenv bootargs ${bootargs} fec_mac=${ethaddr} ${lvds_mode}'`
3. `savenv`
4. Run:

```
// blank display
echo 1 > /sys/class/graphics/fb1/blank
echo 1 > /sys/class/graphics/fb2/blank
echo 1 > /sys/class/graphics/fb3/blank
echo 1 > /sys/class/graphics/fb4/blank
// stop the fec
ifconfig eth0 down
echo 0 > /sys/class/graphics/fb0/blank
//enable bus freq adjustment
```

5. Use case is running, measurements can be taken now.

5.4 System Idle mode

5.4.1 System Idle mode—clock configuration

Clock configuration in Table 19 is aligned with release 3.0.0 GA.

Table 19. System Idle mode clock configuration

Clock Name	Frequency (MHz)
AXI	270
AHB	132
CPU	396
GPU2D	off
GPU3D Core	off

Table 19. System Idle mode clock configuration (continued)

Clock Name	Frequency (MHz)
GPU3D Shader	off
VPU	off
IPU1	off
MMDC CH0	24
MMDC CH1	off

5.4.2 System Idle mode—PLL configuration

PLL configuration in Table 20 is aligned with release 3.0.0 GA.

Table 20. System Idle mode PLL configuration

PLL Name	Frequency (MHz)
PLL1—System PLL	396
PLL2—System Bus PLL	528
pll2 396m pfd	396
pll2 352m pfd	off
pll2 594m pfd	off
PLL3—OTG USB PLL	480
pll3 508m pfd	off
pll3 454m pfd	off
pll3 720m pfd	off
pll3 540m pfd	540
PLL4—Audio PLL	off
PLL5—Video PLL	off
PLL6—ENET PLL	off
PLL7—Host USB PLL	off
PLL8—MLB PLL	off

5.4.3 System Idle mode—system setup

Disconnect everything except the SD and LVDS.

1. //disable DVFS
   - `echo userspace > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor`
2. //set cpu freq at 396M
   - `echo 396000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed`
3. Run the script `/uart_off.sh` (see below).

```
echo 1 > /sys/class/graphics/fb0/blank
echo 1 > /sys/class/graphics/fb1/blank
echo 1 > /sys/class/graphics/fb2/blank
echo 1 > /sys/class/graphics/fb3/blank
echo 1 > /sys/class/graphics/fb4/blank
```

4. Use case is running, measurements can be taken now.

```
uart_off.sh:
        echo "disabling UART"
        /unit_tests/memtool 0x20c407c=0x1

        sleep 5
        /unit_tests/memtool 0x20c8010=0x80010000
        sleep 300
        /unit_tests/memtool 0x20c8010=0x80003000

        sleep 2
        /unit_tests/memtool 0x20c407c=0xf000001
        echo "uart is back ON"
```

5.5 Audio playback

5.5.1 Audio playback—clock configuration

Clock configuration in Table 21 is aligned with release 3.0.0 GA.

Table 21. Audio playback clock configuration

Clock Name	Frequency (MHz)
AXI	270
AHB	132
CPU	396
GPU2D	off
GPU3D Core	off
GPU3D Shader	off
VPU	off
IPU1	off
MMDC CH0	396
MMDC CH1	off

5.5.2 Audio playback—PLL configuration

PLL configuration in Table 22 is aligned with release 3.0.0 GA.

Table 22. Audio playback PLL configuration

PLL Name	Frequency (MHz)
PLL1—System PLL	396
PLL2—System Bus PLL	528
pll2 396m pfd	396
pll2 352m pfd	off
pll2 594m pfd	off
PLL3—OTG USB PLL	480
pll3 508m pfd	508
pll3 454m pfd	off
pll3 720m pfd	off
pll3 540m pfd	540
PLL4—Audio PLL	176
PLL5—Video PLL	off
PLL6—ENET PLL	off
PLL7—Host USB PLL	off
PLL8—MLB PLL	off

5.5.3 Audio playback—system setup

- SD boot
- Connect XGA LVDS panel

1. Add `enable_wait_mode=on` in kernel command line
2. Boot system to SD rootfs with LVDS, run below to enable busfreq scaling

```
#!/bin/sh
echo 1 > /sys/class/graphics/fb0/blank
echo 1 > /sys/class/graphics/fb1/blank
echo 1 > /sys/class/graphics/fb2/blank
echo 1 > /sys/class/graphics/fb3/blank
ifconfig eth0 down
```

If it doesn't run into low busfreq automatically, run:

```
echo 1 > /sys/devices/platform/imx_busfreq.0/enable
echo userspace > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
echo 996000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
echo 396000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
```

```
echo interactive > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
```

3. `gplay 128kbps_44khz_s_mp3.mp3`
4. Measure SoC and ARM data, and record
5. Get the DVFS status before and after with:

```
cat /sys/devices/system/cpu/cpu0/cpufreq/stats/time_in_state
```

5.6 XGA LVDS 1080p playback

5.6.1 XGA LVDS 1080p playback—clock configuration

Clock configuration in Table 23 is aligned with release 3.0.0 GA.

Table 23. XGA LVDS 1080p playback clock configuration

Clock Name	Frequency (MHz)
AXI	270
AHB	132
CPU	396
GPU2D	off
GPU3D Core	off
GPU3D Shader	off
VPU	270
IPU1	270
MMDC CH0	396
MMDC CH1	off

5.6.2 XGA LVDS 1080p playback—PLL configuration

PLL configuration in Table 24 is aligned with release 3.0.0 GA.

Table 24. XGA LVDS 1080p playback PLL configuration

PLL Name	Frequency (MHz)
PLL1—System PLL	396
PLL2—System Bus PLL	528
pll2 396m pfd	396
pll2 352m pfd	452
pll2 594m pfd	off
PLL3—OTG USB PLL	480
pll3 508m pfd	508
pll3 454m pfd	off

Table 24. XGA LVDS 1080p playback PLL configuration (continued)

PLL Name	Frequency (MHz)
pll3 720m pfd	off
pll3 540m pfd	540
PLL4—Audio PLL	176
PLL5—Video PLL	645
PLL6—ENET PLL	off
PLL7—Host USB PLL	off
PLL8—MLB PLL	off

5.6.3 XGA LVDS 1080p playback—system setup

- SD boot
- Connect XGA LVDS panel

5.6.4 XGA LVDS 1080p playback—steps

1. Boot board and run below scripts

```
#!/bin/sh
echo 1 > /sys/class/graphics/fb0/blank
echo 1 > /sys/class/graphics/fb1/blank
echo 1 > /sys/class/graphics/fb2/blank
echo 1 > /sys/class/graphics/fb3/blank
echo 1 > /sys/class/graphics/fb4/blank
ifconfig eth0 down
echo userspace > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
echo 396000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
```

2. Run: `gplay <path to your video>`
3. Measure the power and record result
4. Dump clock before and after and during playback (only once), and record them `./clocks.sh`
5. Enable SW DVFS and remeasure the power
6. `echo interactive > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor`
7. Get the DVFS status before and after with

```
cat /sys/devices/system/cpu/cpu0/cpufreq/stats/time_in_state
```

5.7 3D gaming

5.7.1 3D gaming—clock configuration

Clock configuration in Table 25 is aligned with release 3.0.0 GA.

Table 25. 3D gaming clock configuration—CPU frequency at 396 MHz

Clock Name	Frequency (MHz)
AXI	270
AHB	132
CPU	396
GPU2D	off
GPU3D Core	528
GPU3D Shader	528
VPU	off
IPU1	off@MM06, 270@MM07
MMDC CH0	396
MMDC CH1	off

5.7.2 3D gaming—PLL configuration

PLL configuration in Table 26 is aligned with release 3.0.0 GA.

Table 26. 3D gaming PLL Configuration—CPU frequency at 396 MHz

PLL Name	Frequency (MHz)
PLL1—System PLL	396
PLL2—System Bus PLL	528
pll2 396m pfd	396
pll2 352m pfd	off@MM06, 452@MM07
pll2 594m pfd	528
PLL3—OTG USB PLL	480
pll3 508m pfd	off
pll3 454m pfd	off
pll3 720m pfd	off
pll3 540m pfd	540
PLL4—Audio PLL	off
PLL5—Video PLL	off
PLL6—ENET PLL	off

Table 26. 3D gaming PLL Configuration—CPU frequency at 396 MHz (continued)

PLL Name	Frequency (MHz)
PLL7—Host USB PLL	off
PLL8—MLB PLL	off

5.7.3 3D gaming—system setup

- SD boot
- Connect XGA LVDS panel

5.7.4 3D gaming—steps

1. Add `enable_wait_mode=on` to kernel command line
2. Boot board to SD rootfs, disable Ethernet (`ifconfig eth0 down`), connect to XGA LVDS dispaly.
3. Run script, below, to measure at 400M:

```
#!/bin/sh
echo 1 > /sys/class/graphics/fb1/blank
echo 1 > /sys/class/graphics/fb2/blank
echo 1 > /sys/class/graphics/fb3/blank
ifconfig eth0 down
echo 1 > /sys/devices/platform/imx_busfreq.0/enable
echo userspace > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
echo 396000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
echo 0 > /sys/class/graphics/fb0/blank
```

4. Run 3Dmark_es11 applicaiton, you can copy it from `10.192.225.222/rootfs/wb/utils/Graphics/imx61_rootfs/test/3DMarkMobile`
5. Test samurai record the fps and with mmdc program to get bus loading
6. Measure the power and record result
7. Enable SW DVFS and remeasure the power
8. `echo interactive > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor`
9. Get the DVFS status before and after with:

```
cat /sys/devices/system/cpu/cpu0/cpufreq/stats/time_in_state
```

10. Run script, below, to test 1G

```
#!/bin/sh
echo 1 > /sys/class/graphics/fb1/blank
echo 1 > /sys/class/graphics/fb2/blank
echo 1 > /sys/class/graphics/fb3/blank
ifconfig eth0 down
echo 1 > /sys/devices/platform/imx_busfreq.0/enable
echo performance > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
```

```
echo 0 > /sys/class/graphics/fb0/blank
```

5.8 Dhrystone

5.8.1 Dhrystone—clock configuration

Clocks configuration in Table 27 is aligned with release 3.0.0 GA.

Table 27. Dhrystone clock configuration

Clock Name	Frequency (MHz)
AXI	270
AHB	132
CPU	996
GPU2D	off
GPU3D Core	off
GPU3D Shader	off
VPU	off
IPU1	off
MMDC CH0	396
MMDC CH1	396

5.8.2 Dhrystone—PLL configuration

PLL configuration in Table 28 is aligned with release 3.0.0 GA.

Table 28. Dhrystone PLL configuration

PLL Name	Frequency (MHz)
PLL1—System PLL	996
PLL2—System Bus PLL	528
pll2 396m pfd	396
pll2 352m pfd	off
pll2 594m pfd	off
PLL3—OTG USB PLL	480
pll3 508m pfd	off
pll3 454m pfd	off
pll3 720m pfd	off
pll3 540m pfd	540
PLL4—Audio PLL	off

Table 28. Dhrystone PLL configuration (continued)

PLL Name	Frequency (MHz)
PLL5—Video PLL	off
PLL6—ENET PLL	off
PLL7—Host USB PLL	off
PLL8—MLB PLL	off

5.8.3 Dhrystone—system setup

- SD boot
- Connect XGA LVDS panel

5.8.4 Dhrystone—steps

1. Boot board to SD rootfs
2. Run scripts below to set system:

```
#!/bin/sh
echo 1 > /sys/class/graphics/fb0/blank
echo 1 > /sys/class/graphics/fb1/blank
echo 1 > /sys/class/graphics/fb2/blank
echo 1 > /sys/class/graphics/fb3/blank
echo 1 > /sys/class/graphics/fb4/blank
ifconfig eth0 down
echo 1 > /sys/devices/platform/imx_busfreq.0/enable
```

3. Run dry2 1 instance, and measure

```
while true; do dry2 ; done
```

4. Run dry2 2 instance, and measure

```
while true; do dry2 & dry2; done
```

5. Measure die temperature by:

```
cat /sys/class/thermal/thermal_zone0/temp
```

5.9 Max power

5.9.1 Max power—clock configuration

Clock configuration in Table 29 is aligned with release 3.0.0 GA.

Table 29. Max power clock configuration

Clock Name	Frequency (MHz)
AXI	270
AHB	132
CPU	996
GPU2D	off
GPU3D Core	528
GPU3D Shader	528
VPU	270
IPU1	270
MMDC CH0	396
MMDC CH1	396

5.9.2 Max power—PLL configuration

PLL configuration in Table 30 is aligned with release 3.0.0 GA.

Table 30. Max power PLL configuration

PLL Name	Frequency (MHz)
PLL1—System PLL	996
PLL2—System Bus PLL	528
pll2 396m pfd	396
pll2 352m pfd	452
pll2 594m pfd	528
PLL3—OTG USB PLL	480
pll3 508m pfd	508
pll3 454m pfd	off
pll3 720m pfd	off
pll3 540m pfd	540
PLL4—Audio PLL	176
PLL5—Video PLL	645
PLL6—ENET PLL	off

Table 30. Max power PLL configuration (continued)

PLL Name	Frequency (MHz)
PLL7—Host USB PLL	off
PLL8—MLB PLL	off

5.9.3 Max power—system setup

- SD boot
- Connect HDMI daughter card, and XGA LVDS panel
- Connect TV to each HDMI interface

5.9.4 Max power—steps

1. Edit uboot cmdline bootargs to include dual display configuration:

```
video=mxcfb1:dev=ldb,LDB-XGA,if=RGB666 video=mxcfb0:dev=hdmi,1920x1080M@60,if=RGB24
ldb=sep0
```

2. Run drystone:

```
while true; do dry2; done &
```

3. Run Graphics GPU3D on LVDS

```
echo 0 > /sys/class/graphics/fb2/blank
modprobe galcore
export FB_FRAMEBUFFER_0="/dev/fb2"
cd 3DMarkMobile/fsl_imx_linux
fm_oes_player &
```

4. Run 1080p video on HDMI

```
gplay Avatar_1920x1080_30fpsH264_2x44100AAC_3.6Mbps_246sec.mp4
```

5. Record two groups data from DMM: **average** and **max** value.

5.10 Important commands

In Uboot Console

- `printenv` – display environment variables.
- `setenv` – update environment variables.
  - setenv <name> <value> ...
    - Set environment variable 'name' to 'value ...'
  - `setenv <name>`
    - Delete environment variable 'name'
- `saveenv` – save updates to environment variables.
- `bootargs` – pass to the kernel, which are called kernel command lines.

In Linux Console

- `cat /proc/cmdline`—displays command line

- `cat /sys/devices/virtual/thermal/thermal_zone0/temp`—print temperature to screen (chip should be calibrated)
- In order to print to screen clock configuration, use the `clocks.sh` script

clocks.sh

```
#!/bin/bash

saved_path=$PWD

if ! mount|grep -sq '/sys/kernel/debug'; then
    mount -t debugfs none /sys/kernel/debug
fi

printf "%-24s %-20s %3s %9s\n" "clock" "parent" "use" "flags" "rate"

for foo in $(find /sys/kernel/debug/clock -type d); do
    if [ "$foo" = '/sys/kernel/debug/clock' ]; then
        continue
    fi

    cd $foo

    ec="$(cat usecount)"
    rate="$(cat rate)"
    flag="$(cat flags)"

    clk="$(basename $foo)"
    cd ..
    parent="$(basename $PWD)"

    if [ "$parent" = 'clock' ]; then
    parent="   ---"
    fi

    printf "%-24s %-24s %2d %2d %10d\n" "$clk" "$parent" "$ec" "$flag" "$rate"
    cd $saved_path
done
```

6 Revision history

Table 31 provides a revision history for this application note.

Table 31. Document revision history

Rev. Number	Date	Substantive Change(s)
Rev. 1	2/2013	• Throughout: – For Rev.0 of this document, the board used for testing was the SABRE SD, revision B4; for Rev.1 of this document, the board used for testing was the SABRE SD, revision C2. For more details regarding the differences between the SABRE SD revisions B4 and C2, see the “Revision History” of the i.MX6 SABRE SDP DESIGN FILES (available on the Freescale website at http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=RDIMX6SABREPLAT&fpsp=1&tab=Design_Tools_Tab). – The ODT (on-die termination) was used for measurements on Rev. 0 of this document is 120 Ω for the memory; for the i.MX 6DualLite DDR I/O, the ODT is disabled. – The ODT values have been optimized for performance improvement. The measurements were taken using 120 Ω for the memory and 120 Ω for the i.MX 6DualLite DDR I/O. The ODT values used are indicated in the measurements result tables listed below. – Aligned content to 3.0.0 GA. • Updated the following tables: – Table 2, “VDDARM, VDDSOC, and VDDPU voltage levels (for reference only)” – Table 3, “Deep-Sleep mode (DSM) measurement results” – Table 4, “System Idle mode measurement results” – Table 5, “User Idle mode measurement results” – Table 6, “MP3 Audio Playback measurement results” – Table 7, “1080P Video Playback measurement results on HDMI LCD” – Table 8, “1080P Video Playback measurement results on LVDS LCD” – Table 9, “Dual-core Dhrystone benchmark measurement results” – Table 10, “Single-core Dhrystone benchmark measurement results” – Table 11, “3D gaming MM06 benchmark measurement results—DVFS disabled” – Table 12, “3D gaming MM07 benchmark measurement results—DVFS disabled” • Removed 3D gaming MM06 and MM07 benchmark measurement results with DVFS enabled; plan to update in future release of this document. • Section 2.2.1, “On-die termination (ODT) settings”: Updated “Note.” • Section 2.6, “Board setup used for power measurements”: Updated VDD_HIGH_IN from 2.8 to 3.0 V. • Section 3.4.1, “Use case 1—H.264 1080p Video Playback, on HDMI LCD” and Section 3.4.2, “Use case 2—H.264 1080p Video Playback, on XGA LVDS LCD”: Updated features lists to note that reduction of the DDR bus load by the VDOA module is on Linux platform only. • Section 3.6.1, “Use case 1— 3D gaming benchmark, MM06: Updated DVFS-disabled frame rate from 166.4 to 161.52 fps, and DVFS-enabled frame rate from 198.07 to 221.18 fps. • Section 3.6.2, “Use case 2—3D gaming benchmark, MM07: Updated DVFS-disabled frame rate from 15.203 to 15.242 fps, and DVFS-enabled frame rate from 15.295 to 15.673 fps. • Added use case: Section 3.8, “Non-multimedia use case—USB-to-eMMC file transfer.” • Section 5.8.4, “Dhrystone—steps”: Updated scripts. • Section 5.9.4, “Max power—steps”: Corrected step 4; removed ‘&’ at end of line.
Rev. 0	11/2012	Initial public release.

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: AN4576
Rev. 1
3/2013