AN5384

Implementation of IEEE Standard 1149.6™ on QorIQ LS1088A Processor

Rev. 0 — 19 May 2022

Application Note

Contents

1 Introduction

This document describes how to implement the IEEE standard 1149.6™ on NXPs QorIQ LS1088A processor.

The IEEE standard 1149.6 fully complies with the existing IEEE standard 1149.1. Still, it also requires the following new and mandatory public JTAG instructions that are supported by the NXPs SerDes implementation on the LS1088A processor:

- EXTEST_PULSE
- EXTEST_TRAIN

To provide an implementation of the IEEE standard 1149.6, NXP offers an additional custom public JTAG instruction, INIT_SETUP.

The INIT_SETUP instruction is similar, but not identical to the INITIALIZE instruction described in the *IEEE standard 1149.6, Annex E*. Although, here the references are made to the two of the IEEE 1149.6 mandatory instructions, EXTEST_PULSE and EXTEST_TRAIN. But, the primary focus is on the INIT_SETUP instruction.

On the LS1088A, the pins listed in Table 7 are defined as IEEE 1149.6 advanced I/O pins. All other I/O pins are defined as standard I/O and comply only with IEEE 1149.1.

NOTE

This document is not intended to serve as an introduction to IEEE 1149.6 or its motivations. For a thorough description of testing AC coupled differential nets, see *1149.6™-2003, IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks*.

When USB is not in use and all USB power supplies connect to GND, the JTAG IEEE Std 1149.6 Boundary Scan Register (BSR) does not shift data between TDI and TDO. To shift USB BSR cells, power on the USB_SVDD. Here, the USB boundary cells cannot observe or control USB pins, affecting the USB BSR cells during EXTEST, EXTEST_PULSE, EXTEST_TRAIN, CLAMP, and SAMPLE. The only fails are related to USB IOs when USB_SVDD is powered on and USB_SDVDD and USB_HVDD are powered off. If all USB power supplies connect to GND, the other 1149.1 JTAG or DAP debug instructions still operate.

2 Mandatory IEEE 1149.6 public instructions

The SerDes JTAG logic on the LS1088A fully complies with the two mandatory IEEE 1149.6 instructions, EXTEST_PULSE and EXTEST_TRAIN. See *1149.6™-2003, IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks* for a thorough description of these specific instructions.

2.1 EXTEST_PULSE

According to the *IEEE 1149.6™-2003, Section 5.3*, EXTEST_PULSE is a mandatory instruction. It becomes effective at the falling edge of TCK in the UpdateIR TAP controller state. The Boundary Scan Register (BSR) is placed between the Test-Data Input (TDI)

and Test-Data Output (TDO) in a manner similar to the IEEE 1149.1 EXTEST instruction. The timing diagram from the official IEEE 1149.6 document is depicted in Figure 1.

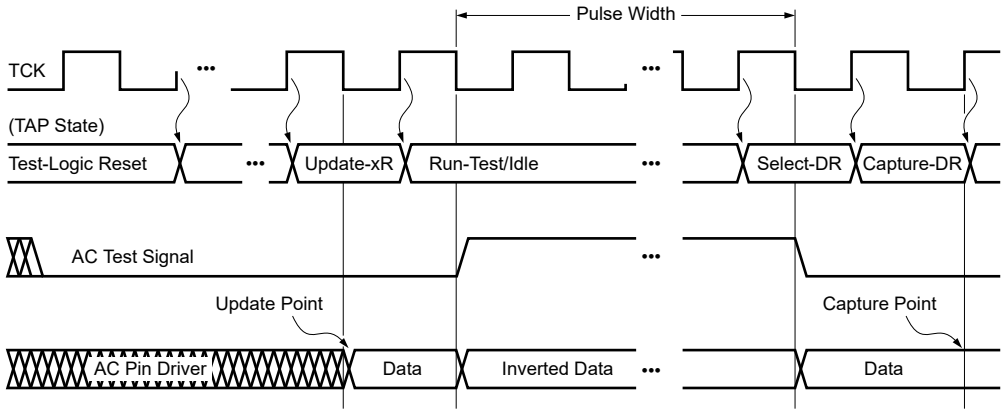

Figure 1. EXTEST_PULSE_behavior

A high-level description of behavior during the EXTEST_PULSE instruction is as follows:

- Normal DC pins behave in the same manner as the EXTEST instruction
- Select AC Behavior for each differential SerDes TX/TX_B pin pair and enable the driver. This condition then drives the logic value in the BSR on the pin pair onto the pins at the falling edge of Test Clock (TCK) in the UpdateIR or UpdateDR states. When Run-Test/Idle is entered, the differential pin drives the inverted data signal starting at the falling edge of TCK. The differential pin drivers transition back to the original, non-inverted state at the falling edge of TCK when Run-Test/Idle state is exited, as shown in Figure 1 on the AC pin driver signals. This event generates a pulse of inverted data on a driver that is as wide as the time spent in the Run-Test/Idle TAP controller state.
- If the Run-Test/Idle TAP controller state is not entered, the output behavior of the SerDes TX pins is not distinguishable from the (DC) EXTEST instruction.
- If AC Behavior is not selected, then each differential SerDes TX/TX_B pin behaves the same as with the EXTEST instruction.
- The SerDes RX/RX_B pins are equipped with test receivers. The differential SerDes channels have one test receiver per leg. When either the EXTEST_PULSE or EXTEST_TRAIN instructions are in effect, it is the responsibility of the test receiver to reconstruct the test waveform driven by the upstream driver when either AC-coupling or DC-coupling is used. It does so by reacting to the edges and not the levels of the input waveform. When (DC) EXTEST is in effect, the test receiver behaves as a level detector.

For a thorough description of this instruction, see *1149.6™-2003, IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks*.

2.2 EXTEST_TRAIN

EXTEST_TRAIN is a mandatory instruction according to the *IEEE 1149.6™ Section 5.4*. It becomes effective at the falling edge of TCK in the UpdateIR TAP controller state. The boundary register is placed between TDI and TDO, similar to the IEEE 1149.1 EXTEST instruction. The timing diagram from the official IEEE 1149.6 document is depicted in Figure 2.

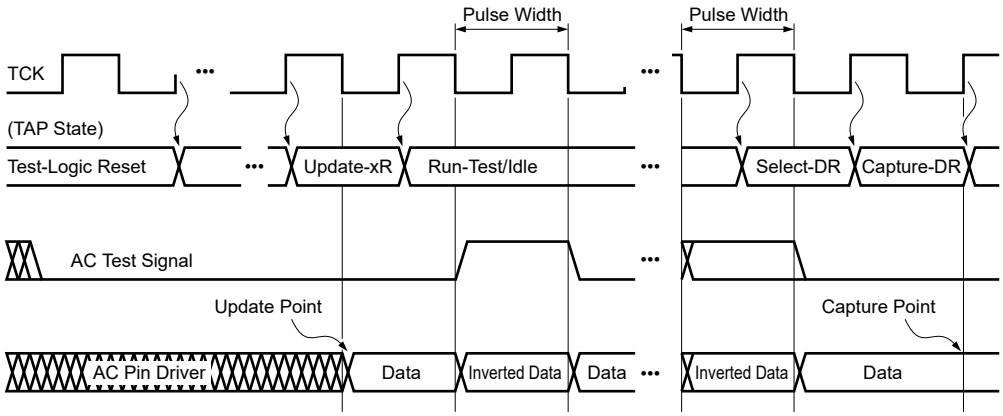

Figure 2. EXTEST_TRAIN behavior

EXTEST_TRAIN is similar to EXTEST_PULSE except in AC Behavior mode. It enables SerDes TX/TX_B pins to toggle between inverted BSR and non-inverted BSR states for each falling edge of TCK while remaining in the Run-Test/Idle state. This process is shown in the Figure 2 on the AC pin driver signals.

For a thorough description of these instructions, see *1149.6™-2003, IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks*.

3 INIT_SETUP instruction

The SerDes channels on the LS1088A are configurable to support the signaling levels required for different interface protocols. To ensure correct electrical behavior, the LS1088A provides the INIT_SETUP instruction and an associated Test Data Register (TDR). These two components allow for the correct configuration of the SerDes pins based on the board configuration where an IEEE 1149.6™ compliant board interconnect test would be applied.

The INIT_SETUP instruction is a custom public JTAG instruction. It is similar to, yet different from, the INITIALIZE instruction discussed in *IEEE 1149.6, ANNEX E*. This instruction is used to preconfigure the electrical parameters of the SerDes RX receivers and TX transmitters to support testing across multiple electrical or physical protocols. Few combinations of signaling levels used by an LS1088A SerDes channel at a given time can potentially be incompatible with SerDes channel signaling of another part on the board. This incompatibility happens due to the difference between the signaling levels of the different protocols. This necessitated the creation of a new instruction to set up the proper voltage levels for the desired protocol during the testing process.

The INIT_SETUP instruction places the TDR between TDI and TDO of the SoC. The proper I/O configuration is shifted-in to set up the correct voltage levels for a given SerDes protocol on a per TX or RX channel basis. Most industrial JTAG board-level interconnect tools support the use of such an instruction to handle multiple physical protocols over a high-speed serial interface.

The INIT_SETUP instruction should be executed as a “preamble” instruction when needed, prior to the execution of other IEEE 1149.1 or IEEE 1149.6 instructions that control the SerDes pins. These instructions are EXTEST, EXTEST_PULSE, EXTEST_TRAIN, and CLAMP. The other IEEE 1149.1-supported instructions (BYPASS, IDCODE, and PRELOAD) always run correctly without the use of the INIT_SETUP instruction.

The SAMPLE instruction is a special case. The INIT_SETUP TDR per-channel settings do not apply during SAMPLE by default, but they are in effect on the TX/TX_B pairs and RX/RX_B pairs if the TDR[sd_sample_override] bit is set. For more information, see the Full TDR layout.

3.1 INIT_SETUP and JTAG TAP state machine

As with prior JTAG implementations, there are two independent sets of controls over the electrical behavior of the SerDes RX and TX analog circuits. The first is the normal, functional “mission” mode, which is how the SerDes lanes are configured in actual production use. The second is JTAG 1149.1/1149.6 test mode where JTAG instructions take priority and control the SerDes RX/TX configurations when the EXTEST instructions are being executed.

When INIT_SETUP is the active instruction, the bits of a new TDR are not clocked during the CaptureDR JTAG state. During Shift-DR, the TDR is placed between TDI and TDO of the SoC. The bits shift through the ports of the functional flip-flops of each SerDes lane to load the desired INIT_SETUP data.

NOTE

During the TestLogicReset state or TRST_B assertion, the INIT_SETUP TDR is reset to a default condition (all zeros). The default protocol is PCI Express for SerDes lanes and the SATA-equivalent 200 mV levels for the PLL reference clock lanes, until changed by a subsequent Shift-DR of the INIT_SETUP instruction. There is no action taken during other states of the TAP state machine or during other instructions. When configured, the settings remain undisturbed until either TSRT_B is asserted, the Test Logic Reset State is entered, or the TDR is changed by another Shift-DR of the INIT_SETUP instruction.

3.2 JTAG opcodes

The new IEEE 1149.6™ JTAG opcodes, as defined in the BSDL file, are shown in Table 1.

Table 1. JTAG 1149.6 public opcodes

JTAG mnemonic	Category	Opcode	
		Binary	Hex
EXTEST_PULSE	Public mandatory	11110101	0xF5
EXTEST_TRAIN		11110110	0xF6
INIT_SETUP	Public custom	11010000	0xD0

3.3 Test Data Register

The TDR is implemented as a serial scan chain. The TDR, described in Table 5, consists of 456 bits. Non-reserved bits contain the bit fields which must configure the platform of SerDes logic for the IEEE 1149.6™ operation. Reserved bits must be set to 0. Behavior is not guaranteed for non-zero settings of reserved bits. Bit 0 connects to TDO, and bit 405 connects to TDI during INIT_SETUP Shift-DR.

3.3.1 TDR global configuration

The TDR has two global configuration bits that apply to all lanes and five individual control bits for each lane. The global configuration bits are TDR[DDR_vsel_override], TDR[jtag_xpad_lo_volt_sel], and TDR[jtag_sample_override], as follows:

- TDR[DDR_vsel_override] determines the DDR G1VDD voltage level, which is 1.2 V or 1.35 V. See the *LS1088A QorIQ Integrated Processor Hardware Specifications* for the specific voltage ranges.
- TDR[jtag_xpad_lo_volt_sel] is fixed to select SerDes XVDD voltage level to 1.35 V. See the *LS1088A QorIQ Integrated Processor Hardware Specifications* for the specific voltage ranges.
- TDR[jtag_sample_override] indicates whether explicit protocol control should be employed during the execution of the SAMPLE instruction to override the mission protocol configuration for the purposes of running a test scenario.

NOTE

The advanced I/O pins are compliant with the IEEE 1149.6™ except that there are limitations placed on SAMPLE. These limitations are due to the inherent practical issues associated with capturing the value of gigabit signaling of the slow and asynchronous TCK at the IEEE 1149.6 test receivers across the externally AC-coupled interfaces.

When the TDR[jtag_sample_override] bit is set, the SD1_RXn capture values on the pins during SAMPLE. Unless the value driven is slow or static, the value cannot be predicted. If the lanes are running at a selected protocol frequency, the use of SAMPLE can affect the signal integrity of the functional data transmissions.

When the TDR[jtag_sample_override] bit is set, the SerDes receive and transmit signals using an internal DC-coupled sample configuration based on electrical settings from the TDR register. When the TDR[jtag_sample_override] bit is not set, the SerDes receive and transmit signals using an internal AC-coupled sample configuration based on their normal electrical settings from the functional mission logic during SAMPLE.

An inherent limitation for SAMPLE is that the IEEE 1149.6 test receivers reject high-speed signals as high-frequency 'noise'. Hence, the protocol data rate must be slow enough to pass through this glitch rejection filtering. In addition, it must be fast enough not to decay below the threshold of the test receivers due to the presence of external AC-coupling at the external interface.

3.3.2 TDR SerDes lane protocol configuration

There is a TDR bit field composed of five bits for each lane, shown in the Figure 3. This field is further subdivided into two subfields. The first three bits [4:2] specify the configuration for the RX protocol. The final two bits [1:0] specify the configuration of the TX protocol for the same lane. Fully mapped bit field decode values for configuring the RX and TX protocols are defined in Table 2 and Table 3.

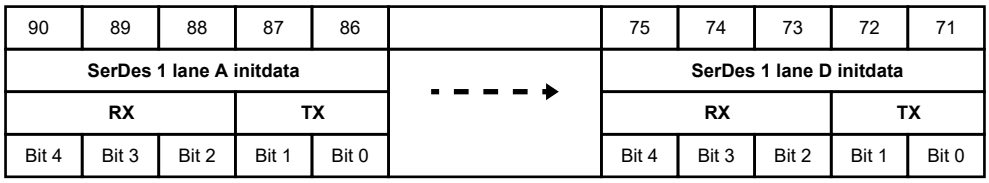

Figure 3. SerDes INIT_SETUP TDR fields for RX and TX

The first three bits specify the decode values for the RX protocol, shown in Table 2.

Table 2. RX configuration protocol decode

RX protocols	INIT_SETUP settings
PEX3, PEX2, PEX, 1000BaseKX	000
Reserved	001
SRIO Short, SGMII 2.5x, QSGMII, JEDEC, SATA, XFI, 10GBaseKR	010
SGMII	011
Reserved	1xx

The final two bits specify the decode values for the TX protocol, shown in Table 3.

Table 3. TX configuration protocol decode

TX protocols	INIT_SETUP settings
PEX3, PEX2, PEX, SGMII 2.5x, HiGig, 10GBaseKR, 1000BaseKX (1.0*full swing)	00
SRIO Short, QSGMII, JEDEC (0.75*full swing)	01

Table continues on the next page...

Table 3. TX configuration protocol decode (continued)

TX protocols	INIT_SETUP settings
SATA, Interlaken 10G, Interlaken Short, JEDEC, XFI (0.585*full swing)	10
SGMII, JDEC (0.667*full swing)	11

The RX and TX settings of a given lane are independent of the settings of all other lanes and also of each other. It is up to the user to program both RX and TX to the same protocol values.

3.3.3 TDR SerDes reference clock configuration

The setting of the configuration bits for the reference clock receivers for SerDes bank is specified in TDR[pll1_config] and TDR[pll2_config] as described in Figure 4 and Table 4.

The final two bits are cleared (set to zero) for the two SerDes reference clock settings because there are no associated TX/TX_B pins.

SerDes bank *b*				
Ref Clock *n*			Cleared	
Bit 4	Bit 3	Bit 2	0	0

Figure 4. SerDes INIT_SETUP TDR fields for ref clocks

Table 4 shows the decode values for the reference clocks for SerDes banks.

Table 4. SerDes bank reference clock decode values

Reference clock configuration	INIT_SETUP settings PLL1/2 initdata[4:2]	INIT_SETUP settings PLL1/2 initdata[1:0]
Reference Clock 400 mV min, shunts on-chip AC coupling, used when board is externally AC-Coupled	000	00 Reserved
Reference Clock 200 mV min, shunts on-chip AC coupling, used when board is externally AC-Coupled	010	00 Reserved
Reference Clock 400 mV min, on-chip AC coupling, used when board is externally DC-Coupled	100	00 Reserved
Reference Clock 200 mV min, on-chip AC coupling, used when board is externally DC-Coupled	110	00 Reserved
All other values are reserved	-	00 Reserved

3.3.4 Full TDR layout

It is recommended to use the standard INIT_SETUP instruction before doing any testing in Boundary SCAN. It is mandatory to use INIT_SETUP for any checking of IO pad.

Table 5 lists the format of the entire TDR and the contents of each field.

Table 5. TDR layout

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
USB	455	ref_ssp_en	1	Set to 0 for JTAG operations per IP vendor	
	454	ref_clkdiv2	0		
	453	mpll_multiplier	0		
	452		0		
	451		0		
	450		0		
	449		0		
	448		0		
	447		0		
	446	tx_vboost_lvl	1	Set to 3'b100 per IP vendor	
	445		0		
	444		0		
	443	ssc_ref_clk_sel	0		
	442		0		
	441		0		
	440		0		
	439		0		
	438		0		
	437		0		
	436		0		
	435		0		
	434	ssc_range	0		
	433		0		
	432		0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	431	acjt_level	0		
	430		0		
	429		0		
	428		0		
	427		0		
	426	pcs_rx_los_mask_val	0		
	425		0		
	424		0		
	423		0		
	422		0		
	421		0		
	420		0		
	419		0		
	418		0		
	417		0		
	416	pcs_tx_swing_full	1	Set to 'd127 per IP vendor	
	415		1		
	414		1		
	413		1		
	412		1		
	411		0		
	410		0		
	409	pcs_tx_deemph_6db	1		
	408		0		
	407		0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	406		0		
	405		1		
	404		1		
	403	pcs_tx_deemph_3p5db	0	Set to 'd24 per IP vendor	
	402		1		
	401		1		
	400		0		
	399		0		
	398		0		
	397	los_bias	1		
	396		0		
	395		1		
	394	VATESTENB	0		
	393		0		
	392	TXPREEMPPULSETUNE	0		
	391	TXVREFTUNE0	1		
	390		0		
	389		0		
	388		1		
	387	TXRISETUNE0	0		
	386		1		
	385	TXRESTUNE0	0		
	384		1		
	383	TXPREEMPAMPTUNE0	0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	382		1		
	381	TXHSXVTUNE0	1		
	380		1		
	379	TXFSLSTUNE0	0		
	378		0		
	377		1		
	376		1		
	375	SQRXTUNE0	0		
	374		0		
	373		0		
	372	OTGTUNE0	1		
	371		0		
	370		0		
	369	COMPDISTUNE0	1		
	368		0		
	367		0		
Pin Control	366	TVDD Voltage Select	0	00 = 3.3 V (do not use) 01 = 2.5 V 10 = 2.5 V 11 = 1.2 V/1.8 V	
	365		0		
	364	LVDD Voltage Select	0	00 = 3.3 V (do not use) 01 = 2.5 V 10 = 2.5 V 11 = 1.2 V/1.8 V	
	363		0		
	362	EVDD Voltage Select	0	00 = 3.3 V 01 = 2.5 V (do not use) 10 = 2.5 V (do not use)	
	361		0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
				11 = 1.2 V/1.8 V	
	360	DVDD Voltage Select	0	00 = 3.3 V 01 = 2.5 V (do not use) 10 = 2.5 V (do not use) 11 = 1.2 V/1.8 V	
	359		0		
	358	Auto-Detect Voltage	0	0 = auto (Voltage Select bits are don't care) 1 = manual (Use Voltage Select bits)	
	357	LVTTL control for ec2_rx_dv	0	0 = LVCMOS input levels 1 = LVTTL input levels	
	356	LVTTL control for ec2_rx_clk	0		
	355	LVTTL control for ec2_rxd3	0		
	354	LVTTL control for ec2_rxd2	0		
	353	LVTTL control for ec2_rxd1	0		
	352	LVTTL control for ec2_rxd0	0		
	351	LVTTL control for ec2_gtx_clk125	0		
	350	LVTTL control for ec2_gtx_clk	0		
	349	LVTTL control for ec2_tx_en	0		
	348	LVTTL control for ec2_txd3	0		
	347	LVTTL control for ec2_txd2	0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	346	LVTTL control for ec2_txd1	0		
	345	LVTTL control for ec2_txd0	0		
	344	LVTTL control for ec1_rx_dv	0		
	343	LVTTL control for ec1_rx_clk	0		
	342	LVTTL control for ec1_rxd3	0		
	341	LVTTL control for ec1_rxd2	0		
	340	LVTTL control for ec1_rxd1	0		
	339	LVTTL control for ec1_rxd0	0		
	338	LVTTL control for ec1_gtx_clk125	0		
	337	LVTTL control for ec1_gtx_clk	0		
	336	LVTTL control for ec1_tx_en	0		
	335	LVTTL control for ec1_txd3	0		
	334	LVTTL control for ec1_txd2	0		
	333	LVTTL control for ec1_txd1	0		
	332	LVTTL control for ec1_txd0	0		
	331	LVTTL control for usb_pwrfault	0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	330	LVTTL control for usb_drvvbus	0		
	329	LVTTL control for iic4_sda	0		
	328	LVTTL control for iic4_scl	0		
	327	LVTTL control for iic3_sda	0		
	326	LVTTL control for iic3_scl	0		
	325	LVTTL control for emi_mdio	0		
	324	LVTTL control for emi_mdc	0		
	323	LVTTL control for irq11	0		
	322	LVTTL control for irq10	0		
	321	LVTTL control for irq9	0		
	320	LVTTL control for irq8	0		
	319	LVTTL control for irq7	0		
	318	LVTTL control for irq6	0		
	317	LVTTL control for irq5	0		
	316	LVTTL control for irq4	0		
	315	LVTTL control for irq3	0		
	314	LVTTL control for sdhc_clk	0		
	313	LVTTL control for sdhc_dat3	0		
	312	LVTTL control for sdhc_dat2	0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	311	LVTTL control for sdhc_dat1	0		
	310	LVTTL control for sdhc_dat0	0		
	309	LVTTL control for sdhc_cmd	0		
	308	LVTTL control for iic2_sda	0		
	307	LVTTL control for iic2_scl	0		
	306	LVTTL control for iic1_sda	0		
	305	LVTTL control for iic1_scl	0		
	304	LVTTL control for uart2_cts_b	0		
	303	LVTTL control for uart1_cts_b	0		
	302	LVTTL control for uart2_rts_b	0		
	301	LVTTL control for uart1_rts_b	0		
	300	LVTTL control for uart2_sin	0		
	299	LVTTL control for uart1_sin	0		
	298	LVTTL control for uart2_sout	0		
	297	LVTTL control for uart1_sout	0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	296	dse_grp_f	1	Drive Strength Enable group F, 000 - output driver disabled 001 = 240 Ohms 010 = 120 Ohms 011 = 80 Ohms 100 = 60 Ohms 101 = 48 Ohms 110 = 40 Ohms 111 = 34 Ohms (max drive)	Includes pins irq11, irq10, irq9, irq8, irq7, irq6, irq5, irq4, irq3, usb_drvvbus, usb_pwrfault
	295		0		
	294		0		
	293	dse_grp_e	1	Drive Strength Enable group E, 000 - output driver disabled 001 = 240 Ohms 010 = 120 Ohms 011 = 80 Ohms 100 = 60 Ohms 101 = 48 Ohms 110 = 40 Ohms 111 = 34 Ohms (max drive)	Includes pins ec1_gtx_clk125, ec1_rx_clk, ec1_rx_dv, ec1_rxd0, ec1_rxd1, ec1_rxd2, ex1_rxd3, ec1_tx_en, ec1_txd0, ec1_txd1, ec1_txd2, ec1_txd3, ec2_gtx_clk, ec2_gtx_clk125, ec2_rx_clk, ec2_rx_dv, ec2_rxd0, ec2_rxd1, ec2_rxd2, ec2_rxd3, ex2_tx_en, ec2_txd0, ec2_txd1, ec2_txd2, ec2_txd3
	292		1		
	291		0		
	290	dse_grp_d	1	Drive Strength Enable group D, 000 - output driver disabled 001 = 240 Ohms 010 = 120 Ohms 011 = 80 Ohms 100 = 60 Ohms 101 = 48 Ohms 110 = 40 Ohms 111 = 34 Ohms (max drive)	Includes pins emi2_mdio
	289		1		
	288		1		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	287	dse_grp_c	1	Drive Strength Enable group C, 000 - output driver disabled 001 = 240 Ohms 010 = 120 Ohms 011 = 80 Ohms 100 = 60 Ohms 101 = 48 Ohms 110 = 40 Ohms 111 = 34 Ohms (max drive)	Includes pins emi2_mdc
	286		1		
	285		1		
	284	dse_grp_b	1	Drive Strength Enable group B, 000 - output driver disabled 001 = 240 Ohms 010 = 120 Ohms 011 = 80 Ohms 100 = 60 Ohms 101 = 48 Ohms 110 = 40 Ohms 111 = 34 Ohms (max drive)	Includes pins sdhc_clk, sdhc_cmd, sdhc_dat0, sdhc_dat1, sdhc_dat2, sdhc_dat3
	283		1		
	282		1		
	281	dse_grp_a	1	Drive Strength Enable group A, 000 = output driver disabled 001 = 240 Ohms 010 = 120 Ohms 011 = 80 Ohms 100 = 60 Ohms 101 = 48 Ohms 110 = 40 Ohms 111 = 34 Ohms (max drive)	Includes pins iic1_scl, iic1_sda, iic2_scl, iic2_sda, iic3_scl, iic3_sda, iic4_scl, iic4_sda, uart1_cts_b, uart1_rts_b, uart1_sin, uart1_sout, uart2_cts_b, uart2_rts_b, uart2_sin, uart2_sout
	280		0		
	279		1		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	278	Hysterisis control for ec2_rx_dv	0	0=off (CMOS input) 1= on (Schmitt trigger input)	
	277	Hysterisis control for ec2_rx_clk	0		
	276	Hysterisis control for ec2_rxd3	0		
	275	Hysterisis control for ec2_rxd2	0		
	274	Hysterisis control for ec2_rxd1	0		
	273	Hysterisis control for ec2_rxd0	0		
	272	Hysterisis control for ec2_gtx_clk125	0		
	271	Hysterisis control for ec2_gtx_clk	0		
	270	Hysterisis control for ec2_tx_en	0		
	269	Hysterisis control for ec2_txd3	0		
	268	Hysterisis control for ec2_txd2	0		
	267	Hysterisis control for ec2_txd1	0		
	266	Hysterisis control for ec2_txd0	0		
	265	Hysterisis control for ec1_rx_dv	0		
	264	Hysterisis control for ec1_rx_clk	0		
	263	Hysterisis control for ec1_rxd3	0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	262	Hysterisis control for ec1_rxd2	0		
	261	Hysterisis control for ec1_rxd1	0		
	260	Hysterisis control for ec1_rxd0	0		
	259	Hysterisis control for ec1_gtx_clk125	0		
	258	Hysterisis control for ec1_gtx_clk	0		
	257	Hysterisis control for ec1_tx_en	0		
	256	Hysterisis control for ec1_txd3	0		
	255	Hysterisis control for ec1_txd2	0		
	254	Hysterisis control for ec1_txd1	0		
	253	Hysterisis control for ec1_txd0	0		
	252	Hysterisis control for usb_pwrfault	0		
	251	Hysterisis control for usb_drvvbus	0		
	250	Hysterisis control for iic4_sda	0		
	249	Hysterisis control for iic4_scl	0		
	248	Hysterisis control for iic3_sda	0		
	247	Hysterisis control for iic3_scl	0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	246	Hysterisis control for emi_mdio	0		
	245	Hysterisis control for emi_mdc	0		
	244	Hysterisis control for irq11	0		
	243	Hysterisis control for irq10	0		
	242	Hysterisis control for irq9	0		
	241	Hysterisis control for irq8	0		
	240	Hysterisis control for irq7	0		
	239	Hysterisis control for irq6	0		
	238	Hysterisis control for irq5	0		
	237	Hysterisis control for irq4	0		
	236	Hysterisis control for irq3	0		
	235	Hysterisis control for sdhc_clk	0		
	234	Hysterisis control for sdhc_dat3	0		
	233	Hysterisis control for sdhc_dat2	0		
	232	Hysterisis control for sdhc_dat1	0		
	231	Hysterisis control for sdhc_dat0	0		
	230	Hysterisis control for sdhc_cmd	0		
	229	Hysterisis control for iic2_sda	0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	228	Hysterisis control for iic2_scl	0		
	227	Hysterisis control for iic1_sda	0		
	226	Hysterisis control for iic1_scl	0		
	225	Hysterisis control for uart2_cts_b	0		
	224	Hysterisis control for uart1_cts_b	0		
	223	Hysterisis control for uart2_rts_b	0		
	222	Hysterisis control for uart1_rts_b	0		
	221	Hysterisis control for uart2_sin	0		
	220	Hysterisis control for uart1_sin	0		
	219	Hysterisis control for uart2_sout	0		
	218	Hysterisis control for uart1_sout	0		
	217	Slewrate control for ec2_rx_dv	1	00 = Slow slew rate 01 = Medium slew rate 10 = Fast slew rate 11 = Max slew rate	
	216		0		
	215	Slewrate control for ec2_rx_clk	1		
	214		0		
	213	Slewrate control for ec2_rxd3	1		
	212		0		
	211	Slewrate control for ec2_rxd2	1		
	210		0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	209	Slewrate control for ec2_rxd1	1		
	208		0		
	207	Slewrate control for ec2_rxd0	1		
	206		0		
	205	Slewrate control for ec2_gtx_clk125	1		
	204		0		
	203	Slewrate control for ec2_gtx_clk	1		
	202		0		
	201	Slewrate control for ec2_tx_en	1		
	200		0		
	199	Slewrate control for ec2_txd3	1		
	198		0		
	197	Slewrate control for ec2_txd2	1		
	196		0		
	195	Slewrate control for ec2_txd1	1		
	194		0		
	193	Slewrate control for ec2_txd0	1		
	192		0		
	191	Slewrate control for ec1_rx_dv	1		
	190		0		
	189	Slewrate control for ec1_rx_clk	1		
	188		0		
	187	Slewrate control for ec1_rxd3	1		
	186		0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note
	185	Slewrate control for ec1_rxd2	1	
	184		0	
	183	Slewrate control for ec1_rxd1	1	
	182		0	
	181	Slewrate control for ec1_rxd0	1	
	180		0	
	179	Slewrate control for ec1_gtx_clk125	1	
	178		0	
	177	Slewrate control for ec1_gtx_clk	1	
	176		0	
	175	Slewrate control for ec1_tx_en	1	
	174		0	
	173	Slewrate control for ec1_txd3	1	
	172		0	
	171	Slewrate control for ec1_txd2	1	
	170		0	
	169	Slewrate control for ec1_txd1	1	
	168		0	
	167	Slewrate control for ec1_txd0	1	
	166		0	
	165	Slewrate control for usb_pwrfault	0	
	164		0	
	163	Slewrate control for usb_drvvbus	0	
	162		0	

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	161	Slewrate control for iic4_sda	0		
	160		0		
	159	Slewrate control for iic4_scl	0		
	158		0		
	157	Slewrate control for iic3_sda	0		
	156		0		
	155	Slewrate control for iic3_scl	0		
	154		0		
	153	Slewrate control for emi_mdio	1		
	152		0		
	151	Slewrate control for emi_mdc	1		
	150		0		
	149	Slewrate control for irq11	0		
	148		0		
	147	Slewrate control for irq10	0		
	146		0		
	145	Slewrate control for irq9	0		
	144		0		
	143	Slewrate control for irq8	0		
	142		0		
	141	Slewrate control for irq7	0		
	140		0		
	139	Slewrate control for irq6	0		
	138		0		
	137	Slewrate control for irq5	0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	136		0		
	135	Slewrate control for irq4	0		
	134		0		
	133	Slewrate control for irq3	0		
	132		0		
	131	Slewrate control for sdhc_clk	1		
	130		0		
	129	Slewrate control for sdhc_cmd	1		
	128		0		
	127	Slewrate control for sdhc_dat3	1		
	126		0		
	125	Slewrate control for sdhc_dat2	1		
	124		0		
	123	Slewrate control for sdhc_dat1	1		
	122		0		
	121	Slewrate control for sdhc_dat0	1		
	120		0		
	119	Slewrate control for iic2_sda	0		
	118		0		
	117	Slewrate control for iic2_scl	0		
	116		0		
	115	Slewrate control for iic1_sda	0		
	114		0		
	113	Slewrate control for iic1_scl	0		
	112		0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	111	Slewrate control for uart2_cts_b	0		
	110		0		
	109	Slewrate control for uart1_cts_b	0		
	108		0		
	107	Slewrate control for uart2_rts_b	0		
	106		0		
	105	Slewrate control for uart1_rts_b	0		
	104		0		
	103	Slewrate control for uart2_sin	0		
	102		0		
	101	Slewrate control for uart1_sin	0		
	100		0		
	99	Slewrate control for uart2_sout	0		
	98		0		
	97	Slewrate control for uart1_sout	0		
	96		0		
SerDes 1	95	PLL1 initdata	0	[4] REF Clock ioconfig	111 = Reserved 110 = Reference Clock 200 mV min, on-chip AC coupling, used when board is externally DC-Coupled 101 = Reserved 100 = Reference Clock 400 mV min, on-chip AC coupling, used when board is externally DC-Coupled 011 = Reserved 010 = Reference Clock 200 mV min, shunts on-chip AC coupling, used when board is externally AC-Coupled 001 = Reserved
	94		0	[3] REF Clock ioconfig	
	93		0	[2] REF Clock ioconfig	

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
					000 = Reference Clock 400 mV min, shunts on-chip AC coupling, used when board is externally AC-Coupled
	92		0	[1] reserved	
	91		0	[0] reserved	
	90	Lane A initdata	0	[4] RX ioconfig	111 = Reserved 110 = Reserved 101 = Reserved 100 = Reserved 011 = SGMII 010 = SRIO Short, SGMII 2.5x, QSGMII, JEDEC, SATA, XFI, Interlaken Short, Interlaken 10G, 10GBaseKR 001 = Reserved 000 = PEX3, PEX2, PEX, 1000BaseKX
	89		0	[3] RX ioconfig	
	88		0	[2] RX ioconfig	
	87		0	[1] TX ioconfig	11= SGMII, JDEC (0.667*full swing) 10 = SATA, Interlaken 10G, Interlaken Short, JEDEC, XFI (0.585*full swing) 01 = SRIO Short, QSGMII, JEDEC (0.75*full swing) 00 = PEX3, PEX2, PEX, SGMII 2.5x, 10GBaseKR, 1000BaseKX (1.0*full swing)
	86		0	[0] TX ioconfig	
	85	Lane B initdata	0	[4] RX ioconfig	111 = Reserved 110 = Reserved 101 = Reserved 100 = Reserved 011 = SGMII 010 = SRIO Short, SGMII 2.5x, QSGMII, JEDEC, SATA, XFI, Interlaken Short, Interlaken 10G, 10GBaseKR 001 = Reserved 000 = PEX3, PEX2, PEX, 1000BaseKX
	84		0	[3] RX ioconfig	
	83		0	[2] RX ioconfig	

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	82		0	[1] TX ioconfig	11= SGMII, JDEC (0.667*full swing) 10 = SATA, Interlaken 10G, Interlaken Short, JEDEC, XFI (0.585*full swing) 01 = SRIO Short, QSGMII, JEDEC (0.75*full swing) 00 = PEX3, PEX2, PEX, SGMII 2.5x, 10GBaseKR, 1000BaseKX (1.0*full swing)
	81		0	[0] TX ioconfig	
	80	Lane C initdata	0	[4] RX ioconfig	111 = Reserved 110 = Reserved 101 = Reserved 100 = Reserved 011 = SGMII 010 = SRIO Short, SGMII 2.5x, QSGMII, JEDEC, SATA, XFI, Interlaken Short, Interlaken 10G, 10GBaseKR 001 = Reserved 000 = PEX3, PEX2, PEX, 1000BaseKX
	79		0	[3] RX ioconfig	
	78		0	[2] RX ioconfig	
	77		0	[1] TX ioconfig	11= SGMII, JDEC (0.667*full swing) 10 = SATA, Interlaken 10G, Interlaken Short, JEDEC, XFI (0.585*full swing) 01 = SRIO Short, QSGMII, JEDEC (0.75*full swing) 00 = PEX3, PEX2, PEX, SGMII 2.5x, 10GBaseKR, 1000BaseKX (1.0*full swing)
	76		0	[0] TX ioconfig	
	75	Lane D initdata	0	[4] RX ioconfig	111 = Reserved 110 = Reserved 101 = Reserved 100 = Reserved 011 = SGMII 010 = SRIO Short, SGMII 2.5x, QSGMII, JEDEC, SATA, XFI, Interlaken Short, Interlaken 10G, 10GBaseKR 001 = Reserved
	74		0	[3] RX ioconfig	
	73		0	[2] RX ioconfig	

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
					000 = PEX3, PEX2, PEX, 1000BaseKX
	72		0	[1] TX ioconfig	11= SGMII, JDEC (0.667*full swing) 10 = SATA, Interlaken 10G, Interlaken Short, JEDEC, XFI (0.585*full swing) 01 = SRIO Short, QSGMII, JEDEC (0.75*full swing) 00 = PEX3, PEX2, PEX, SGMII 2.5x, 10GBaseKR, 1000BaseKX (1.0*full swing)
	71		0	[0] TX ioconfig	
	70		0	[4] REF Clock ioconfig	111 = Reserved 110 = Reference Clock 200 mV min, on-chip AC coupling, used when board is externally DC-Coupled 101 = Reserved 100 = Reference Clock 400 mV min, on-chip AC coupling, used when board is externally DC-Coupled 011 = Reserved 010 = Reference Clock 200 mV min, shunts on-chip AC coupling, used when board is externally AC-Coupled 001 = Reserved 000 = Reference Clock 400 mV min, shunts on-chip AC coupling, used when board is externally AC-Coupled
	69		0	[3] REF Clock ioconfig	
	68	PLL2 initdata	0	[2] REF Clock ioconfig	
	67		0	[1] reserved	
	66		0	[0] reserved	
SerDes 2	65	PLL1 initdata	0	[4] REF Clock ioconfig	111 = Reserved 110 = Reference Clock 200 mV min, on-chip AC coupling, used when board is externally DC-Coupled 101 = Reserved 100 = Reference Clock 400 mV min, on-chip AC coupling, used when board is externally DC-Coupled 011 = Reserved
	64		0	[3] REF Clock ioconfig	
	63		0	[2] REF Clock ioconfig	

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
					010 = Reference Clock 200 mV min, shunts on-chip AC coupling, used when board is externally AC-Coupled 001 = Reserved 000 = Reference Clock 400 mV min, shunts on-chip AC coupling, used when board is externally AC-Coupled
	62		0	[1] reserved	
	61		0	[0] reserved	
	60	Lane A initdata	0	[4] RX ioconfig	111 = Reserved 110 = Reserved 101 = Reserved 100 = Reserved 011 = SGMII 010 = SRIO Short, SGMII 2.5x, QSGMII, JEDEC, SATA, XFI, Interlaken Short, Interlaken 10G, 10GBaseKR 001 = Reserved 000 = PEX3, PEX2, PEX, 1000BaseKX
	59		0	[3] RX ioconfig	
	58		0	[2] RX ioconfig	
	57		0	[1] TX ioconfig	11= SGMII, JDEC (0.667*full swing) 10 = SATA, Interlaken 10G, Interlaken Short, JEDEC, XFI (0.585*full swing) 01 = SRIO Short, QSGMII, JEDEC (0.75*full swing) 00 = PEX3, PEX2, PEX, SGMII 2.5x, 10GBaseKR, 1000BaseKX (1.0*full swing)
	56		0	[0] TX ioconfig	
	55	Lane B initdata	0	[4] RX ioconfig	111 = Reserved 110 = Reserved 101 = Reserved 100 = Reserved 011 = SGMII 010 = SRIO Short, SGMII 2.5x, QSGMII, JEDEC, SATA, XFI, Interlaken Short, Interlaken 10G, 10GBaseKR
	54		0	[3] RX ioconfig	
	53		0	[2] RX ioconfig	

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
					001 = Reserved 000 = PEX3, PEX2, PEX, 1000BaseKX
	52		0	[1] TX ioconfig	11= SGMII, JDEC (0.667*full swing) 10 = SATA, Interlaken 10G, Interlaken Short, JEDEC, XFI (0.585*full swing) 01 = SRIO Short, QSGMII, JEDEC (0.75*full swing) 00 = PEX3, PEX2, PEX, SGMII 2.5x, 10GBaseKR, 1000BaseKX (1.0*full swing)
	51		0	[0] TX ioconfig	
	50	Lane C initdata	0	[4] RX ioconfig	111 = Reserved 110 = Reserved 101 = Reserved 100 = Reserved 011 = SGMII 010 = SRIO Short, SGMII 2.5x, QSGMII, JEDEC, SATA, XFI, Interlaken Short, Interlaken 10G, 10GBaseKR 001 = Reserved 000 = PEX3, PEX2, PEX, 1000BaseKX
	49		0	[3] RX ioconfig	
	48		0	[2] RX ioconfig	
	47		0	[1] TX ioconfig	11= SGMII, JDEC (0.667*full swing) 10 = SATA, Interlaken 10G, Interlaken Short, JEDEC, XFI (0.585*full swing) 01 = SRIO Short, QSGMII, JEDEC (0.75*full swing) 00 = PEX3, PEX2, PEX, SGMII 2.5x, 10GBaseKR, 1000BaseKX (1.0*full swing)
	46		0	[0] TX ioconfig	
	45	Lane D initdata	0	[4] RX ioconfig	111 = Reserved 110 = Reserved 101 = Reserved 100 = Reserved 011 = SGMII
	44		0	[3] RX ioconfig	
	43		0	[2] RX ioconfig	

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
					010 = SRIO Short, SGMII 2.5x, QSGMII, JEDEC, SATA, XFI, Interlaken Short, Interlaken 10G, 10GBaseKR 001 = Reserved 000 = PEX3, PEX2, PEX, 1000BaseKX
	42		0	[1] TX ioconfig	11= SGMII, JDEC (0.667*full swing) 10 = SATA, Interlaken 10G, Interlaken Short, JEDEC, XFI (0.585*full swing) 01 = SRIO Short, QSGMII, JEDEC (0.75*full swing) 00 = PEX3, PEX2, PEX, SGMII 2.5x, 10GBaseKR, 1000BaseKX (1.0*full swing)
	41		0	[0] TX ioconfig	
	40	PLL2 initdata	0	[4] REF Clock ioconfig	111 = Reserved 110 = Reference Clock 200 mV min, on-chip AC coupling, used when board is externally DC-Coupled 101 = Reserved 100 = Reference Clock 400 mV min, on-chip AC coupling, used when board is externally DC-Coupled 011 = Reserved 010 = Reference Clock 200 mV min, shunts on-chip AC coupling, used when board is externally AC-Coupled 001 = Reserved 000 = Reference Clock 400 mV min, shunts on-chip AC coupling, used when board is externally AC-Coupled
	39		0	[3] REF Clock ioconfig	
	38		0	[2] REF Clock ioconfig	
	37		0	[1] reserved	
	36		0	[0] reserved	
COP IOCONFIG	35	ssckio termination	0		
	34		0		
	33		0		

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	32		0		
	31	ssckio fixed term/ misc ovrd	0	0 = calibrated, 1 = selected	
	30	ssckio external	0	0 = AC couple, 1 = DC couple	
	29	ssckio ac_jtag jtag_ctrl threshold value	0	[2]	
	28		0	[1]	
	27		0	[0]	
	26	ssckio to_refclktstx_diff_sysclk	0		
	25		0		
	24	Reserved	0		
	23	Reserved	0		
	22	Reserved	0		
	21	Reserved	0		
	20	SS CKIO Sample Override	0	SS CKIO Sample Override	
	19	SD1 & SD2 Sample Override	0	SD1 & SD2 Sample Override	
	18	Reserved	0		
	17	USB1 PHY reset	0	USB1 PHY reset	
	16	SD2 xvdd_low_vsel	0	0 = 1.5 V, 1 = 1.35 V	
	15	SD1 xvdd_low_vsel	0	0 = 1.5 V, 1 = 1.35 V	
	14	DDR_DSE	0	[0] 1 = full strength	
	13		0	[1] 0 = 1.0 V 1 = 0.9 V	
	12		0	[2]	
	11		0	[3]	

Table continues on the next page...

Table 5. TDR layout (continued)

Block	INIT_SETUP/ TDR Bit	Description	Default	Note	
	10		0	[4]	
	9		0	[5]	
	8		0	[6] 1 = mdic cal en	
	7		0	[7] 1 = select mdic cal loop	
	6		0		
	5	DDR TermSel	0		
	4		0		
	3	Reserved	0		
	2	Reserved	0		
	1	Reserved	0		
	0	Global TDR enable	0	For USB and pins_control_dft 0 = Mission control 1 = TDR control	

Table 6 provides USB3.0 RX aio_parametric levels for calculations of S1-S10 levels.

Table 6. USB3.0 ACJTLEVEL[4:0]

Name	ACJTLEVEL[4:0]	AC Mode Vhystedge (+ -)	DC Mode Vhystlevel (+ only)
usb3_v1	00001	94	60
usb3_v2	00010	116	75
usb3_v3	00011	139	90
usb3_v4	00100	162	105
usb3_v5	00101	187	135
usb3_v6	00110	212	150
usb3_v7	10001	185	60
usb3_v8	10010	217	75

3.4 BSDL file

A BSDL file is available for the LS1088A. The full BSDL file is available on the appropriate NXP website.

4 IEEE 1149.6 compliant pins

The pins listed in Table 7 are defined as IEEE 1149.6™ advanced I/O on the LS1088A. All other I/O pins are defined as standard I/O and comply only with the IEEE 1149.1.

Table 7. SerDes pin list

Signal	Signal name	Pin type
SerDes, PCIe, 10GE, 1GE		
SD1_TX0_P	Transmit Data for SerDes Bank 1 Lane A (positive)	O
SD1_TX1_P	Transmit Data for SerDes Bank 1 Lane B (positive)	O
SD1_TX2_P	Transmit Data for SerDes Bank 1 Lane C (positive)	O
SD1_TX3_P	Transmit Data for SerDes Bank 1 Lane D (positive)	O
SD1_TX0_N	Transmit Data for SerDes Bank 1 Lane A (compliment)	O
SD1_TX1_N	Transmit Data for SerDes Bank 1 Lane B (compliment)	O
SD1_TX2_N	Transmit Data for SerDes Bank 1 Lane C (compliment)	O
SD1_TX3_N	Transmit Data for SerDes Bank 1 Lane D (compliment)	O
SD1_RX0_P	Receive Data for SerDes Bank 1 Lane A (positive)	I
SD1_RX1_P	Receive Data for SerDes Bank 1 Lane B (positive)	I
SD1_RX2_P	Receive Data for SerDes Bank 1 Lane C (positive)	I
SD1_RX3_P	Receive Data for SerDes Bank 1 Lane D (positive)	I
SD1_RX0_N	Receive Data for SerDes Bank 1 Lane A (compliment)	I
SD1_RX1_N	Receive Data for SerDes Bank 1 Lane B (compliment)	I
SD1_RX2_N	Receive Data for SerDes Bank 1 Lane C (compliment)	I
SD1_RX3_N	Receive Data for SerDes Bank 1 Lane D (compliment)	I
SD1_REF_CLK1_P	SerDes Bank 1 PLL 1 Reference Clock (positive)	I
SD1_REF_CLK2_P	SerDes Bank 1 PLL 2 Reference Clock (positive)	I
SD1_REF_CLK1_N	SerDes Bank 1 PLL 1 Reference Clock (compliment)	I
SD1_REF_CLK2_N	SerDes Bank 1 PLL 2 Reference Clock (compliment)	I
USB1_RX_M	USB PHY SS Receive Data (-)	I
USB1_RX_P	USB PHY SS Receive Data (+)	I
USB1_TX_M	USB PHY SS Transmit Data (-)	O
USB1_TX_P	USB PHY SS Transmit Data (+)	O
USB2_RX_M	USB PHY SS Receive Data (-)	I
USB2_RX_P	USB PHY SS Receive Data (+)	I
USB2_TX_M	USB PHY SS Transmit Data (-)	O
USB2_TX_P	USB PHY SS Transmit Data (+)	O

4.1 Compliance pins

The compliance pins listed in Table 8 are supported:

Table 8. Compliance pins

Pin	Description
TBSCAN_EN	TBSCAN_EN_B is an IEEE 1149.1™ JTAG compliance enable pin. 0: To be compliant to the 1149.1 specification for boundary scan functions. The JTAG-compliant state is documented in the BSDL. 1: JTAG connects to DAP controller for the Arm core debug. In normal operation, this pin must be pulled high to OVDD with 4.7 K ohm.
JTAG_BSR_VSEL	JTAG_BSR_VSEL is an IEEE 1149.1 JTAG compliance enable pin. 0: Normal operation. This pin must be pulled down to GND with a pull-down resistor of value 1k ohm. 1: To be compliant to the 1149.1 specification for boundary scan functions. The JTAG-compliant state is documented in the BSDL.
TEST_SEL_B	TEST_SEL_B is an IEEE 1149.1 JTAG compliance enable pin. 1: All cores enabled. This pin must be pulled up to OVDD through 1 K resistance. 0: Disable core 3 and core 4
SCAN_MODE_B	SCAN_MODE_B is an IEEE 1149.1 JTAG compliance enable pin. 1: Functional mode. This pin must be pulled up to OVDD through 1 K resistance. 0: SCAN Mode.

4.2 Unsupported USB pins

The USB pins listed in Table 9 are not supported in boundary scan:

Table 9. Unsupported USB pins

Pin name	Description	I/O type
USB1_D_M	USB PHY HS data (-)	I/O
USB1_D_P	USB PHY HS data (+)	I/O
USB1_ID	USB PHY ID detect	I
USB1_RESREF	USB PHY impedance calibration	I/O
USB2_D_M	USB PHY HS data (-)	I/O
USB2_D_P	USB PHY HS data (+)	I/O
USB2_ID	USB PHY ID detect	I
USB2_RESREF	USB PHY impedance calibration	I/O

4.3 USB reset counter

The USBPHY requires ~2000 clock cycles to come out of reset before to it can become a part of BSR. A counter inside USB_PHY design uses these 2000 clocks de-asserting reset to internal PHY logic. As long as PHY remains in reset state, the boundary scan

continues to fail. Therefore, it is recommended to use INIT_SETUP instructions. The LS1088A device mandates the use of IO config prior to boundary scan.

INIT_SETUP is only 456 bits long and for USB_PHY to come out of reset, ~2000 clock cycles are required. Therefore, to ensure that USB PHY gets required number of cycles to come out of reset, 1906 dummy 0's are shifted through TDI before INIT_SETUP.

5 Revision history

Table 10 summarizes the revisions to this document.

Table 10. Revision history

Revision	Date	Description
0	19 May 2022	Initial public release

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