Mask Set Errata for Mask 1N71K

This report applies to mask 1N71K for these products:

- MKL17Z128VMP4, MKL17Z128VLH4, MKL17Z128VFT4, MKL17Z128VFM4R, MKL17Z128VFM4, KKL17Z256CAL4R, MKL17Z128VMP4R, MKL17Z256CAL4R, MKL17Z256VFM4, MKL17Z256VFT4, MKL17Z256VFT4R, MKL17Z256VLH4, MKL17Z256VMP4, MKL17Z256VMP4R
- MKL27Z128VFM4, MKL27Z128VFT4, MKL27Z128VLH4, MKL27Z128VLH4R, MKL27Z128VMP4, MKL27Z256VFM4, MKL27Z256VFM4R, MKL27Z256VFT4, MKL27Z256VLH4, MKL27Z256VMP4
- MKL33Z128VLH4, MKL33Z128VMP4, MKL33Z256VLH4, MKL33Z256VMP4
- MKL43Z128VLH4, MKL43Z128VMP4, MKL43Z256VLH4, MKL43Z256VMP4

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
e8992	AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode
e9380	FlexIO: Reading FlexIO register when FlexIO functional clock is disabled results in a bus hang
e8777	I2C: Address match wake-up from low-power mode cannot receive data
e9308	I2C: I2C does not hold bus between byte transfers in receive and may result in lost data
e9457	Kinetis Flashloader/ ROM Bootloader: The peripheral auto-detect code in bootloader can falsely detect presence of SPI host causing non-responsive bootloader
e8010	LLWU: CMP flag in LLWU_Fx register cleared by multiple CMP out toggles when exiting LLSx or VLLSx modes.
e7950	LLWU: When exiting from Low Leakage Stop (LLS) mode using the comparator, the comparator ISR is serviced before the LLWU ISR
e10527	LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters
e7986	LPUART: The LPUART_TX pin is tri-stated when the transmitter is disabled
e7914	PIT: After enabling the Periodic Interrupt Timer (PIT) clock gate, an attempt to immediately enable the PIT module may not be successful.
e8060	ROM: Bytes sent from host over I2C and SPI interfaces may be lost
e8058	ROM: COP can't be re-enabled in application code due to being disabled by ROM boot code
e8594	ROM: I2C0_A1 register does not contain the reset default value when MCU boots from ROM
e8595	ROM: ROM read memory command may read the incorrect data back from flash in some cases
e10358	SIM: A reset during system clock divider (SIM_CLKDIV1) update may cause the crossbar switch to stall

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Table 1. Errata and Information Summary (continued)

Erratum ID	Erratum Title
e6396	sLCD: LCD_GCR[RVTRIM] bits are in reverse order
e2580	UART: Start bit sampling not compliant with LIN 2.1 specification
e7857	UART: WT timer in T=0 mode and CWT timer in T=1 mode can expire between 0.2 ETU to 0.8 ETU earlier than programmed.
e7919	USBOTG: In certain situations, software updates to the Start of Frame Threshold Register (USBx_SOFTHLD) may lead to an End of Frame error condition
e7822	USBReg: Some devices have VREG_OUT trim value incorrectly programmed

Table 2. Revision History

Revision	Changes
19 AUGUST 2014	Initial revision
19 SEPTEMBER 2016	The following errata was removed. • e3863 The following errata were added. • e9457 • e8992 • e9308 • e10527 • e9380 • e8777 • e8060 • e8595 • e8594 • e10358 • e8058 • e8010

e8992: AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode

Description: Upon entry into VLPS from VLPR, if NMI is asserted before the VLPS entry completes, then the NMI does not generate a wakeup to the MCU. However, the NMI interrupt will occur after the MCU wakes up by another wake-up event.

Workaround: There are two workarounds:

1) First transition from VLPR mode to RUN mode, and then enter into VLPS mode from RUN mode.

2) Assert NMI signal for longer than 16 bus clock cycles.

e9380: FlexIO: Reading FlexIO register when FlexIO functional clock is disabled results in a bus hang

Description: Accessing a FlexIO register when the FlexIO functional clock is disabled (the clock source configured to 0 in PCC_FLEXIO0[PCS], or the selected clock source is disabled) will hang the bus and the access will stall forever.

Workaround: Always enable the FlexIO functional clock before accessing any FlexIO register.

e8777: I2C: Address match wake-up from low-power mode cannot receive data

Description: When the device is in a low-power mode that supports address match wake-up, receiving a matching address will wake up the MCU, however, the I2C will not respond correctly. I2C traffic after the wake-up address will not generate TCF interrupt events.

Workaround: Either one of the following sequences will enable the address match wake-up to operate correctly:

1) Send only the matching slave address followed by a repeated start and then resend the matching slave address including any subsequent data.

2) Send only the matching slave address followed by a stop condition and then resend the matching slave address including any subsequent data.

e9308: I2C: I2C does not hold bus between byte transfers in receive and may result in lost data

Description: When the I2C module is in receive mode, the bus is typically held by simply not reading the I2C_D register. However, in devices with this errata, the bus is not held between byte transfers by this action. If the I2C_D register and the data buffer are full, incoming data from an I2C device will overwrite data in the data buffer.

Workaround: When configured to receive data, the delay in processing incoming bytes should be minimized. Delay can be minimized by the use of DMA or increased interrupt priority.

e9457: Kinetis Flashloader/ ROM Bootloader: The peripheral auto-detect code in bootloader can falsely detect presence of SPI host causing non-responsive bootloader

Description: During the active peripheral detection process, the bootloader can interpret spurious data on the SPI peripheral as valid data. The spurious data causes the bootloader to shutdown all peripherals except the “falsely detected" SPI and enter the command phase loop using the SPI. After the bootloader enters the command phase loop using the SPI, the other peripherals are ignored, so the desired peripheral is no longer active.

The bootloader will not falsely detect activity on the I2C, UART, or USB interfaces, so only the SPI interface is affected.

Workaround: Ensure that there is an external pull-up on the SPI chip-select pin or that the pin is driven high. This will prevent the bootloader from seeing spurious data due to activity on the SPI clock pin.

e8010: LLWU: CMP flag in LLWU_Fx register cleared by multiple CMP out toggles when exiting LLSx or VLLSx modes.

Description: The comparator's corresponding wakeup flag in the LLWU_Fx register is cleared prematurely if:

1.The CMP output is toggled more than one time during the LLSx wakeup sequence and the comparator's corresponding flag in the LLWU_Fx register is cleared.

Or

2.The CMP output is toggled more than one time during the VLLSx wakeup sequence, PMC_REGSC[ACKISO] is cleared, and the comparator's corresponding flag in the LLWU_Fx register is cleared.

Workaround: When MCU is waking up from LLS, code can implement a software flag to retain the wakeup source, if required by software.

When MCU is waking up from VLLSx, code can implement a software flag prior to clearing PMC_REGSC[ACKISO] to retain the wakeup source, if required by software.

e7950: LLWU: When exiting from Low Leakage Stop (LLS) mode using the comparator, the comparator ISR is serviced before the LLWU ISR

Description: The comparator's interrupt service routine when exiting from LLS mode is serviced before the LLWU ISR. Clearing the comparator flag in CMPx_SCR clears the corresponding comparator flag in the LLWU_Fx register which may be used to determine wakeup source in the LLWU ISR.

Workaround: Code can implement a software flag in the CMP ISR to retain wakeup source if required by software.

e10527: LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters

Description: When the LPUART transmitter is idle (LPUART_STAT[TC]=1), two break characters may be sent when using LPUART_CTRL[SBK] to send one break character. Even when LUART_CTRL[SBK] is set to 1 and cleared (set to 0) immediately.

Workaround: To queue a single break character via the transmit FIFO, set LPUART_DATA[FRETSC]=1 with data bits LPUART_DATA[T9:T0]=0.

e7986: LPUART: The LPUART_TX pin is tri-stated when the transmitter is disabled

Description: The LPUART transmitter is disabled when the MCU:

- Enters Stop, Wait, or VLPS with the DOZEN bit set
- Enters LLS or VLLS power mode.

The LPUART will tri-state the LPUART_TX pin when the transmitter is disabled, which may result in leakage current.

Workaround: Before the MCU enters Stop, Wait, or VLPS power mode with the DOZEN bit set or enters the LLS or VLLS power mode, enable the pullup resistor on the LPUART_TX pin to ensure the pin does not float. If the TXINV bit is set, enable the pulldown resistor on the LPUART_TX pin.

e7914: PIT: After enabling the Periodic Interrupt Timer (PIT) clock gate, an attempt to immediately enable the PIT module may not be successful.

Description: If a write to the PIT module enable bit (PIT_MCR[MDIS]) occurs within two bus clock cycles of enabling the PIT clock gate in the SIM_CG register, the write will be ignored and the PIT will fail to enable.

Workaround: Insert a read of the PIT_MCR register before writing to the PIT_MCR register. This guarantees a minimum delay of two bus clocks to guarantee the write is not ignored.

e8060: ROM: Bytes sent from host over I2C and SPI interfaces may be lost

Description: Ping packet byte to the I2C and SPI loss occurs occasionally when the target is out of reset.

Workaround: 1.Run the I2C/SPI interface at 48 MHz core clock.

2.Insert a delay of at least 1 ms between the two bytes of the initial ping packet sent from the host to the device

3.If no response from the device is received, the host should re-send the ping packet

e8058: ROM: COP can't be re-enabled in application code due to being disabled by ROM boot code

Description: COP is disabled by ROM boot code,can’t be re-enabled in application code. If the MCU boots up from ROM and then jumps into flash code, the flash code will fail to enable COP again.

Workaround: To use the COP watchdog in an application, write 00b to FOPT[BOOTSRC_SEL] bit to boot from flash out of reset.

e8594: ROM: I2C0_A1 register does not contain the reset default value when MCU boots from ROM

Description: When the MCU boots from ROM, then the I2C0_A1 register will not hold the reset default value (i.e. 0x00) from the ROM boot.

Workaround: Re-initialize the I2C0_A1 register when booting from ROM and when I2C0 is used by applications.

e8595: ROM: ROM read memory command may read the incorrect data back from flash in some cases

Description: When using the ROM Read Memory command to read the same flash address twice, if in the middle of the two consecutive reads, the flash address space content is changed by either a flash erasing or programming command, the second Read Memory command does not return the correct value in flash, and instead returns the same value as the first read. The root cause is that the flash cache is not disabled and retains the previous content of the flash.

Workaround: Use one of two options:

1) Avoid continuous read of the same flash address space twice

2) Invalidate flash cache before second read of the same flash address

e10358: SIM: A reset during system clock divider (SIM_CLKDIV1) update may cause the crossbar switch to stall

Description: If a reset other than power on reset (POR) or a low voltage detect (LVD) occur during the SIM_CLKDIV1 update, the system crossbar switch could be stalled requiring an LVD or POR to recover.

Workaround: Avoid reset events during SIM_CLKDIV1 update and operate at a bus frequency greater than 50 KHz. Reset sources can be inhibited when updating the SIM_CLKDIV1 by:

• Disabling the clock monitor reset, and loss of lock reset if available, and servicing the COP (computer operating properly timer) if it is enabled. A COP timeout period of greater than 2.7 ms must be used.

• The external pin reset can be delayed until after SIM_CLKDIV1 update by enabling the reset pin filter to use the LPO clock by setting RCM_RPFC[RSTFLTSRW] to 0x2. If this filter has already been enabled it must be disabled and re-enabled immediately before writing the SIM_CLKDIV register.

Once the update to SIM_CLKDIV1 has completed, reset sources can be re-enabled and the reset pin filter can be disabled if desired. To verify the divider has been updated, the SIM_CLKDIV1 register should be read back two times after it was written.

e6396: sLCD: LCD_GCR[RVTRIM] bits are in reverse order

Description: The four bits of LCD_GCR[RVTRIM] are in reverse order, in such a way that the LSB corresponds to bit 27 and the MSB corresponds to bit 24 of the LCD_GCR. The RVTRIM adjustment from lower voltage to higher voltage does not follow a linear increase in the LCD_GCR[RVTRIM] value. The RVTRIM adjustment should follow this sequence:

0,8,4,12,2,10,6,14,1,9,5,13,3,7,11,15

to achieve a linear increase from lower voltage to higher voltage.

The reset value of this field is still 8, which corresponds to a low voltage value of the VIREG.

Workaround: You can use a lookup table with the correct order of RVTRIM values for a linear change on the VIREG voltage (contrast). If planning to use a user-selectable contrast, a memory buffer is required to keep track of the logic value of the RVTRIM. When required to increase or decrease the contrast of the LCD, the buffer pointer should be increased or decreased accordingly and the corresponding value from the lookup table should be written to the LCD_GCR[RVTRIM].

To avoid a low voltage on VIREG after reset, LCD_GCR[RVTRIM] must be updated during the LCD initialization routine.

e2580: UART: Start bit sampling not compliant with LIN 2.1 specification

Description: The LIN 2.1 specification states that start bits should be checked at sample 7, 8, 9, and 10. The UART module checks the start bit at samples 3, 5, and 7 instead.

Workaround: Start bits longer than 5/16 of a bit time are guaranteed to be recognized. Start bits shorter than this should not be used with this version of the UART because they might not be recognized.

e7857: UART: WT timer in T=0 mode and CWT timer in T=1 mode can expire between 0.2 ETU to 0.8 ETU earlier than programmed.

Description: In ISO7816 receive mode, the wait timer (WT) used in T=0 mode and the character wait timer (CWT) used in T=1 mode can expire between 0.2 ETU to 0.8 ETU earlier than programmed. The early expiration of the timers can cause software to discard valid data during communication.

Workaround: To minimize the possibility of discarded data, in T=0 mode, program the WI counter field for the wait timer as WWT + D *480 ETUs for both receive and transmit.

To minimize the possibility of discarded data, in T=1 mode, program the CWI counter field for the character wait timer as CWT + 5 ETUs when receiving and CWT + 4 ETUs when transmitting.

e7919: USBOTG: In certain situations, software updates to the Start of Frame Threshold Register (USBx_SOFTHLD) may lead to an End of Frame error condition

Description: If software updates the Start of Frame Threshold Register (USBx_SOFTHLD) to a value greater than the previous value while the internal SOF countdown counter value is between the previous and updated SOF_THLD value, a new token packet transaction may be initiated, even though it may not complete before the next SOF. This may lead to an End of Frame error condition (CRC5OEF), causing the USB controller to hang.

Workaround: Fix the SOF_THLD to a constant safe or larger value, which is independent of the packet type/ size.

e7822: USBReg: Some devices have VREG_OUT trim value incorrectly programmed

Description: After exiting reset, the device loads its programmed VREG_OUT trim value. On devices that have an incorrect trim value, when asserting reset, VREG_OUT will be 3.3V and when reset is de-asserted VREG_OUT will be 3.02V.

Workaround: Program SIM_USBPHYCTL[USB3VOUTTRG]=0b110 to set VREG_OUT equal to 3.3V.

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