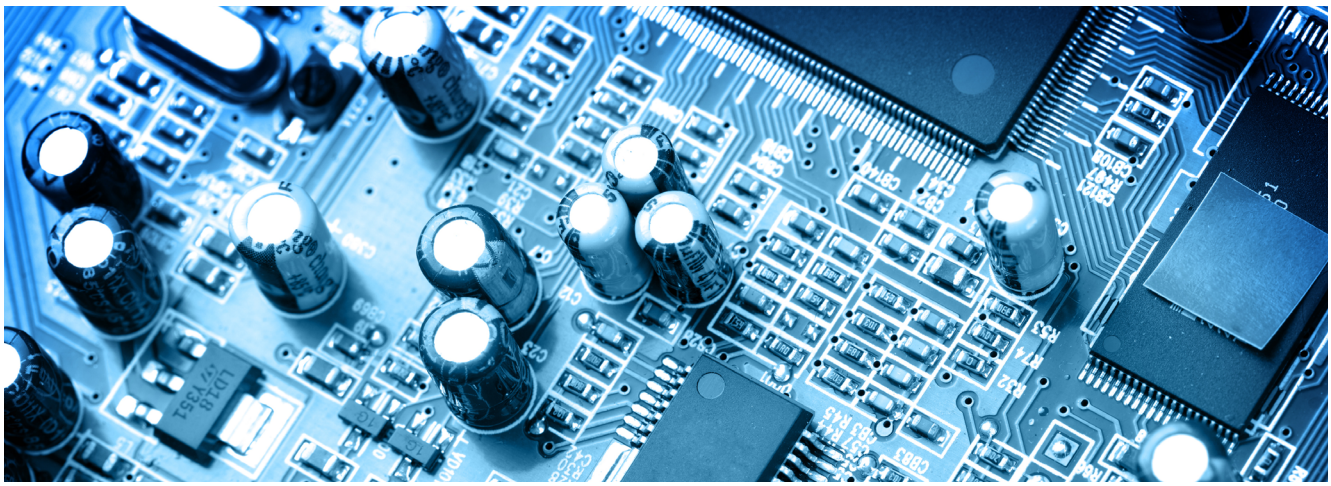
SECURE CONNECTIONS FOR A SMARTER WORLD

FACT SHEET
P3S0200

P3S0200 — I3C SWITCH WITH HARDWARE SELECT AND ENABLE



The P3S0200 is ideally suited for the switching of high-speed I3C-bus signals in computing and server applications, such as servers, workstations, and notebooks that have limited I3C-bus controller ports.

NXP's I3C Switch wide bandwidth of 52 MHz allows signals to pass with minimum edge and phase distortion. The device multiplexes outputs from the I3C controller to one of two corresponding targets with the hardware select pin for 1:2 applications. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs so it can also be used in 2:1 applications. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation required of demanding I3C-bus applications.

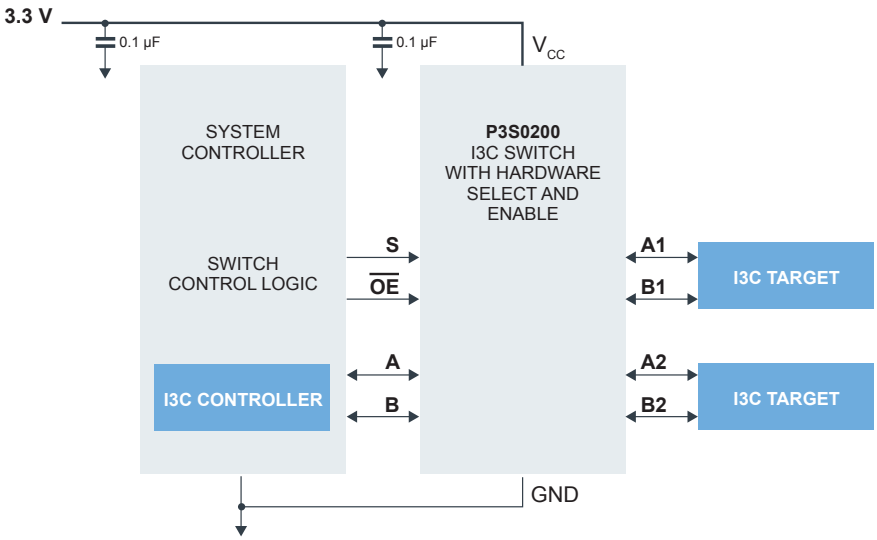
KEY FEATURES

- Easy to Use
  - Can be used at 2:1 or 1:2 mux for both open drain (I^2C-bus) and push pull (I3C-bus) applications
  - Mux with hardware pin enable
- Wide Voltage Level
  - Supports voltage nodes 1.2 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V
  - V_{CC}(A): 2.3 V to 3.6 V
  - Does not support level translation – all nodes are same voltage
- Excellent Operating Specifications
  - ON Resistance — 6 Ω maximum and 0.1 Ω typical mismatch between channels
  - ON Capacitance — 6 pF typical
  - High Bandwidth — 52 MHz typical
- Highly Robust
  - HBM JESD22-A114F Class 3A exceeds 8000 V
  - CDM exceeds 12000 V for I/O to GND protection

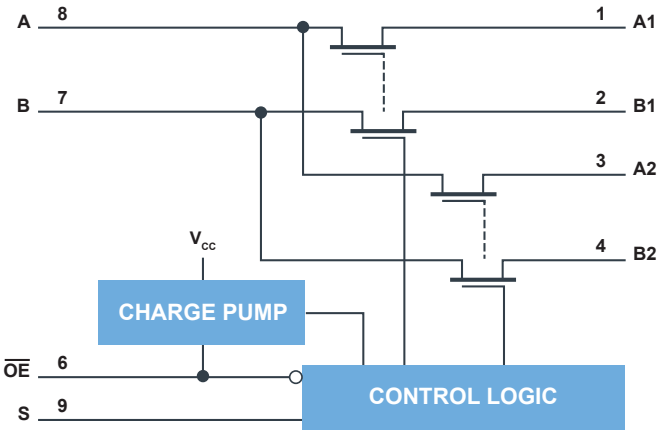
APPLICATIONS

- Easy to Use
- I3C or I^2C 2:1 or 1:2 mux applications
- DDR5 RDIMM for server applications
- Laptops
- Smart phones
- Communications systems

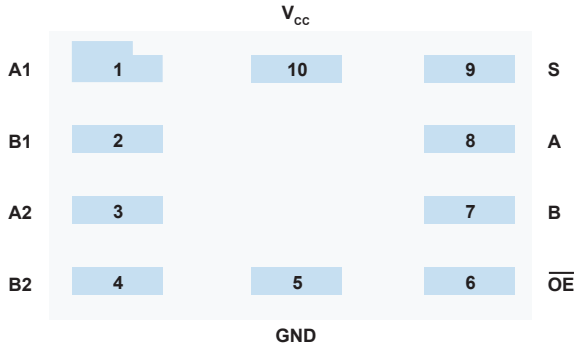
TYPICAL 1:2 APPLICATION (CONTROLLER TO TWO TARGETS)



LOGIC DIAGRAM



PACKAGE DRAWING



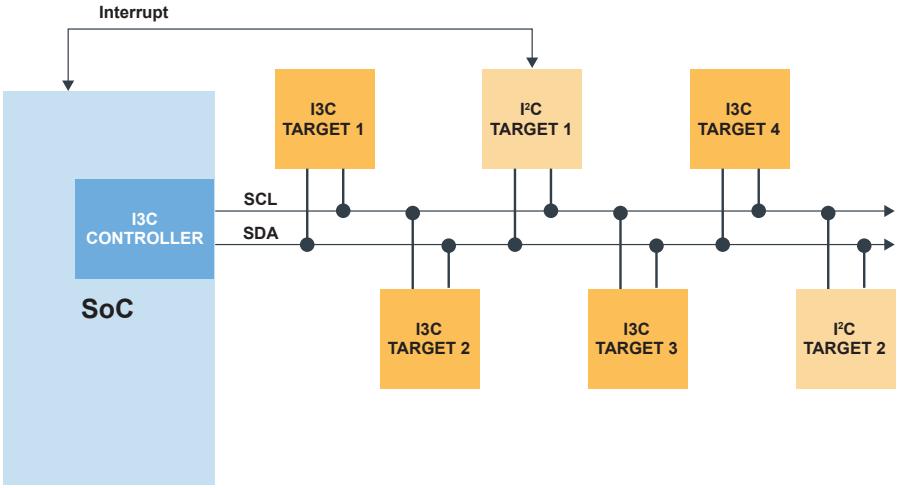
TRANSPARENT TOP VIEW

Orderable Part Number	Package	Pack Method
P3S0200GMX	X2SON8 SOT2015 - 2.0 x 1.5 x 0.5 mm with 0.5 mm pitch	5Ku per 7" tape and reel

WHAT IS MIPI I3C

MIPI I3C (and the publicly available MIPI I3C Basic) provide a scalable, medium-speed, utility and control bus for connecting peripherals to an application processor. Its design incorporates key attributes from both I²C-bus and SPI interfaces to provide a unified, high-performance, low-power interface solution that delivers a flexible upgrade path for I²C-bus and SPI implementers. Originally introduced in 2017, I3C was the culmination of a multi-year development project based on extensive collaboration with the MEMS and Sensors Industry Group and across the broader electronics ecosystem.

As shown in Figure 1, I²C-bus targets (with 50 ns filter) can coexist with I3C controllers operating at 12.5 MHz, enabling the migration of existing I²C-bus designs to the I3C specification. Conversely, I3C targets operating at typical 400 kHz or 1 MHz I²C-bus speeds can coexist with existing I²C-bus controllers.



Just like I²C, I3C is implemented with standard CMOS I/O pins using a two-wire interface, but unlike I²C it supports in-band interrupts enabling target devices to notify controllers of interrupts, a design feature that eliminates the need for a separate general-purpose input/output (GPIO) interrupt for each target, reducing system cost and complexity. Support for dynamic address assignments help minimize pin counts, which is key for accommodating space-constrained form factors.

I3C supports a multi-drop bus that, at 12.5MHz, supports standard data rate (SDR) of 10 Mbps with options for high-data-rate (HDR) modes. The net result is that I3C offers a leap in performance and power efficiency compared with I²C as shown in Figure 2.

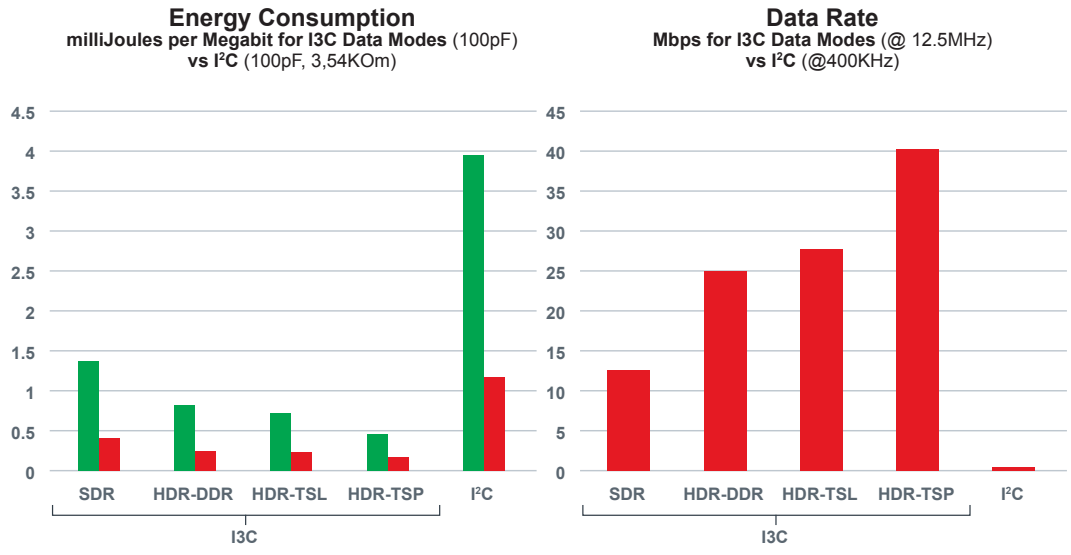


Figure 2 — Comparison of Energy Consumption and Data Rates: I3C vs I²C

Additional technical highlights for I3C include multi-controller support, dynamic addressing, command-code compatibility and a uniform approach for advanced power management features, such as sleep mode. It provides synchronous and asynchronous timestamping to improve the accuracy of applications that fuse signals from various peripherals. It can also batch and transmit data quickly to minimize energy consumption of the host processor.

While the full version of I3C is available only to MIPI Alliance members, MIPI has released a public version called I3C Basic that bundles the most commonly needed I3C features for use by developers and other standards organizations. I3C Basic is available for implementation without MIPI membership and is intended to facilitate a royalty-free licensing environment for all implementers. Figure 3 summarizes the key features supported by I3C and I3C Basic.

To support developers, compatibility between different I3C implementations has been confirmed through multiple interoperability workshops, and several supporting MIPI resources are available. These include:

- I3C Host Controller Interface — MIPI I3C HCI℠
- I3C HCI Driver for Linux
- I3C Discovery and Configuration Specification — DisCo for I3C℠
- I3C Debug and Test Interface — MIPI Debug for I3C℠

I3C intellectual property (IP) is available from multiple vendors, including a licence free version for I3C Basic. I3C conformance testing and verification IP test suites are also available from multiple vendors.

More information on I3C and I3C Basic is available via the MIPI Alliance website.

COMPARISON OF FEATURES			
FEATURE	I3C v1.0	I3C BASIC	I3C v1.1
12.5 MHz SDR (Controller, Targer and I²C Target Compatibility)	✓	✓	✓
Target can operate as I²C device on I²C bus and on I3C bus using HDR modes	✓	✓	✓
Target Reset	✓	✓	✓
Specified 1.2 V – 3.3 V Operation for 50pf C load	✓	✓	✓
In-Band Interrupt (w/MDB)	✓	✓	✓
Dynamic Address Assignment	✓	✓	✓
Error Detection and Recovery	✓	✓	✓
Secondary Controller	✓	✓	✓
Hot-Join Mechanism	✓	✓	✓
Common Command Codes (Required / Optional)	✓	✓ ✓	✓
Specified 1.0 V Operation for 100pt C load	✓	✓	✓
Set Static Address as Dynamic Address CCC (SETAASA)	✓	✓	✓
Synchronous Timing Control	✓	✓	✓
Asynchronous Timing Control (Modes 0-3)	✓	✓	✓
HDR-DDR	✓	✓	✓
HDR-TSL / TSP	✓	✓	✓
HDR-BT (Multi-Lane Bulk Transport)	✓	✓	✓
Grouped Addressing	✓	✓	✓
Device to Device(s) Tunneling	✓	✓	✓
Multi-Lane for Speed (Dual / Quad for SDR and HDR-DDR)	✓	✓	✓
Monitoring Device Early Termination	✓	✓	✓

* Pertains to features that I3C Basic supports

Figure 3 — Comparison of I3C and I3C Basic Features

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