AN12232

QN908x ADC Configuration Guide

Rev. 0.2 — March 2019 Application note

Document information

Info	Content
Keywords	QN908x, BLE, ADC
Abstract	This Application note describes the ADC usage

Revision history

Rev	Date	Description
0.1	2018/08	Initial release
0.2	2019/03	Changed the Application Note name to QN908x ADC Application Note to QN908x ADC Configuration Guide

Contact information

For more information, please visit: http://www.nxp.com

1. Introduction

The Analog Digital Converter (ADC) is a Sigma Delta ADC with CIC filter and decimation filter.

Main Features：

- 23 bits data output, containing 1 sign bit
- Integrated PGA
- 8 external input channels and 3 internal channels for battery monitoring, temperature sensing, offset calibration and random number generation
- Selectable reference voltage from VCC, internal bandgap, or external reference
- Window compare function with interrupt capability
- Supports DMA

2. Input mode

The following will introduce the single mode, differential mode.

Before using the ADC module, the power and clock for ADC should be enabled.

single-ended mode:

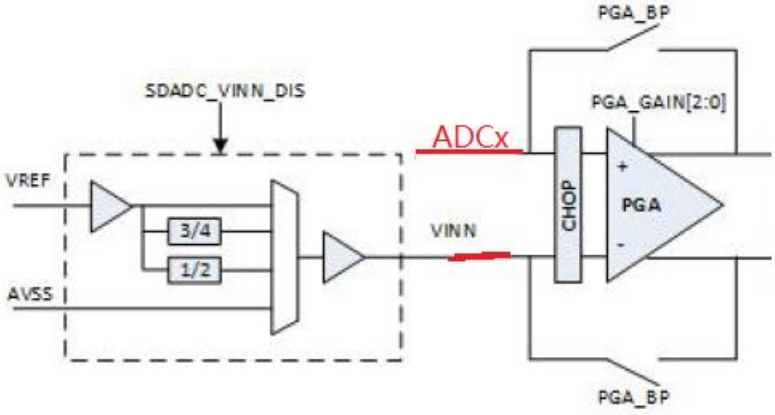

Fig 1. **Single-ended mode**

For single-ended analog input usage, the negative input is connected to an internal voltage, Vinn, which is generated from the ADC reference voltage (Vref) and configurable from Vref, 3/4 Vref, 1/2 Vref or GND.

If PGA_GAIN =1 and ADC_GAIN=1, then the formula for single mode is:
(Vadcx – Vinn) / Vref = RegData / 2^{22} ➔ Vadcx = (RegData / 2^{22}) * Vref + Vinn

Vadcx: Voltage of analog input single from pin
Vinn: Voltage common input, it can be chosen from Vref, 1/2Vref, 3/4Vref and GND.

Vref: Reference voltage, it can be chosen from internal bandgap, VCC and external reference on pin PA07. The internal bandgap voltage store on flash information address(0x210B07F4).
RegData: Read from DATA register.
Measurement range:
ADCx – Vinn range from -Vref to +Vref.
That is -Vref <= (ADCx – Vinn) <= Vref
➔ Vinn - Vref <= ADCx <= (Vinn + Vref)

In addition, Vss <= ADCx <= Vcc.

For example:
Vss = GND
Vcc = 3.0V
Vref = internal bandgap voltage about 1.2V.
Vref Gain = 1.0
GAIN = 1.0
Vinn = 3/4 Vref = 0.9 V

Vinn - Vref <= ADCx <= Vinn + Vref
➔ -0.3 V <= ADCx <= 2.1 V
➔ GND <= ADCx <= 2.1 V

differential mode:

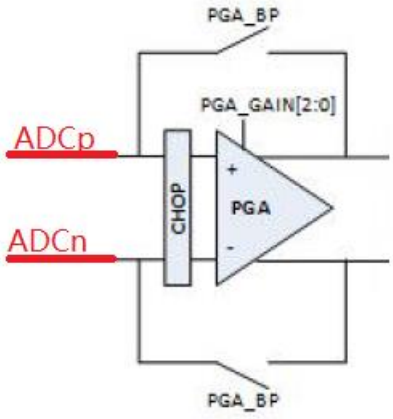

Fig 2. **Differential mode**

The ADC core is a differential ADC. The channels 0~3 are for external differential input. The formula for defferential mode is:

$(Vp – Vn) / Vref = RegData / 2^{22}$ ➔ $Vp – Vn = (RegData / 2^{22}) * Vref$

The Vp – Vn can be either positive or negative depending on which input is at higher voltage.

Vp: Analog input from positive pin

Vn: Analog input from negative pin
Vref: Reference voltage, it can be chosen from internal bandgap, VCC and external reference on pin PA07. The internal bandgap voltage store on flash information address(0x210B07F4).
RegData: Read from DATA register.

3. Output data rate

The output data rate depends on ADC clock and CIC down sample rate.

Output data rate = ADC clock / down sample rate

For example,
the clock is 500 k, which is simply set as
adcConfigStruct.clock = kADC_Clock500 K;
the down sample rate is 256, which is simply set as
adcSdConfigStruct.downSample = kADC_DownSample256;
set the convert mode to Burst convert mode, which is set as
adcConfigStruct.convMode = kADC_ConvModeBurst;
each time the conversion is completed, output a pulse in a GPIO pin, and the following waveform can be obtained.
The output data rate is 500 K / 256 = 1.953 K, it is consistent with the measurement results.

Fig 3. **Output data rate**

4. Conversion modes

The ADC supports multiple conversion modes, which are controlled by register bits CONV_MODE and SCAN_MODE. The following is the conversion process of each mode.

Single mode:

In this mode, ADC performs only one conversion of one channel, and then stops once the conversion is complete.

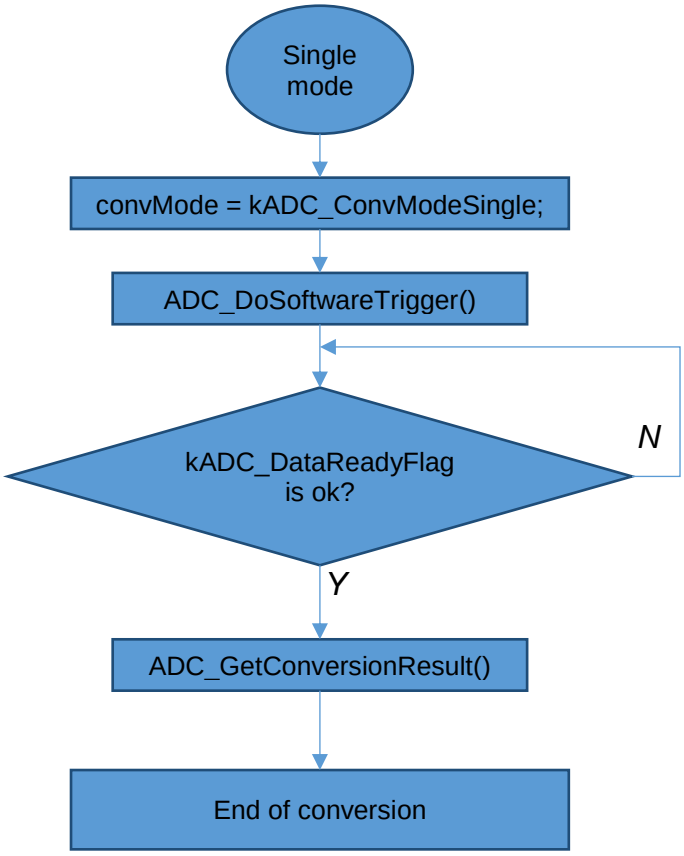

Fig 4. **Flow chart (Single mode)**

Burst mode:

In this mode, ADC will perform successive conversion of one channel, and will not stop until the register bit ENABLE is cleared.

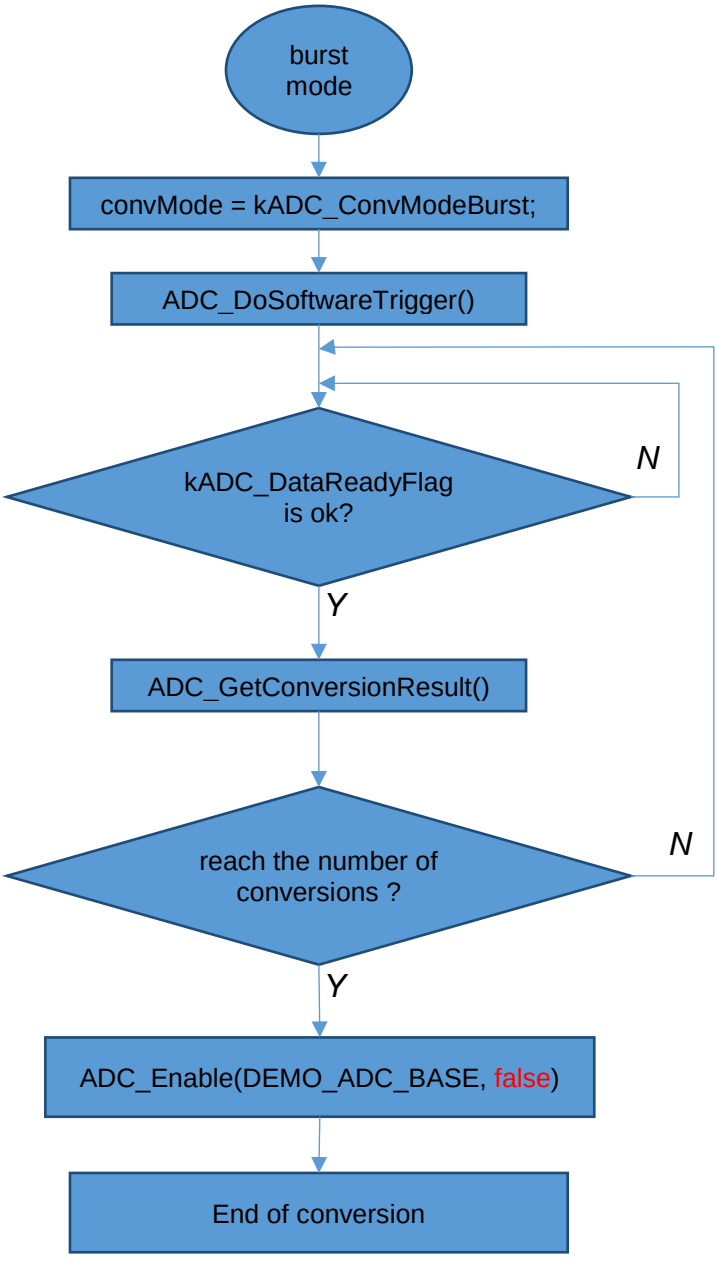

Fig 5. **Flow chart (Burst mode)**

Single scan mode:

In this mode, ADC performs only one conversion of all the selected channels by register CH_SEL. After complete one round of scan of all enabled channels, the ADC will stop automatically.

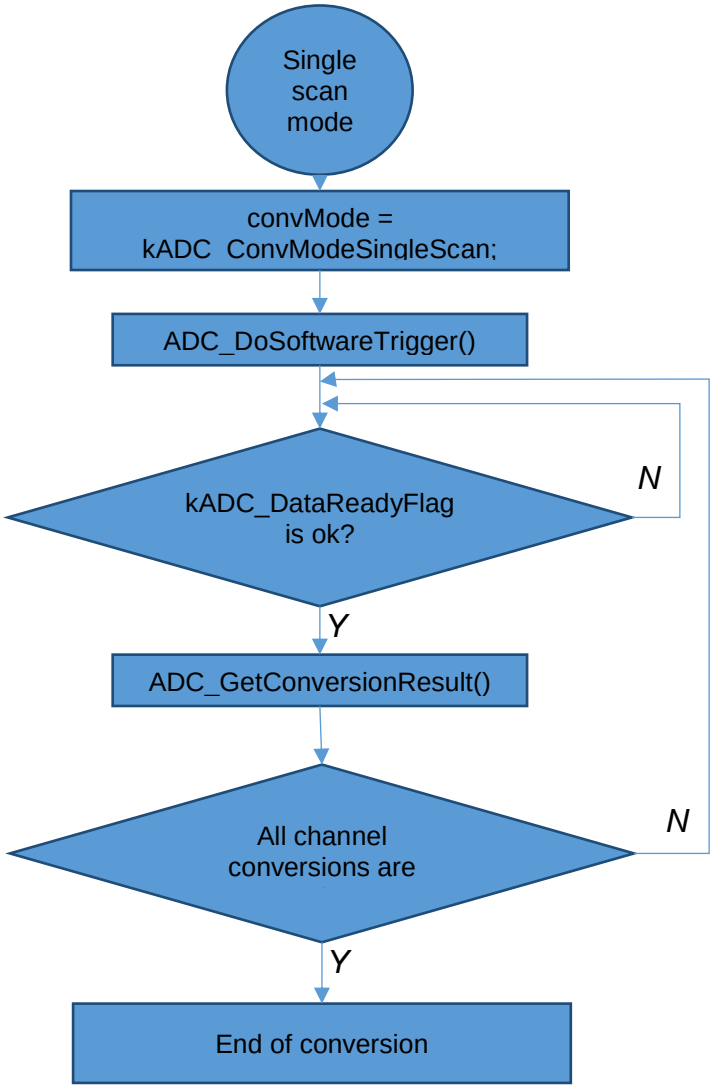

Fig 6. **Flow chart (Single scan mode)**

burst scan mode:

In this mode, ADC will perform successive conversion of all the selected channels by register CH_SEL, and will not stop until the register bit ENABLE is cleared.

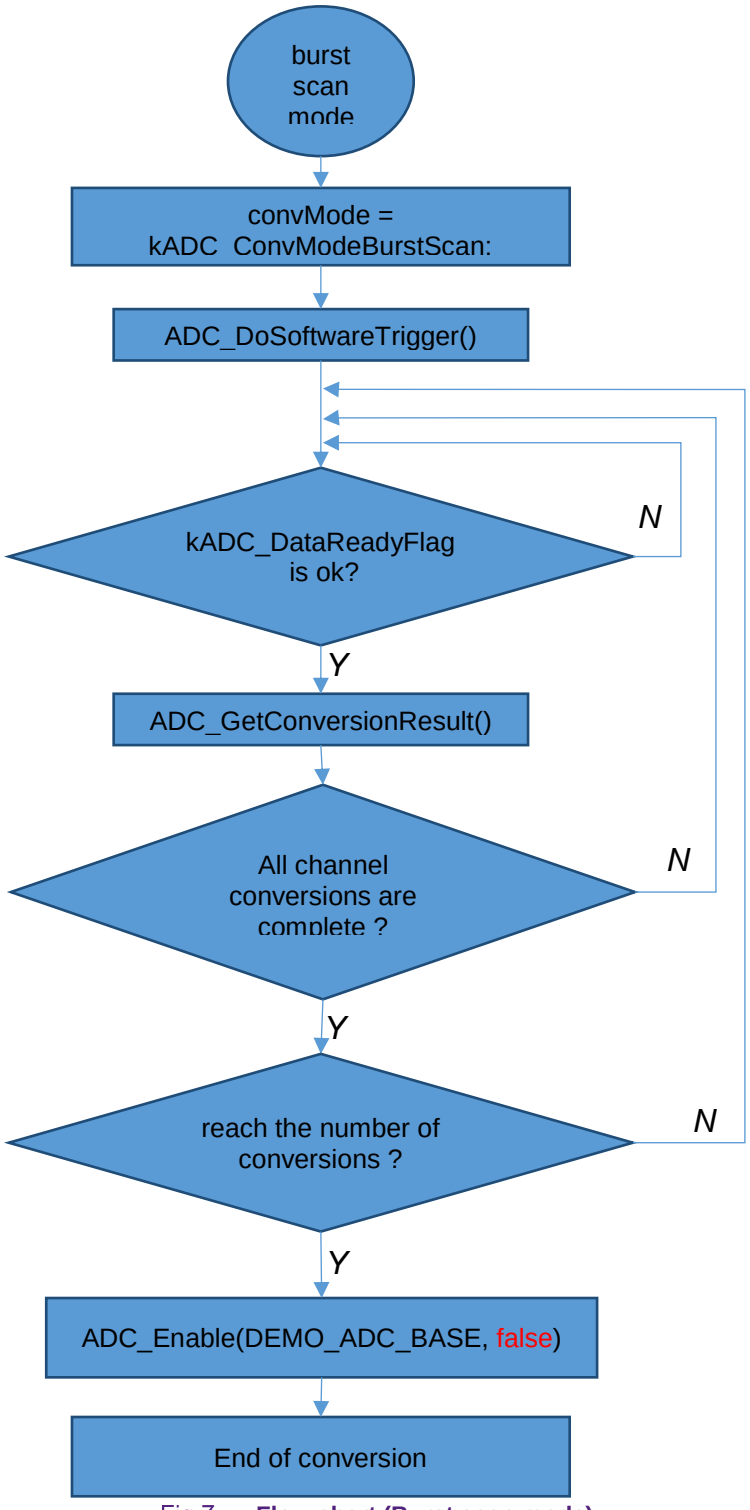

Fig 7. **Flow chart (Burst scan mode)**

5. Cautions

Input Voltage Range:

Input voltage range(VINP-VINN) is either 0.8 * Vref / GAIN at Vref = 1.2 V, or 0.5 * Vref / GAIN at Vref = VCC.
where, GAIN = PGA_GAIN * ADC_GAIN.

If a PGA is enabled, pay attention to output voltage swing limitations of the operational amplifier.
The following figure is a comparison instance of PGA enable and bypass.

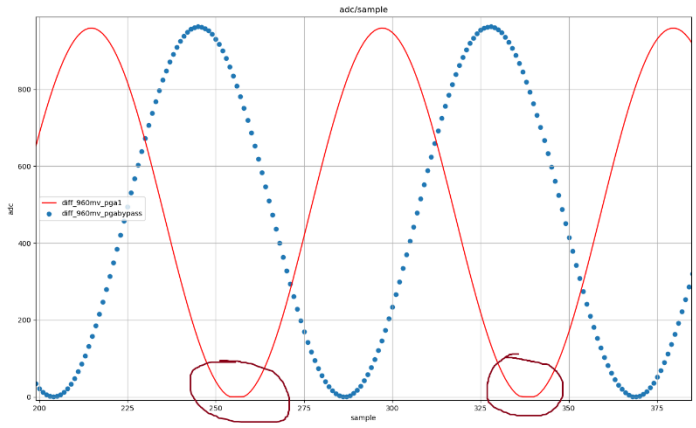

Fig 8. **PGA_GAIN=1 VS PGA_BYPASS**

Sample vs Noise:
According to the Sigma Delta ADC principle, the higher down sample rate, the smaller the noise, as shown in the two figures below.

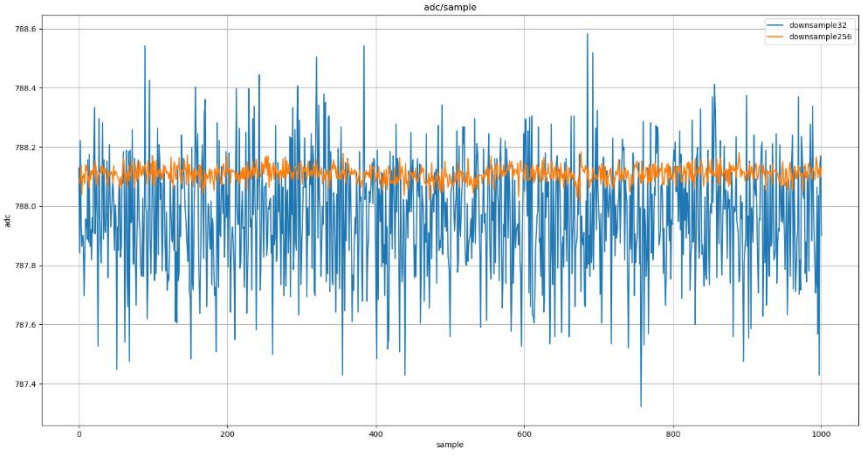

Fig 9. **down sample 32 / down sample 256**

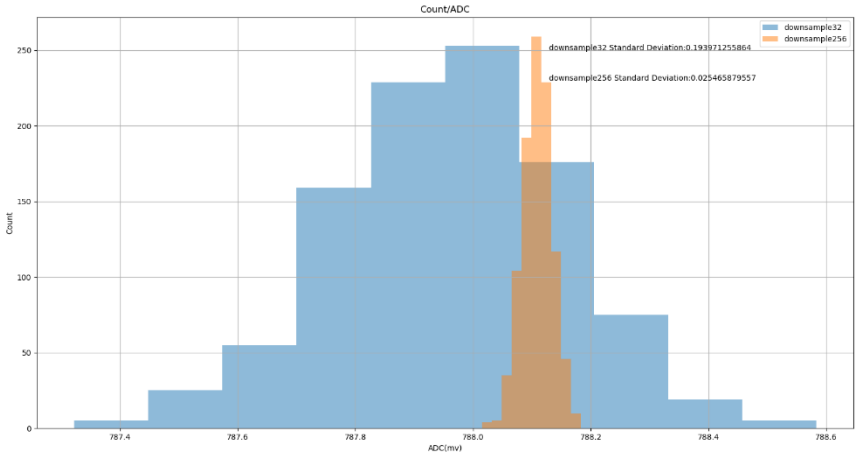

Fig 10. **down sample 32 / down sample 256**

6. Calibration

In order to get the best performance from the ADC two parameters should be calibrated. These parameters are offset and gain.

When the PGA is bypass, the input and output errors of ADC are small, and the customers can choose whether or not to calibrate according to their own system requirements. It can be seen from fig.11 that the measurement value of ADC is the largest deviation of the actual value of 2 mv.

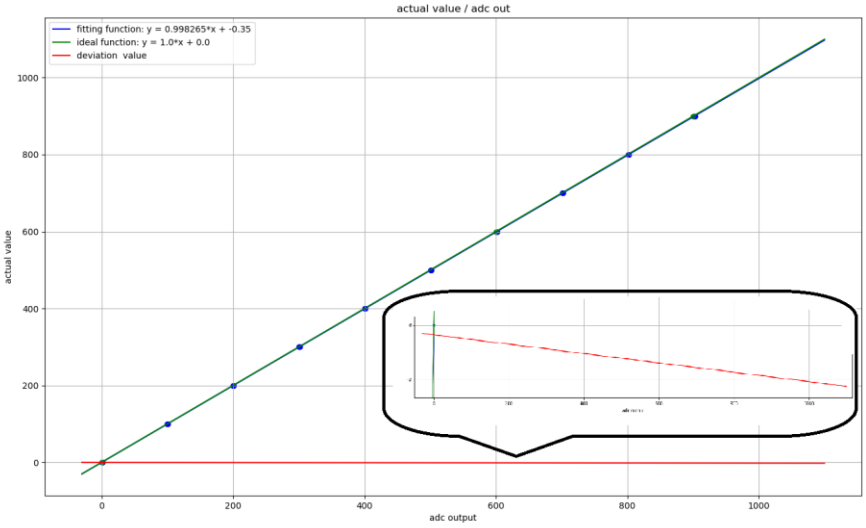

Fig 11. **PAG Bypass**

When the PGA is enable, the input and output errors of ADC gets large, we can do some calibration to correct the error.

The calibration process is as follows:

1) Prepare two accurate voltage output, V1, V2

2) Measure these two voltage points to get ADC output adc1, adc2

3) According to points of (adc1, V1), (adc2, V2), find the function Vy = adcx * a + b

4) The correct voltage value can be calculated by a and b

The figure 12 is a set of test data before calibration, can see that the measured value and the actual value deviation are up to 8 mv. The figure 13 is a set of test data after calibration, the deviation decreased to 0.2 mv.

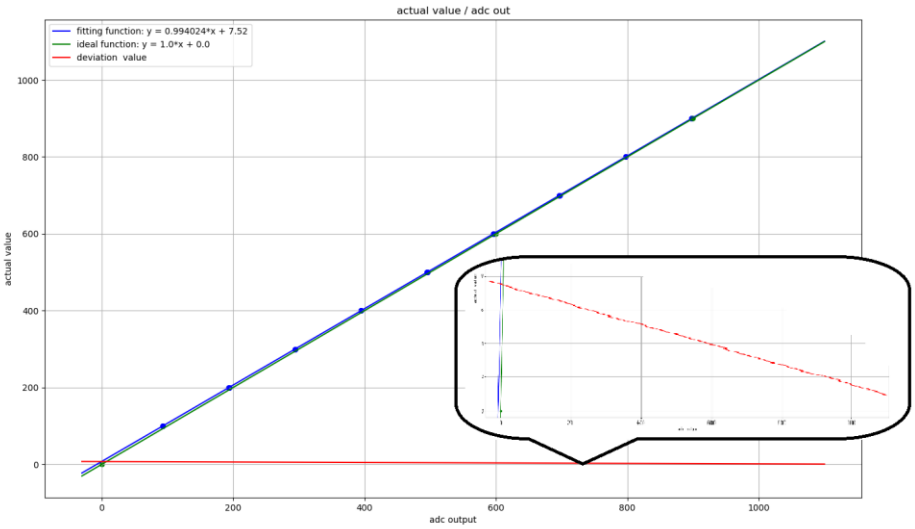

Fig 12. **PAG Gain=1 Before the calibration**

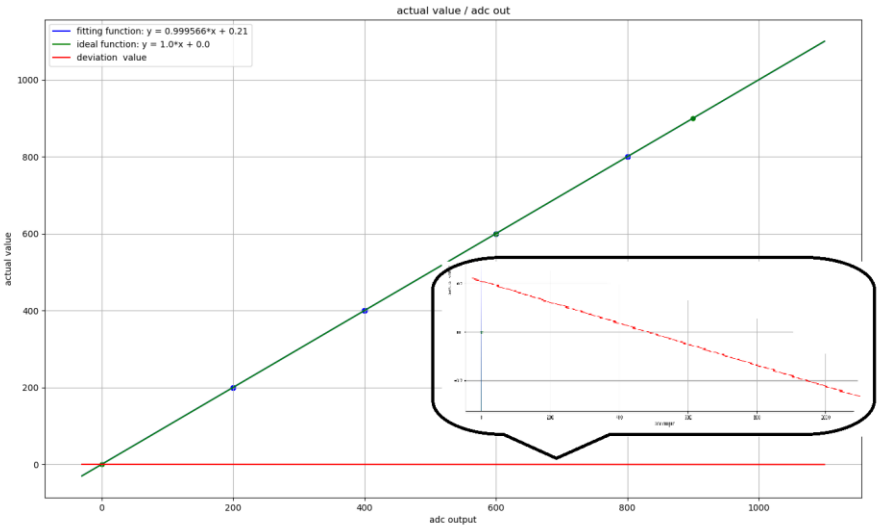

Fig 13. **PAG Gain=1 After the calibration**

7. Temperature measurement

The ADC module has a P-N transistor junction with temperature dependent properties acting as an embedded temperature sensor. The voltage across this junction rises or lowers with temperature allowing silicon to act as a temperature sensor. Figure 14 shows the typical ADC readings(mV) of the temperature sensor output across a range of temperatures.

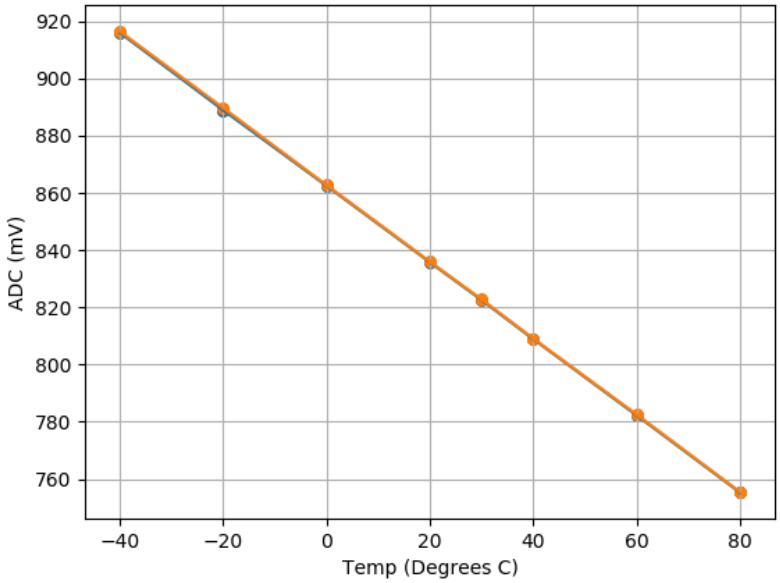

Fig 14. **Typical ADC Temperature Readings**

The graph shows that the temperature sensor output is linear. The temperature sensor output voltage is highest at cold temperatures and lowest at hot temperatures. The readings range from 916d at –40 °C down to 755d at 80 °C. An approximate transfer function demonstrated in the following sections represents this behavior.
Typically, the relation between Temp sensor value (T) vs output voltage V will exhibit this equation:

$$V = -a * T + b$$

where: a and b are constant.

After the test statistics, we fixed slope ‘a’ as ‘coe’;
Through the calibration of a point, that is, we measure the corresponding voltage value of a temperature point in the production phase, and we can obtain a point on the line (T0, offset).
where: T0 is the ambient temperature during the production calibration;
offset is the voltage value of the measured ADC output.

Then the formula above can be deformed:

$$V - offset = (T0 - T) * coe$$

$$T = (offset - V) / coe + T0$$

The value of offset coe and T0 are stored in flash, and detailed information is in the 7.3.1.1 flash information page section of UM11023.
Because the measured temperature is the internal temperature of the chip, it may be affected by the heat dissipation condition of the actual device. The final value of offset will add a correction factor ‘ADC_TEMP_CORRECTION_FACTOR’ in the application.

Table 1. Measurement result shown:

Temperature (℃)	ADC Output (mV)	Temperature Result(℃)	Delta(℃)
-40	916.05	-39.43	0.57
-20	888.925	-19.35	0.65
0	862.48	0.24	0.24
20	835.73	20.05	0.05
40	808.92	39.91	-0.09

60	782.26	59.66	-0.34
80	755.3	79.63	-0.37

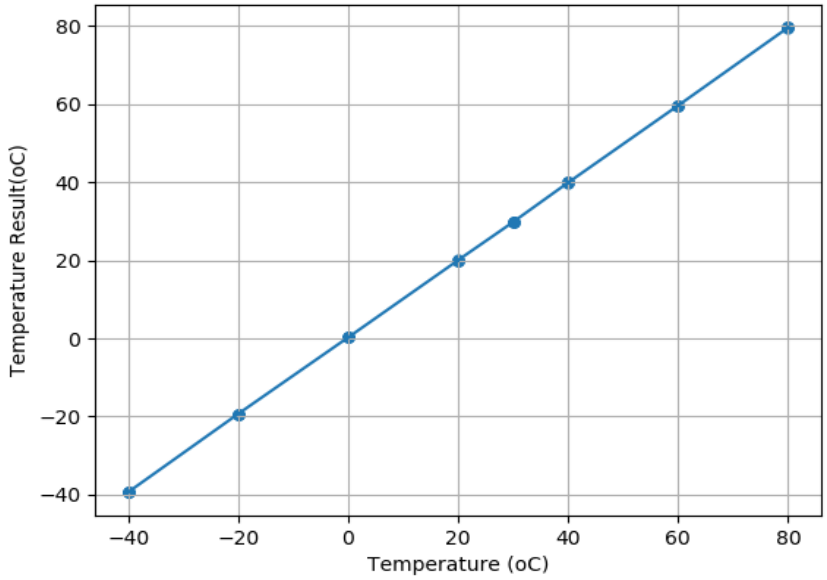

Fig 15. **Temperature Error**

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