Freescale Semiconductor
Product Brief

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MPC8533E Integrated Host Processor Product Brief

The MPC8533E PowerQUICC™ III is a low power high performance embedded processor. The MPC8533E combines capabilities of a computation intensive super-scalar PowerPC™ processor core complex with high performance system peripherals and logic required for networking, communications, and imaging applications.

The MPC8533E is optimized for control and data plane intensive processing applications such as routers, switches, internet access devices, firewall and other packet filtering processors, network attached storage, and storage area networks where the benefits of processing and moving large amounts of data can be leveraged. The integration of vector and double precision floating point processing engines make the MPC8533E ideal for mathematically intensive applications such as printing, imaging, and industrial computing. MPC8533E integrates multi-lane PCI Express, Gigabit Ethernet, and DDR memory controller to increase data bandwidths, reduce valuable board real estate, and lower over-all power consumption.

Contents

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NOTE

The MPC8533E is also available without a security engine, in a configuration known as the MPC8533. All specifications other than those relating to security apply to the MPC8533 exactly as described in this document.

1 Application Examples

The MPC8533E is a very flexible device and can be configured to meet many system application needs. The following section provides block diagrams of various applications.

1.1 Multifunction Printer Application

Figure 1 illustrates an MPC8533E in a multifunction printer application enabled by local bus, PCI Express, PCI, and Ethernet.

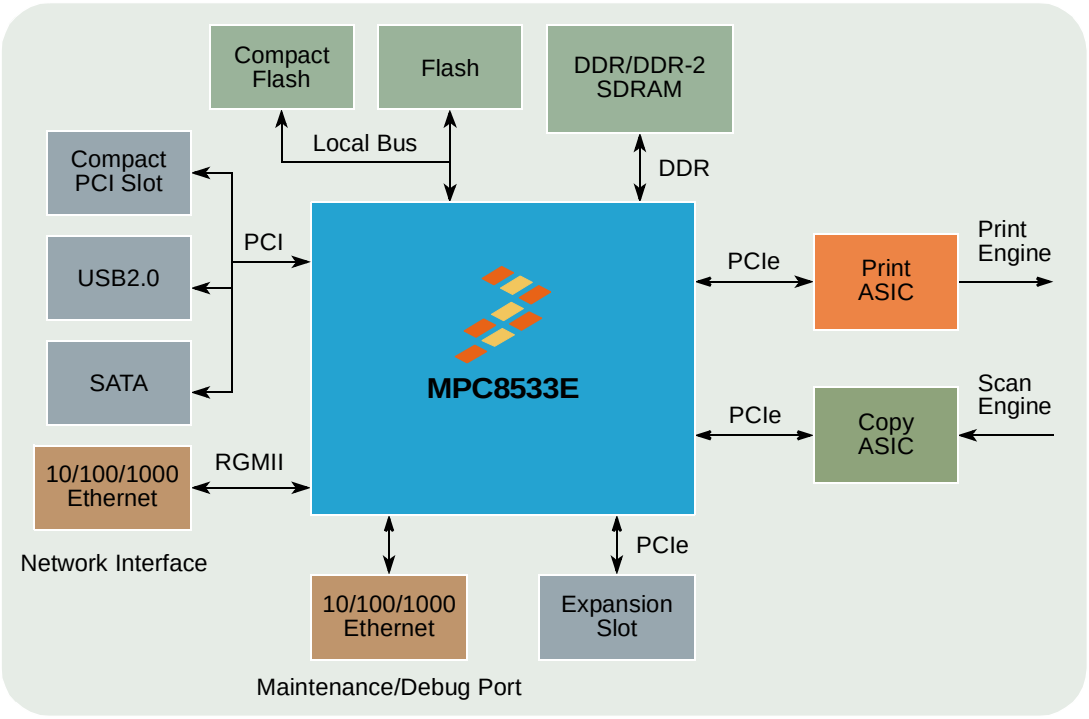

Figure 1. Multifunction Printer Application Enabled by Local Bus, PCI Express, PCI, and Ethernet

1.2 Firewall Appliance

Figure 2 shows an MPC8533E as a small-medium enterprise firewall appliance enabled by local bus, PCI and Ethernet.

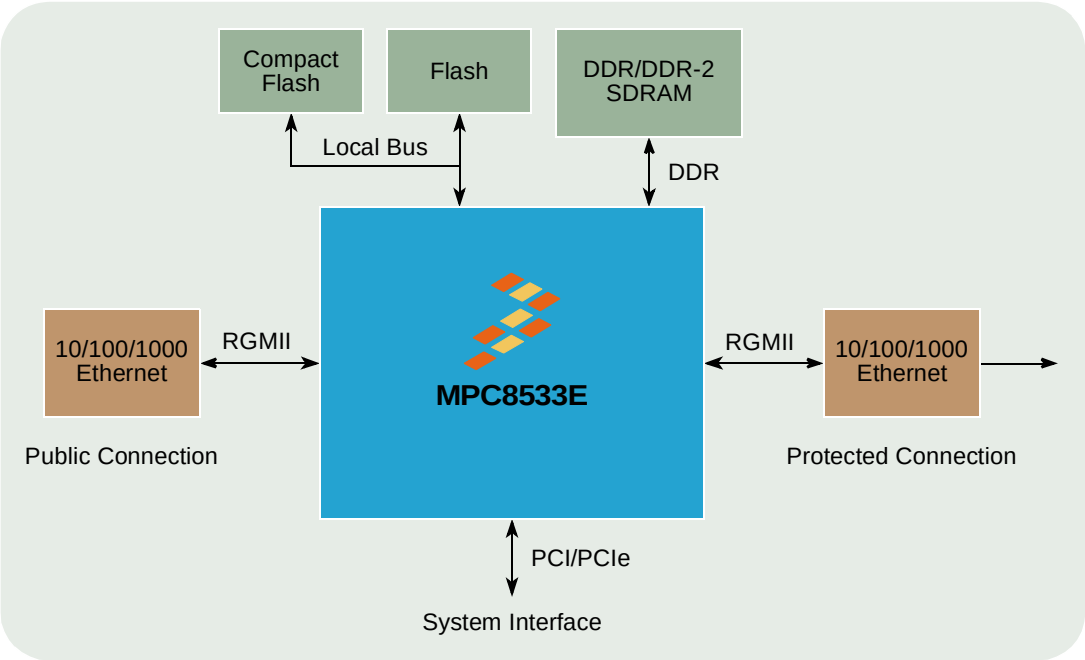

Figure 2. Firewall Appliance Enabled by local bus, PCI, and Ethernet

1.3 Multi-function Router Application

Figure 3 shows an MPC8533E in a multi-function router application enabled by local bus, PCI Express, PCI and Ethernet.

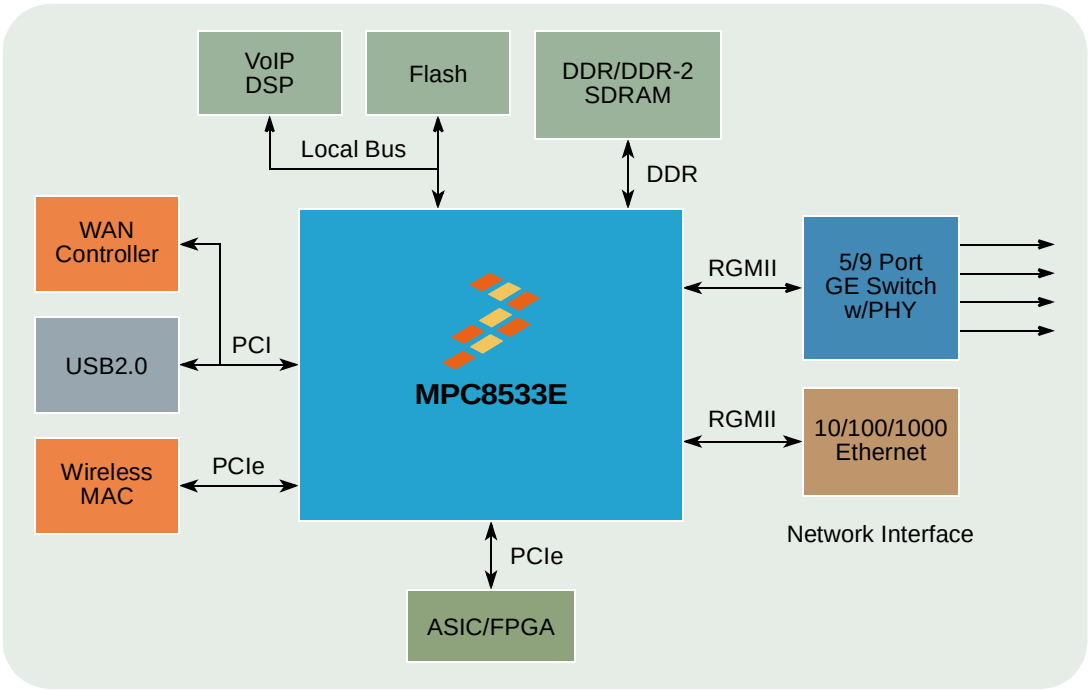

Figure 3. Multi-function Router Application Enabled by local bus, PCI, and Ethernet

1.4 IP SAN Host Bus Adapter

Figure 4 shows the MPC8533E as an IP SAN host bus adapter enabled by local bus, PCI Express, and Ethernet.

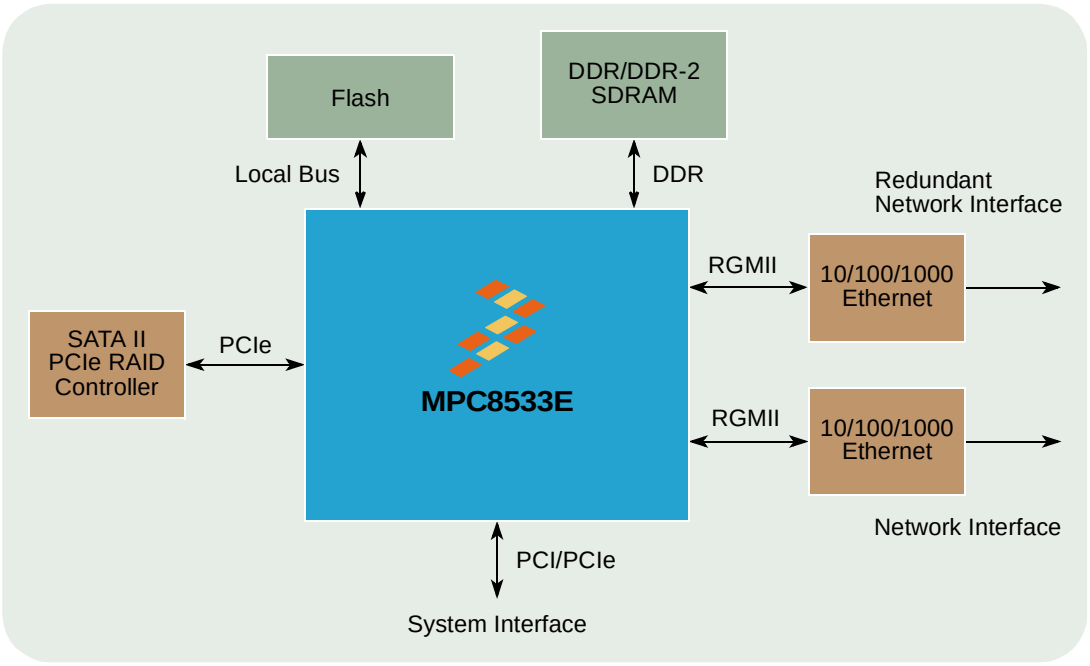

Figure 4. IP SAN Host Bus Adapter enabled by local bus, PCI Express, and Ethernet

1.5 VoIP Aggregation Application

Figure 5 shows MPC8533E in a VoIP aggregation application enabled by local bus and Ethernet.

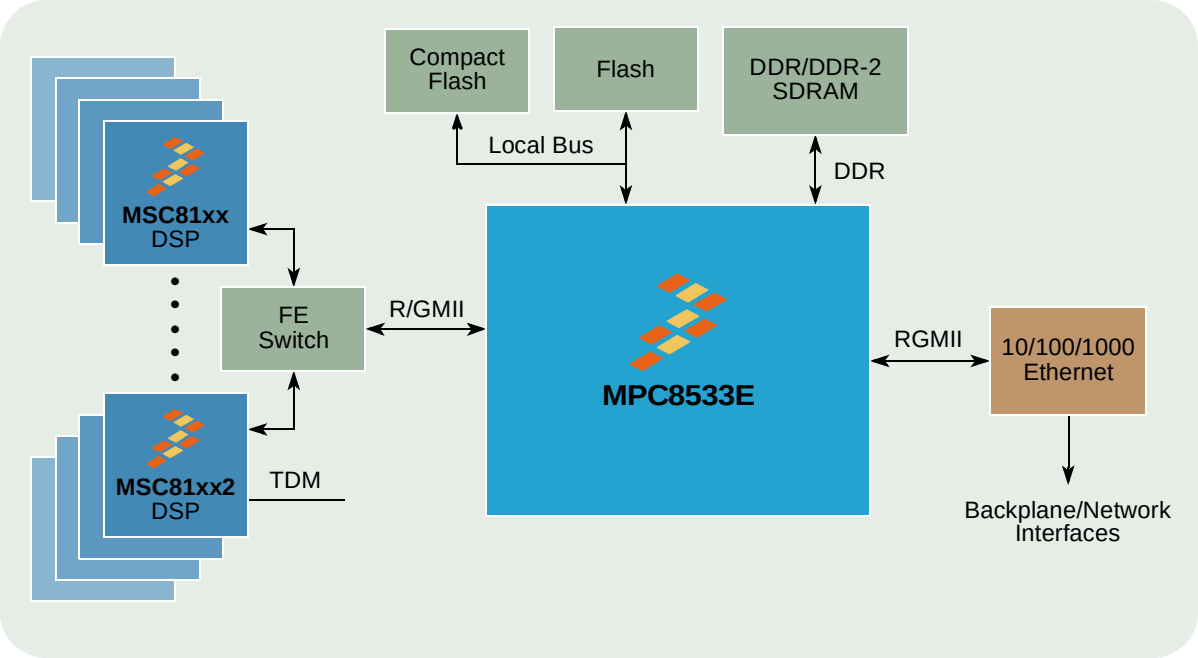

Figure 5. VoIP Aggregation Application Enabled by local bus and Ethernet

2 Features

This section describes the features of the MPC8533E.

2.1 Block Diagram

Figure 6 shows the major functional units within the MPC8533E.

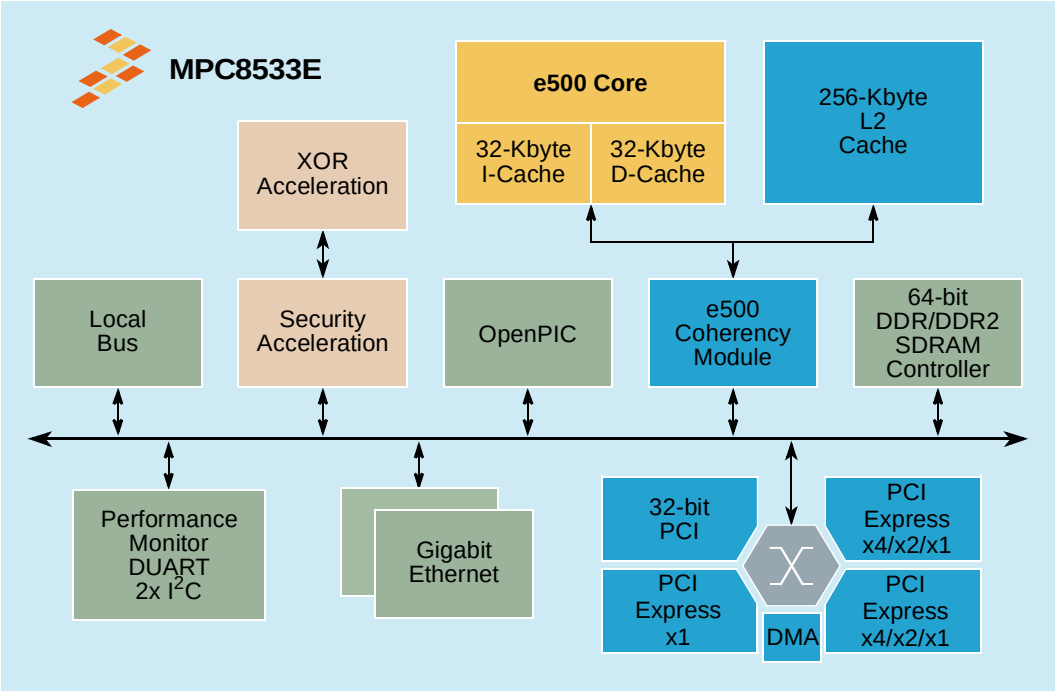

Figure 6. MPC8533E Block Diagram

2.2 Critical Performance Parameters

- Maximum e500 core frequency of 1.066 GHz
- Maximum memory bus frequency of 533 MHz for DDR2 (400 MHz for DDR)
- Supply voltages:
  - Core: 1.0 V
  - PCI Express: 1.0 V
  - PCI: 3.3 V
  - Ethernet: 3.3 or 2.5 V (subject to protocol)
  - Local bus: 3.3, 2.5 V, or 1.8 V
  - DDR: 2.5 V for DDR, 1.8 V for DDR2 (conforms to JEDEC standard)
- Operating junction temperature range is 0–90 degrees C
- Package: 783-pin FC PBGA (flip-chip plastic ball grid array)

2.3 Chip-Level Features

Key features of the MPC8533E include:

- High-performance PowerPC e500v2 core with 36-bit physical addressing
- Separate 32-Kbyte level-1 instruction and data caches; 256 Kbytes of level-2 cache
- Integrated security engine with XOR acceleration
- Two integrated 10/100/1Gb enhanced three-speed Ethernet controllers (eTSECs) with TCP/IP acceleration and classification capabilities
- DDR/DDR2 SDRAM memory controller
- 32-bit PCI controller
- Three PCI Express controllers: Dual x4/x2/x1 interfaces and single x1 interface
- Programmable interrupt controller (PIC)
- Four-channel DMA controller
- Two I^2C controllers
- DUART
- Local bus controller (LBC)
- 16 general-purpose I/O signals (8 dedicated input; 8 dedicated output)

2.4 Module Features

The following sections cover the numerous features of the device in greater detail.

2.4.1 e500 Core and Memory Unit

The MPC8533E contains a high-performance 32-bit Book E–enhanced e500v2 core that implements the PowerPC architecture. In addition to 36-bit physical addressing, this version of the e500 core includes:

- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit general-purpose registers.
- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.

The MPC8533E also contains 256 Kbytes of L2 cache/SRAM, as follows:

- Eight-way set-associative cache organization with 32-byte cache lines
- Flexible configuration (can be configured as part cache, part SRAM)
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- SRAM features include the following:
  - I/O devices access SRAM regions by marking transactions as snoopable (global).
  - Regions can reside at any aligned location in the memory map.
  - Byte-accessible ECC uses read-modify-write transaction accesses for smaller-than-cache-line accesses.

2.4.2 e500 Coherency Module (ECM) and Address Map

The e500 coherency module (ECM) provides a mechanism for I/O-initiated transactions to snoop the bus between the e500 core and the integrated L2 cache in order to maintain coherency across local cacheable memory. It also provides a flexible switch-type structure for core- and I/O-initiated transactions to be routed or dispatched to target modules on the device.

The MPC8533E supports a flexible 36-bit physical address map. Conceptually, the address map consists of local space and external address space. The local address map is supported by ten local access windows that define mapping within the local 36-bit (64-Gbyte) address space.

The MPC8533E can be made part of a larger system address space through the mapping of translation windows. This functionality is included in the address translation and mapping units (ATMUs). Both inbound and outbound translation windows are provided. The ATMUs allows the MPC8533E to be part of larger address maps such as the PCI or PCI Express 64-bit address environment.

2.4.3 Integrated Security Engine (SEC)

NOTE

The features described in this section are available only on the MPC8533E. The MPC8533 does not contain an integrated security engine.

The SEC is a modular and scalable security core optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP. Although it is not a protocol processor, the SEC is designed to perform multi-algorithmic operations (for example, 3DES-HMAC-SHA-1) in a single pass of the data. The version of the SEC used in the MPC8533E is specifically capable of performing single-pass security cryptographic processing for SSL 3.0, SSL 3.1/TLS 1.0, IPSec, SRTP, and 802.11i.

- Compatible with code written for the Freescale MPC8548E, MPC8541E and MPC8555E devices
- XOR engine for parity checking in RAID storage applications.
- Four crypto-channels, each supporting multi-command descriptor chains
- Cryptographic execution units:
  - PKEU—public key execution unit
  - DEU—Data Encryption Standard execution unit
  - AESU—Advanced Encryption Standard unit
  - AFEU—ARC four execution unit
  - MDEU—message digest execution unit
  - KEU—Kasumi execution unit
  - RNG—Random number generator

2.4.4 Enhanced Three-Speed Ethernet Controllers (eTSEC)

Two on-chip enhanced three-speed Ethernet controllers (eTSECs) incorporate a media access control (MAC) sublayer that supports 10 and 100 Mbps and 1 Gbps Ethernet/802.3 networks with MII, RMII,

GMII, RGMII, TBI, and RTBI physical interfaces . The eTSECs include 2 Kbyte receive and 10 Kbyte transmit FIFOs and DMA functions.

The MPC8533E eTSECs support programmable CRC generation and checking, RMON statistics, and jumbo frames of up to 9.6 Kbytes. Frame headers and buffer descriptors (BDs) can be forced into the L2 cache to speed classification or other frame processing. They are designed to comply with IEEE Std. 802.3™, 802.3u™, 802.3x™, 802.3z™, 802.3ac™, 802.3ab™. The BDs are based on the MPC8260 and MPC860T 10/100 Ethernet programming models. Each eTSEC provides hardware support for accelerating TCP/IP packet transmission and reception. By default, TCP/IP acceleration is not enabled and the eTSEC processes frames as pure Ethernet frames, emulating a PowerQUICC III TSEC and allowing existing driver software to be re-used with minimal change. Key features of these controllers include:

- Flexible configuration for multiple PHY interface configurations. Note that to allow maximum flexibility with respect to protocol voltages and software compatibility, the MPC8533E offers two eTSECs numbered, eTSEC1 and eTSEC3. As such, there are no interdependencies between the two eTSEC controllers. The respective base register offsets also correspond to eTSECs 1 and 3 as offered in other PowerQUICC III devices such the MPC8548E.
- Ethernet standard interface capability – TBI, GMII, or MII
- Ethernet reduced interface capability – RTBI, RGMII, or RMII
- 8-bit FIFO interface capability
- TCP/IP acceleration and QoS features:
  - IP v4 and IP v6 header recognition on receive
  - IP v4 header checksum verification and generation
  - TCP and UDP checksum verification and generation
  - Per-packet configurable acceleration
  - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
  - Transmission from up to eight physical queues
  - Reception to up to eight physical queues
- Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex): IEEE Std. 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
- IEEE Std. 802.1 virtual local area network (VLAN) tags and priority
- VLAN insertion and deletion
  - Per-frame VLAN control word or default VLAN for each eTSEC
  - Extracted VLAN control word passed to software separately
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- Wake-on-LAN™ functionality
- MAC address recognition
- Ability to force allocation of header information and buffer descriptors into L2 cache

2.4.5 DDR SDRAM Controller

The MPC8533E supports DDR and DDR2 SDRAM. The memory interface controls main memory accesses and provides for a maximum of 16 Gbytes of main memory.

The MPC8533E supports a variety of SDRAM configurations. SDRAM banks can be built using DIMMs or directly-attached memory devices. Sixteen multiplexed address signals provide for device densities of from 64 Mbits to 4 Gbits. Four chip select signals support up to four banks of memory. The MPC8533E supports bank sizes from 64 Mbytes to 4 Gbytes. Nine column address strobes (MDM[0:8]) are used to provide byte selection for memory bank writes.

The MPC8533E can be configured to retain the currently active SDRAM page for pipelined burst accesses. Page mode support of up to 16 simultaneously open pages (32 for DDR2) can dramatically reduce access latencies for page hits. Depending on the memory system design and timing parameters, using page mode can save 3 to 4 clock cycles from subsequent burst accesses that hit in an active page.

Using ECC, the MPC8533E detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble.

The MPC8533E can invoke a level of system power management by asserting the MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode.

The MPC8533E offers both hardware and software options to support battery-backed main memory. In addition, the DDR controller offers an initialization bypass feature which system designers may use to prevent re-initialization of main memory during system power-on following abnormal shutdown.

2.4.6 PCI Controller

The MPC8533E supports a 32-bit PCI controller that can operate at speeds of up to 133 MHz. Other features include:

- Compatible with *PCI Local Bus Specification, Revision 2.2,* supporting 32- and 64-bit addressing
- Can function as host or agent bridge interface
- As a master, supports read and write operations to PCI memory space, PCI I/O space, and PCI configuration space
- Can generate PCI special-cycle and interrupt-acknowledge commands. As a target, it supports read and write operations to system memory as well as configuration accesses.
- Supports PCI-to-memory and memory-to-PCI streaming, memory prefetching of PCI read accesses, and posting of processor-to-PCI and PCI-to-memory writes
- PCI 3.3-V compatible with selectable hardware-enforced coherency

2.4.7 PCI Express Interface

The MPC8533E supports three PCI Express controllers compliant with the *PCI Express Base Specification Revision 1.0a*. Power-on reset configuration options allow root complex or endpoint functionality.

The physical layers of the PCI Express controllers operate at a 2.5-Gbaud data rate (effective rate of 2 Gbps due to encoding overhead) per lane. Receive and transmit ports operate independently, resulting in an aggregate theoretical bandwidth of 16 Gbps (x4 link).

PCI Express interface features include:

- Two x4/x2/x1 interfaces and one x1 interface
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing and 256-byte maximum payload size
- Full 64-bit decode with 36-bit wide windows

2.4.8 Programmable Interrupt Controller (PIC)

The MPC8533E PIC implements the logic and programming structures of the OpenPIC architecture, providing for external interrupts (with fully nested interrupt delivery), message interrupts, internal-logic driven interrupts, and global high-resolution timers. Up to 16 programmable interrupt priority levels are supported.

The PIC can be bypassed to allow use of an external interrupt controller.

2.4.9 DMA Controller, I^2C, DUART, and Local Bus Controller

The MPC8533E provides an integrated four-channel DMA controller, which can transfer data between any of its I/O or memory ports or between two devices or locations on the same port. The DMA controller also can be used as follows:

- To chain (both extended and direct) through local memory-mapped chain descriptors.
- To handle misaligned transfers, as well as stride transfers and complex transaction chaining.
- To specify local attributes such as snoop and L2 write stashing.

There are two I^2C controllers. These synchronous, multimaster buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. Both the transmitter and receiver support 16-byte FIFOs.

The MPC8533E local bus controller (LBC) port allows connections with a wide variety of external memories, DSPs, and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The user programmable machine (UPM) can be programmed to interface to synchronous devices or custom ASIC interfaces. The SDRAM controller provides access to standard SDRAM. Each chip select can be

configured so that the associated chip interface can be controlled by the GPCM, UPM, or SDRAM controller. All may exist in the same system. The local bus controller supports the following features:

- Multiplexed 32-bit address and data bus operating at up to 166 MHz
- Eight chip selects support eight external slaves
- Up to eight-beat burst transfers
- 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- Three protocol engines available on a per-chip-select basis
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Supports zero-bus-turnaround (ZBT) RAM

3 Developer Environment

The MPC8533E, as a member of the PowerQUICC family and a member of the PowerPC-core-based line of processors, enjoys an extensive, mature development environment. Freescale's own hardware reference designs, models, CodeWarrior™ tools, and board support packages are complemented by a wide range of third party ecosystem offerings, as well as the active engagement of the open source community. Freescale’s internal Developer Technologies organization enables third parties to offer comparable and complementary tools and resources.

MPC8533E boasts a development environment which includes:

- Models and simulators
- Board reference designs
- Comprehensive software development environments
- Debuggers and performance analysis tools
- Toolchains
- Boot loaders
- Operating systems
- Board support packages

4 Document Revision History

Table 1 provides a revision history for this product brief.

Table 1. Revision History

Revision	Location(s)	Substantive Change(s)
Rev. 0		This is the first publicly-released version of this document.

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