

Errata to the MPC866 PowerQUICC User's Manual, Rev. 2

This errata describes corrections the *MPC866 PowerQUICC User's Manual*, Revision 2. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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Section/Page

Changes

14.2.1/14-4

In Table 14-1, “The Input Frequency Requirements,” change “320 MHz” to “400 MHz” as follows:

Table 14-1. The Input Frequency Requirements

| MODCK[1-2] | Frequency In | PDF | MFI, MFN, MFD for DPGDCK |
|------------|---|--|--|
| 00, 01 | OSCM = 10 MHz to 10.66 MHz | 0 | $160 \text{ MHz} < \text{OSCLK} * 2 * (\text{MFI} + (\text{MFN} / (\text{MFD} + 1))) < 400 \text{ MHz}$ |
| 11 | EXTCLK = 10 MHz to 10.66 MHz | 0 | $160 \text{ MHz} < \text{OSCLK} * 2 * (\text{MFI} + (\text{MFN} / (\text{MFD} + 1))) < 400 \text{ MHz}$ |
| 10 | $45 \text{ MHz} \leq \text{EXTCLK} \leq 66 \text{ MHz}$ | $10 \text{ MHz} \leq \text{EXTCLK} / (\text{PDF} + 1) \leq 32 \text{ MHz}$ | $160 \text{ MHz} < \text{OSCLK} * 2 * (\text{MFI} + (\text{MFN} / (\text{MFD} + 1))) / (\text{PDF} + 1) < 400 \text{ MHz}$ |

21.2.4, 20-10

In Table 20-4, “TODR Field Descriptions,” in TOD field description, change “TOD is cleared automatically after one serial clock...” to say “TOD is cleared automatically after 1 system clock...”

21.3, 21-11

Under third bullet point, change “For an RxBD, the value must be even,” to say, “For an RxBD, the value must be mod 4 aligned.”

32.8/32-19

Add a note to beginning of section, as follows: “PIP in transparent mode is not supported.”

H.1.1/H-4

Change the eleventh bulleted feature from “24 general purpose I/O port pins” to “26 general purpose I/O port pins.”

H.2/H-5

Change the note to read:

Note: All PCMCIA Slot B registers are reserved except for PGCRB, which is used to provide OP2 and OP3 functionality.

| | | | | | | | | |
|-------|-------------------------------------|----|----|-----|-----|----|----|----|
| | 0 | 7 | 8 | 15 | | | | |
| Field | — | | — | | | | | |
| Reset | 0000_0000_0000_0000 | | | | | | | |
| R/W | R/W | | | | | | | |
| Addr | (IMMR & 0xFFFF0000) + 0x0E4 (PGCRB) | | | | | | | |
| | 16 | 17 | 18 | 23 | 24 | 25 | 26 | 31 |
| Field | — | — | | OP2 | OP3 | — | | |
| Reset | 0000_0000_0000_0000 | | | | | | | |
| R/W | R/W | | | | | | | |
| Addr | (IMMR & 0xFFFF0000) + 0x0E6 (PGCRB) | | | | | | | |

Figure H-2. PGCRB Register

Table H-1. PGCRB Field Descriptions

| Bits | Name | Description |
|-------|------|--|
| 0–7 | — | Reserved, should be cleared. |
| 8–15 | — | Reserved, should be cleared. |
| 16–17 | — | Reserved, should be cleared. |
| 18–23 | — | Reserved, should be cleared. |
| 24 | OP2 | Writing a zero or a 1 is reflected on the pin. |
| 25 | OP3 | Writing a zero or a 1 is reflected on the pin. |
| 26–31 | — | Reserved, should be cleared. |

H.5/H-7

In Table H-2 (formerly Table H-1), delete second from last row “OP2/MODCK1/STS - OP2 removed”.

Change last row “OP3/MODCK2/DSDO - OP3 removed and DSDO removed.” to “OP3/MODCK2/DSDO - DSDO removed.”

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ARCO Tower 15F
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Japan
0120 191014 or
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support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
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