A2ETYPEBRN_2_5_0
Jan 22, 2010
Rev. 0

ATM to Ethernet Type B Interworking RAM Package Release 2.5.0

General

This release note reflects differences between the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev 3, and the features which are available for this device using the provided microcode RAM packages. The following release note reveals any exceptions to the features which are specified in this release of the specification. The notes describe any addition to the specification or any missing functionality in comparison to the specification.

The user should follow tightly the instructions specified in the QE_Ucode_Loader file provided in the package in relation to the header files containing the code. These instructions assure proper operation and activation of the right features in the code.

Refer to the *QUICC Engine Microcode Errata* for all known issues related to this and other microcode packages.

This package includes the following core blocks: ATM, Ethernet, Interworking, IMA, IP fragmentation, IP Reassembly, and Virtual Port Interworking. Features of these core blocks that are not supported in this package are described in Table 3.

Availability

The package is currently available for the following devices.

Table 1. Package Availability by Device

Device	Loader file name (.h)
MPC8360 rev 2.1	iw_ae_type_b_mpc8360_r2.1.h
MPC8568 rev 1.1	iw_ae_type_b_mpc8568_r1.1.h

Package Content

The tables below designate the content of this package. The baseline is the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev 3. The tables below show additional features and features which are not supported. For the specification of additional features, which are not described in the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev 3, please contact Freescale support. Contact information may be found at www.freescale.com.

Table 2. New Features (which are not Described in QEIWRM, Rev 3)

Feature	Comments
None	

Table 3. Removed Features (Described in QEIWRM, Rev 3 but Not Supported)

Feature	Comments	QEIWRM, Rev 3
LPM PCD		Section 30.3.2.4, “Longest Prefix Match (LPM) PCD”
Header Manipulation for ATM frames which are interworked to CPU		Section 29.2.8.2, “Processing of ATM frames which are Interworked to CPU”
VLAN Specific Header Manipulation Command Descriptor		Section 31.1.11.2, “VLAN Specific Header Manipulation Command Descriptor”
Expanded Hash Table		Section 30.5.3.3.1, “TableLookup_FourWayHash PCD”
ATM AAL5 Multicast		Section 29.2.2.2, “Ethernet to ATM AAL5 Multicast Data Structures”
AAL2 CID MUX		Section 12.3.1.2, “CID Multiplexing”
CAM Emulation lookup table with 2 bytes		Section 30.5.3.1.1, “CAM Emulation Lookup Table (CELUT) for LookupKey Size of 2 Bytes”
IPHCoE		Chapter 31, “Protocol Interworking Programming Model” and Chapter 34, “IPv4/UDP Header Compression”

Revision History

Table 4. Revision History for Release 2.5.0

Release Date: Oct 29, 2009 Revision Register Number: 0xBAE0_B250	
New Features	1. Rate limiter in HES mode support and Per queue Rate limiter. 2. IEEE Standard 1588V2.
Removed Features	None.
Bug Fixes	Policer and PW codes are not invoked when CPU busy condition happened for Copy2CPU frames.
	AAL5 Auto-VC-Off with GBR may abort legal frames.
	Interworking connection statistics TCI counters are not working correctly.
	AAL5 frame based with GBR IW AVCON/AVCF might not work.

Table 5. Revision History for Release 2.4.0

Release Date: Oct 27, 2009 Revision Register Number: 0xBAE0_B240	
New Features	IMA link counters feature for ICP, Filler and User ATM cell counters. See section 26.4.5.4”IMA Link Counters table”, section 26.4.3.1, “IMA Control(IMACNTL)“ and section 26.4.3 “IMA Root Table“
Removed Features	None.
Bug Fixes	None.

Table 6. Revision History for Release 2.3.1

Release Date: Sep 23, 2009 Revision Register Number: 0xBAE0_B231	
New Features	
Removed Features	None.

Table 6. Revision History for Release 2.3.1

Release Date: Sep 23, 2009 Revision Register Number: 0xBAE0_B231	
Bug Fixes	ATM AAL5/AAL2 Interworking Rx Thread management and synchronization mechanism might fail under heavy traffic load conditions. This can lead to MURAM corruption, packet loss, loss of buffers from the buffer pool and/or thread halt.
	In the Ethernet Receiver, a frame with length 1518 is not counted by the etherStatsPkts1024 counter.
	If IW function is enabled (REMODR[IWEn==1]), RSH is not functional. (RSH has to be set to zero).
	Frames received after Generation Violation (and MIN_WRAP seconds have not passed) go through compression instead of being sent as regular frames.
	When using the Data Copy Mode of the Virtual Port and the data buffer sizes of the Virtual Port queue are exact multiples of the data buffer sizes of the Intermediate queue, then memory corruption can occur.
	There are scenarios where LPM leads to a wrong match.
	In IP Reassembly, if the parser BMR is located on the secondary bus, the Ethernet transmitter may not transmit some enqueued frames.
	During IP Reassembly, if the number of allowed fragments received is exceeded, the Ethernet receiver may hang.
	Virtual Port Queues WFQ in mixed mode might skip strict priority queues.
	Possible SDMA error and/or cache coherency problem for Tx BD with length equal to zero. BD with length equal to zero can occur if a Trailer Removal HMCD is applied to a frame for which the removed portion alone is contained within the last BD.
	When enqueue busy or FBP busy conditions are encountered on destination Tx protocol and appropriate interrupts are unmasked, an SDMA and/or cache coherency problem may occur.
	Possible SDMA error and/or cache coherency problem when using the Virtual Port Fast Swap Queue operation mode. Therefore, the Virtual Port Fast swap queue operation mode is not functional.
	Possible Channel loss for ATM APC scheduler when issuing ATM transmit Host Command.
	Eth2ATM with Auto VC On mechanism for GBR internal channel is not working.
	Serial ATM and ATM transmit host command can result with improper operation of the ATM scheduler.

Table 7. Revision History for Release 2.3.0

Release Date: Nov 12, 2008 Revision Register Number: 0xCE00005	
New Features	Added to GCRA VP shaping (GCRA over GCRA) Scheduler the Auto VP on/off mode. (Section 11.2.12.3, GCRA VP Shaping/GCRA over APC or GCRA over GCRA in QEIWRM, Rev 3)
	Virtual Port queues can be completely removed from the scheduler by configuring QueueDisableMask parameter located on VP Global PRAM. (Table 31-3. Virtual Port Global Parameter RAM in the QEIWRM, Rev 3)
Removed Features	None.

Table 7. Revision History for Release 2.3.0 (continued)

Release Date: Nov 12, 2008 Revision Register Number: 0xCE00005	
Bug Fixes	In an Ethernet Rx in heavy traffic (when smoother is disabled) load or in case of an errored frame (CRC, IP Check Sum etc..) and the frame size is less the 128 byte unexpected behavior may occur.
	Using “Add VC” Host command immediately after using any “APC scheduler” Host command might cause data corruption in add VC command.
	In Ethernet IW to ATM when there is an Enqueue BSY condition and AVCON is enabled, the TQDIndex in Enqueue BSY Interrupt Entry is incorrect (filled with AAL2 CC).
	In ATM GCRA scheduler, in the case where there is no Channel Code under one of the GCRA priority levels there is a possibility of wrong ATM traffic shaping.
	Virtual Port Weighted Fair Queuing algorithm implementation has a flaw that could cause starvation in the operating queues if a new queue is added to operation.
	Using IP reassembly where a case of Dynamic LookUp Table busy condition occurs the IPR may hang.
	ATM Interworking in IMA mode can behave unexpectedly in case of a high system load.
	When working in Fast Ethernet Half Duplex and a collision error occurs the port might halt.
	Ethernet receiver can cause unpredictable memory corruption while discarding illegal short frames.
	In IW Eth2AAL2, when AVCON mode is enabled and the TQD is located in external memory wrong behavior may occur.
	In case of IW error interrupt (Ethernet Rx) the attribute status may be faulty.
	Using IP reassembly where a case of Dynamic LookUp Table busy condition occurs the IPR may hang.
	Race condition In ETH2ATM IW function using Auto VC on/off mechanism.
	In a heavily loaded system with IP reassembly the IPR may hang.

Table 7. Revision History for Release 2.3.0 (continued)

Release Date: Nov 12, 2008 Revision Register Number: 0xCE00005	
Bug Fixes	Working with a customized preamble is not supported for frames smaller then 64 bytes.
	Data memory corruption can occur for Ethernet to Virtual Port IW in case Virtual Port does not forward a frame to next IW stage.
	When working in Fast Ethernet Half Duplex and a collision error occurs the port might halt.
	In some cases ATM AAL2/AAL5 Rx working in IW mode can halt. The reason for that is a memory corruption that breaks the threads synchronization linked list. When the list is broken, some threads can go to sleep and will not be woken up. Here is the list of some of the cases. Note that the cases below will not always cause the system to stop—some timing conditions must occur as well: 1. BUSY to CPU 2. BUSY to ENET 3. IW Interrupt queue overflow 4. IW to Virtual Port.
	In Dynamic Lookup table PCD busy flow, the microcode will not reload 2 registers after task switch. Wrong handling of busy event may eventually cause IPR to hang.
	In IPR function, Free queue pool In pointer can be handled by few IPR threads and Automatic learning PCD at the same time without MURAM semaphore mechanism. This might cause IPR queues to disappear from the pool due to no synchronization in returning the queues.

Table 8. Revision History—Revision 2.2.1

Revision 2.2.1	
Bug Fixes	At the Ethernet Tx the Rate limiter dynamic change might have caused the Ethernet Tx to halt.

Table 9. Revision History—Revision 2.2.0

Release 2.2.0	
New Feature	Recirculation to virtual port. Ethernet and ATM can place packets to a Virtual Port queue instead of an output queue. This allows for recirculation of packets through the IW function. See Section 28.2.5, “Ethernet or ATM (AAL5 and AAL2) Recirculation to Virtual Port” of the QEIWRM, Rev 3.
	Added the support of Virtual Port in termination mode. In this mode the CPU can place frames in Virtual Port queues, and the Virtual Port processes them through the IW function and forwards then to an outgoing port. Only swap mode is supported. See Chapter 31, “Virtual Port” of the QEIWRM, Rev 3.
	Added Header Manipulation for ATM frames which are interworked to CPU. See Section 28.2.7.2, “Processing of ATM frames which are Interworked to CPU” of the QEIWRM, Rev 3.
	User can stop dynamically the AAL5 and AAL2 AVCON mechanism by clearing AAL5 IW Unicast TxQD [AVCON] and by setting the IW AAL2 Extension TxQD[AVCON_Dis] bit. User must also set the STPT bit in the TCT.

Table 9. Revision History—Revision 2.2.0 (continued)

Release 2.2.0	
Bug Fixes	When working with Ethernet the LossLess flow control feature can be enabled by mistake and the transmitter may send a flow control frame.
	Copy2CPU option is not allowed. It might cause a halt of the system.
	In interworking the IW Error Interrupt in register IWEMODER has to be masked. {IWEMODER[26]==0).
	In ATM Interworking to Ethernet a memory corruption can occur if MAX_BD3 parameter is equal to one or/and if IWMODER[FwErrCPU] mode is enabled on Interworking Global Parameter RAM.
	When the Ethernet receive is highly loaded with in coming frames it might stop functioning at all. This bug is valid only if the next two conditions take place: 1. More than one thread are enabled. 2. The maximum length of the incoming frames is longer than 4*(VFIFO block size). (VFIFO block size = 128 up to 248). QENET22

Table 10. Revision History—Revision 2.1.2

Release 2.1.2	
New Feature	Ethernet Hierarchical schedule (HES) work conserving mode. Programing model will be released in the next specification document.
Bug Fixes	When AAL2 Timer CU mode is enabled and the TCT[AVCF] mode is also set, the channel might be deleted from the APC table even though the cell is partially full.
	Regarding Frames that belong to an IPR flow; Total byte counter in IW statistics will count only IP packet bytes instead of total length of the frame.
	In interworking, when an Ethernet frame is directed only to a termination queue {Only to CPU} HM is occasionally not supported.
	Regarding Regular frames which belong to an IPR flow; In case of IWAD [FwE] =0 and IWMODER [FwAllCPU] =1, the frames may end in Enet CPU queue instead of IPRQ0.

Table 11. Revision History—Revision 2.1.1

Release 2.1.1	
New Feature	
Bug Fixes	In case of a reassembled frame (IP reassembly) which is directed both to an interworking queue and is forwarded to CPU, a data corruption will occur
	When using hierarchical scheduling with a SQQDs smaller the 64 byte, the Buffer Descriptor base of each queue should be allocated in the address range of: 0x0 to 0x7FFF_FFFF.
	In interworking mode frames which are larger then MAXD1 should be discarded. Actually frames where discarded only when their length was larger then Rounded_MAXD1. Note: Rounded_MAXD1=CEIL(MAXD1/MRBLR)*MRBLR.
	When using HES adding a New LPs (Logic Port) may cause old LPs to stop working for a short while to a complete stop.
	In a heavily loaded system ETH queues which are fragmented may stop transmitting.

Table 12. Revision History—Revision 2.1.0

Release 2.1.0	
New Features	IP reassembly can now support reassembly of up to two out-of-order received fragments. More details about this new feature can be found in the IP reassembly specification. See Chapter 32, “IP Reassembly” in the QEIWRM, Rev 3.
Bug Fixes	The following Ethernet scheduler wrong functionality has been fixed: 1. Long response time for rate limiter changes. 2. Scheduler inaccuracy of up to 6% for different frame lengths and band width rates.
	BMR is undefined in case of DMA semaphore reject for IWF statistics {IWCS}

Table 13. Revision History—Revision 2.0.0

Release 2.0.0	
New Features	Ethernet transmitter hierarchical scheduler. See Section 8.4.17, “Hierarchical Scheduling Support” in the QEIWRM, Rev 3.
	Host commands for re-initializing parameters (dynamic changes) after the first MCC init was already issued (6 commands). See Section 22.3, MCC Commands” in the QEIWRM, Rev 3.
Bug Fixes	Parser events are not set in IP reassembly flow
	IP reassembly may not function properly in heavily loaded system.
	Duplicate ID mode in IP fragmentation is not functional.
	MURAM data corruption may occur when using IP fragmentation.

Table 14. Revision History—Revision 1.1.1

Release 1.1.1	
Bug Fixes	In certain cases IP fragmentation includes L2 FCS field into the last IP fragment.
	Wrong IP identification field in case of fragmentation of a fragment.
	IWCS incremented for Short Frames in Eth Rx when RSH=0.

Table 15. Revision History—Revision 1.1.0

Release 1.1.0	
New Features	IP fragmentation in Ethernet transmitter. See Chapter 8, “UCC Ethernet Controller (UEC)” of the QEIWRM, Rev 3.

Table 16. Revision History—Revision 1.0.1

Release 1.0.1	
New Features	VFIFO block size is configurable. VFIFO block size had a fixed value of 128 bytes in previous releases. Three values are allowed now: 128, 192, and 248. Allowing block sizes beyond 128 bytes enhances the performance, in particular for large packets. See Section 8.8.1, “Init Tx, Init Rx and InitTx and Rx Parameters Command” in the QEIWRM, Rev 3.
Bug Fixes	Ethernet/AAL5 BD write pointer (in TQD) may be corrupted when its most significant byte changes its value.
	IW Thread PRAM address is not loaded(IW_E_ExtPage) when the frame is dropped due to CPU BUSY condition.
	Possible deadlock in Ethernet to XXX interworking in case of BUSY condition and IWCT Index = 0 (No IWCT).
	No transmission in case of odd number of channels for GCRA WRR mode.
	Enet Address classifier PCD (MC/BC) not working.
	IP reassembly does not work properly when using external lookup table.

Table 17. Revision History—Revision 1.0.0

Release 1.0.0	
New Features	Initial release with the new name ‘Type B’. This package is based on the former ‘FULLWIS’ package. This release contains latest files with all known bug fixes.
	CPU bit in Parse & Lookup AD. See Section 29.1.3.1, “Continue Parse and Lookup Action Descriptor (CPL=1)” in QEIWRM, Rev 3.
	Ethernet Address Classifier PCD. See Section 30.3.4.3, “EthernetAddressClassifier_PCD” in QEIWRM, Rev 3.
Bug Fixes	Out of bound addressing WRED param (Average Parameters) in LossLess Flow Control Table.
	IP Reassembly - Fix total length bug and to CPU fix. Also fix offset_in wrap in to CPU and DBM mode.
	Automatic learning - add Copy2CPU feature.
	Virtual Port - IW thread PRAM should be initialized with IF_distributor snum.

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