ATM to Ethernet Type G Interworking RAM Package Release 0.0.1

General

This release note reflects differences between the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev 3, and the features which are available for this device using the provided microcode RAM packages. The following release note reveals any exceptions to the features which are specified in this release of the specification. The notes describe any addition to the specification or any missing functionality in comparison to the specification.

The user should follow tightly the instructions specified in the QE_Ucode_Loader file provided in the package in relation to the header files containing the code. These instructions assure proper operation and activation of the right features in the code.

Refer to the *QUICC Engine Microcode Errata* for all known issues related to this and other microcode packages.

This package includes the following core blocks: ATM, Ethernet, Interworking, IMA and Virtual Port Interworking. Features of these core blocks that are not supported in this package are described in Table 3.

Availability

The package is currently available for the following devices.

Table 1. Package Availability by Device

Device	Loader file name (.h)
MPC8360 rev 2.1	iw_ae_type_g_mpc8360_r2.1.h
MPC8568 rev 1.1	iw_ae_type_g_mpc8568_r1.1.h

Package Content

The tables below designate the content of this package. The baseline is the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev 3. The tables below show additional features and features which are not supported. For the specification of additional features, which are not described in the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev 3, please contact Freescale support. Contact information may be found at www.freescale.com.

Table 2. New Features (which are not Described in QEIWRM, Rev 3)

Feature	Comments
None	None

Table 3. Removed Features (Described in QEIWRM, Rev 3 but Not Supported)

Feature	Comments	QEIWRM, Rev 3
LPM PCD		Section 30.3.2.4, “Longest Prefix Match (LPM) PCD”
VLAN Specific Header Manipulation Command Descriptor		Section 31.1.11.2, “VLAN Specific Header Manipulation Command Descriptor”
Expanded Hash Table		Section 30.5.3.3.1, “TableLookup_FourWayHash PCD”
ATM AAL5 Multicast		Section 29.2.2.2, “Ethernet to ATM AAL5 Multicast Data Structures”
AAL2 CID MUX		Section 12.3.1.2, “CID Multiplexing”
CAM Emulation lookup table with 2 bytes		Section 30.5.3.1.1, “CAM Emulation Lookup Table (CELUT) for LookupKey Size of 2 Bytes”
IPHCoE		In Chapter 31, “Protocol Interworking Programming Model,” and Chapter 34, “IPv4/UDP Header Compression”

Revision History

Table 4. Revision History for Release 0.0.1

Release Date: Sep 23, 2009 Revision Register Number: 0xBAE10001	
New Features	None.
Removed Features	None.
Bug Fixes	ATM AAL5/AAL2 Interworking Rx Thread management and synchronization mechanism might fail under heavy traffic load conditions. This can lead to MURAM corruption, packet loss, loss of buffers from the buffer pool and/or thread halt. .
	Possible SDMA error and/or cache coherency problem for Tx BD with length equal to zero. BD with length equal to zero can occur if a Trailer Removal HMCD is applied to a frame for which the removed portion alone is contained within the last BD.
	When enqueue busy or FBP busy conditions are encountered on destination Tx protocol and appropriate interrupts are unmasked, an SDMA and/or cache coherency problem may occur.
	Possible SDMA error and/or cache coherency problem when using the Virtual Port Fast Swap Queue operation mode. Therefore, the Virtual Port Fast swap queue operation mode is not functional.
	Possible Channel loss for ATM APC scheduler when issuing ATM transmit Host Command.

Table 5. Revision History for Release 0.0.0

Release Date: Jun 30, 2009 Revision Register Number: 0xBAE10000	
New Features	Virtual Port support.
	IP fragmentation in Ethernet transmitter, see Chapter 8, “UCC Ethernet Controller (UEC)” of the QEIWRM, Rev 3.
	Ethernet Hierarchical scheduler (HES) including conserving mode, see Section 8.4.17, “Hierarchical Scheduling Support” in the QEIWRM, Rev 3.
	Ethernet Address Classifier PCD. See Section 30.3.4.3, “EthernetAddressClassifier_PCD” in QEIWRM, Rev 3.
	Recirculation to virtual port. Ethernet and ATM can place packets to a Virtual Port queue instead of an output queue. This allows for recirculation of packets through the IW function. See Section 28.2.5, “Ethernet or ATM (AAL5 and AAL2) Recirculation to Virtual Port” of the QEIWRM, Rev 3
	Added the support of Virtual Port in termination mode. In this mode the CPU can place frames in Virtual Port queues, and the Virtual Port processes them through the IW function and forwards them to an outgoing port. Only swap mode is supported. See Chapter 31, “Virtual Port” of the QEIWRM, Rev 3.
	VFIFO block size is configurable. VFIFO block size had a fixed value of 128 bytes in previous releases. Three values are allowed now: 128, 192, and 248. Allowing block sizes beyond 128 bytes enhances the performance, in particular for large packets. See Section 8.8.1, “Init Tx, Init Rx and InitTx and Rx Parameters Command” in the QEIWRM, Rev 3.
	Added Header Manipulation for ATM frames which are interworked to CPU. See Section 28.2.7.2, “Processing of ATM frames which are Interworked to CPU” of the QEIWRM, Rev 3.
	User can stop dynamically the AAL5 and AAL2 AVCON mechanism by clearing AAL5 IW Unicast TxQD [AVCON] and by setting the IW AAL2 Extension TxQD[AVCON_Dis] bit. User must also set the STPT bit in the TCT.
	Added to GCRA VP shaping (GCRA over GCRA) Scheduler the Auto VP on/off mode. (Section 11.2.12.3, GCRA VP Shaping/GCRA over APC or GCRA over GCRA in QEIWRM, Rev 3)
	Interworking Statistics.
Removed Features	None.

Table 5. Revision History for Release 0.0.0 (continued)

Release Date: Jun 30, 2009 Revision Register Number: 0xBAE10000	
Bug Fixes	Out of bound addressing WRED param (Average Parameters) in LossLess Flow Control Table.
	Ethernet/AAL5 BD write pointer (in TQD) may be corrupted when its most significant byte changes its value.
	IW Thread PRAM address is not loaded(IW_E_ExtPage) when the frame is dropped due to CPU BUSY condition
	Possible deadlock in Ethernet to XXX interworking in case of BUSY condition and IWCT Index = 0 (No IWCT).
	No transmission in case of odd number of channels for GCRA WRR mode
	In interworking mode frames which are larger then MAXD1 should be discarded. Actually frames were discarded only when their length was larger then Rounded_MAXD1. Note: Rounded_MAXD1=CEIL(MAXD1/MRBLR)*MRBLR.
	In a heavily loaded system ETH queues which are fragmented may stop transmitting.
	When AAL2 Timer CU mode is enabled and the TCT[AVCF] mode is also set, the channel might be deleted from the APC table even though the cell is partially full.
	In interworking, when an Ethernet frame is directed only to a termination queue {Only to CPU} HM is occasionally not supported.
	When working with Ethernet the LossLess flow control feature can be enabled by mistake and the transmitter may send a flow control frame.
	In interworking the IW Error Interrupt in register IWEMODER has to be masked. {IWEMODER[26]==0)
	In ATM Interworking to Ethernet a memory corruption can occur if MAX_BD3 parameter is equal to one and/or if IWMODER[FwErrCPU] mode is enabled on Interworking Global Parameter RAM.
	When the Ethernet receive is highly loaded with incoming frames it might stop functioning. This bug is valid only if the next two conditions take place: 1. More than one thread is enabled. 2. The maximum length of the incoming frames is longer than 4*(VFIFO block size). (VFIFO block size = 128 up to 248). QENET22
	At the Ethernet Tx the rate limiter dynamic change might have caused the Ethernet Tx to halt.
	When working in Fast Ethernet Half Duplex and a collision error occurs, the port might halt.
	In some cases ATM AAL2/AAL5 Rx working in IW mode can halt. The reason for that is a memory corruption that breaks the threads synchronization linked list. When the list is broken, some threads can go to sleep and will not be woken up. Here is the list of some of the cases. Note that the cases below will not always cause the system to stop—some timing conditions must occur as well: 1. BUSY to CPU 2. BUSY to ENET 3. IW Interrupt queue overflow 4. IW to Virtual Port.
	Working with a customized preamble is not supported for frames smaller then 64 bytes.
	Race condition In ETH2ATM IW function using Auto VC on/off mechanism.
	ATM Interworking in IMA mode can behave unexpectedly in case of a high system load.

Table 5. Revision History for Release 0.0.0 (continued)

Release Date: Jun 30, 2009 Revision Register Number: 0xBAE10000	
Bug Fixes cont.	When working in Fast Ethernet Half Duplex and a collision error occurs the port might halt.
	Ethernet receiver can cause unpredictable memory corruption while discarding illegal short frames.
	In IW Eth2AAL2, when AVCON mode is enabled and the TQD is located in external memory wrong behavior may occur.
	In case of IW error interrupt (Ethernet Rx) the attribute status may be faulty.
	In an Ethernet Rx in heavy traffic (when smoother is disabled) load or in case of an errored frame (CRC, IP Check Sum etc..) and the frame size is less the 128 byte unexpected behavior may occur.
	Using “Add VC” Host command immediately after using any “APC scheduler” Host command might cause data corruption in add VC command.
	In Ethernet IW to ATM when there is an Enqueue BSY condition and AVCON is enabled, the TQDIndex in Enqueue BSY Interrupt Entry is incorrect (filled with AAL2 CC).
	In ATM GCRA scheduler, in the case where there is no Channel Code under one of the GCRA priority levels there is a possibility of wrong ATM traffic shaping.

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