Ethernet to Ethernet Interworking and POS RAM Package Release 0.0.1

General

This release note reflects differences between the *QUICC Engine™ Block Reference Manual with Protocol Interworking,* QEIWRM, Rev. 3, and the features which are available for this device using the provided microcode RAM packages. This document reveals any exceptions to the features which are specified in this release of the specification. The note also describes additions or missing functionality in comparison to the specification.

The user should follow tightly the instructions specified in the QE_Ucode_Loader file provided in the package in relation to the header files containing the code. These instructions assure proper operation and activation of the right features in the code.

Refer to the *QUICC Engine Microcode Errata* for all known issues related to this and other microcode packages.

This package includes the following core blocks: Ethernet, Interworking, IP reassembly, IP fragmentation, Virtual Port, Hierarchical Scheduling, Longest Prefix Match PCD and POS Multi-PHY termination. Features of these core blocks that are not supported in this package are described in Table 3.

Availability

The package is currently available for the following devices.

Table 1. Package Availability by Device

Device	Loader file name (.h)
MPC8360 rev 2.1	iw_e2e_pos_mpc8360_r2.1.h
MPC8568 rev 1.1	iw_e2e_pos_mpc8568_r1.1.h

Package Content

The tables below designate the content of this package. The baseline is the *QUICC Engine™ Block Reference Manual with Protocol Interworking,* QEIWRM, Rev. 3. The tables below show additional features and features which are not supported. For the specification of additional features, which are not described in the *QUICC Engine™ Block Reference Manual with Protocol Interworking,* QEIWRM, Rev. 3, please contact Freescale support. Contact information may be found at www.freescale.com.

Table 2. New Features (Which are Not Described in QEIWRM, Rev. 3)

Feature	Comments
None	

Table 3. Removed Features (Described in QEIWRM, Rev. 3 but Not Supported)

Feature	Comments	QEIWRM, Rev. 3
ATM Ethernet IW/Termination	This package does not include ATM, Ethernet interworking, or ATM termination.	
PPP Ethernet IW/Termination	This package does not include PPP, Ethernet interworking, or PPP termination.	
Expanded Hash Table		Section 30.5.3.3.1, “TableLookup_FourWayHash PCD”
CAM Emulation Lookup Table (CELUT) for LookupKey Size of 2 Bytes		Section 30.5.3.1.1, “CAM Emulation Lookup Table (CELUT) for LookupKey Size of 2 Bytes”
VLAN Specific Header Manipulation Command Descriptor		Section 31.1.11.2, “VLAN Specific Header Manipulation Command Descriptor”
IP Header Compression / Decompression		Chapter 34, “IPv4/UDP Header Compression”
UCC POS Single PHY Mode		Chapter 13, “UCC POS Controller (UPOS)”
1-2Bytes segmets protection.		Chapter 13, “UCC POS Controller (UPOS)”
Fast Swap and Data Copy modes	Some Virtual Port modes.	Section 32.5.2.2 “Fast Swap Mode” and 32.5.2.3 “Data Copy Mode”

Revision History

Table 4. Revision History for Release 0.0.1

	Release Date: Jan 12, 2010 Revision Register Number: 0xBEE0_E001
New Features	None.
Removed Features	None.
Bug Fixes	Miss ordering between ACK1 and ACK2 in POS TX IDLE/TBNR flow (Errata ID: POS1). The Protocol Error bit (PRE) is not signaled in the RxBD (Errata ID: POS2).

Table 5. Revision History for Release 0.0.0

	Release Date: Oct 12, 2009 Revision Register Number: 0xBEE0_E000
New Features	None. Initial Release.
Removed Features	None. Initial Release.
Bug Fixes	None. Initial Release.

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