ETH2ETHTYPEDRN_1_0_0
Aug 31, 2009
Rev. 2

Ethernet to Ethernet Interworking Type D RAM Package Release 1.0.0

General

This release note reflects differences between the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev. 2, and the features which are available for this device using the provided microcode RAM packages. This document reveals any exceptions to the features which are specified in this release of the specification. The note also describes additions or missing functionality in comparison to the specification.

The user should follow tightly the instructions specified in the QE_Ucode_Loader file provided in the package in relation to the header files containing the code. These instructions assure proper operation and activation of the right features in the code.

Refer to the *QUICC Engine Microcode Errata* for all known issues related to this and other microcode packages.

This package includes the following core blocks: Ethernet, Interworking, Header Compression and Header Decompression, IP fragmentation, Virtual Port, and Longest Prefix Match PCD. Features of these core blocks that are not supported in this package are described in Table 3.

Availability

The package is currently available for the following devices.

Table 1. Package Availability by Device

Device	Loader file name (.h)
MPC8360 rev 2.1	iw_e2e_type_d_mpc8360_r2.1.h
MPC8568 rev 1.1	iw_e2e_type_d_mpc8568_r1.1.h

Package Content

The tables below designate the content of this package. The baseline is the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev. 2. The tables below show additional features and features which are not supported. For the specification of additional features, which are not described in the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev. 2, please contact Freescale support. Contact information may be found at www.freescale.com.

Table 2. New Features (Which are Not Described in QEIWRM, Rev. 2)

Feature	Comments
DF bit checking while interworking to Ethernet with IP fragmentation	IP frames with DF bit set on IP header and violating the MTU configured on Ethernet Tx will be treated as unrecognized frames and dropped according to interworking rules.

Table 3. Removed Features (Described in QEIWRM, Rev. 2 but Not Supported)

Feature	Comments	QEIWRM, Rev. 2
ATM Ethernet IW/Termination	This package does not include ATM, Ethernet interworking, or ATM termination.	
PPP Ethernet IW/Termination	This package does not include PPP, Ethernet interworking, or PPP termination.	
Expanded Hash Table		Section 29.5.3.3.1, “TableLookup_FourWayHash PCD”
CAM Emulation Lookup Table (CELUT) for LookupKey Size of 2 Bytes		Section 29.5.3.1.1, “CAM Emulation Lookup Table (CELUT) for LookupKey Size of 2 Bytes”
VLAN Specific Header Manipulation Command Descriptor		Section 30.1.10.2, “VLAN Specific Header Manipulation Command Descriptor”

Revision History

Table 4. Revision History for Release 1.0.0

	Release Date: Aug 31, 2009 Revision Register Number: 0xBEE0D100
New Features	None
Removed Features	None
Bug Fixes	In the Ethernet Receiver, a frame with length 1518 is not counted by the etherStatsPkts1024 counter.
	If IW function is enabled (REMODR[IWEn==1]), RSH is not functional. (RSH has to be set to zero).
	Frames received after Generation Violation (and MIN_WRAP seconds have not passed) go through compression instead of being sent as regular frames.
	When using the Data Copy Mode of the Virtual Port and the data buffer sizes of the Virtual Port queue are exact multiples of the data buffer sizes of the Intermediate queue, then memory corruption can occur.
	There are scenarios where LPM leads to a wrong match.
	In IP Reassembly, if the parser BMR is located on the secondary bus, the Ethernet transmitter may not transmit some enqueued frames.
	During IP Reassembly, if the number of allowed fragments received is exceeded, the Ethernet receiver may hang.
	Virtual Port Queues WFQ in mixed mode might skip strict priority queues.

Table 5. Revision History—Revision 0.0.2

	Release 0.0.2
New Features	Interworking to Ethernet with IP fragmentation— IP frames with DF bit set on IP header and violating the MTU configured on Ethernet Tx will be treated as unrecognized frames and dropped according to interworking rules.
Bug Fixes	In an Ethernet Rx in heavy traffic (when smoother is disabled) load or in case of an errored frame (CRC, IP Check Sum etc..) and the frame size is less the 128 byte— unexpected behavior may occur.
	When working in Fast Ethernet Half Duplex and a collision error occurs, the port might halt.
	Ethernet receiver can cause unpredictable memory corruption while discarding illegal short frames.
	Working with customized preamble is not supported for frames smaller then 64 bytes.
	When the Ethernet receive is highly loaded with incoming frames it might stop functioning. This bug is valid only if the next two conditions take place: 1. More than one thread is enabled. 2. The maximum length of the incoming frames is longer than 4 × (VFIFO block size). (VFIFO block size = 128 up to 248).

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