PAETYPECRN_1_4_1
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Rev. 0

# PPP and ATM Termination Type C RAM Package Release 1.4.1

## General

This release note reflects differences between the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM. Rev 3, and the features which are available for this device using the provided microcode RAM packages. This document reveals any exceptions to the features which are specified in this release of the specification. The note also describes additions or missing functionality in comparison to the specification.

The user should follow tightly the instructions specified in the QE_Ucode_Loader file provided in the package in relation to the header files containing the code. These instructions assure proper operation and activation of the right features in the code.

Refer to the *QUICC Engine Microcode Errata* for all known issues related to this and other microcode packages.

This package includes the following core blocks: MLMC PPP, PPP Mux, Ethernet, ATM, IMA, and ESS7. This is a termination package, but IW features can be activated for received Ethernet & PPP packets. Features of the core blocks that are not supported in this package are described in Table 3.

## Availability

The package is currently available for the following devices.

**Table 1. Package Availability by Device**

| Device | Loader file name (.h) |
|---|---|
| MPC8360 rev 2.1 | iw_pae_type_c_mpc8360_r2.1.h |
| MPC8568 rev 1.1 | iw_pae_type_c_mpc8568_r1.1.h |

## Package Content

The tables below designate the content of this package. The baseline is *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM. Rev 3. The tables designate additional features and features which are not supported. For the specification of additional features, which are not described in the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM. Rev 3, please contact Freescale support. Contact information may be found at www.freescale.com.

**Table 2. New Features (Which are Not Described in QEIWRM. Rev 3)**

| Feature | Comments |
|---|---|
| None | |

**Table 3. Removed Features (Described in QEIWRM. Rev 3 but Not Supported)**

| Feature | Comments | QEIWRM. Rev 3 |
|---|---|---|
| Expanded Hash Table | | Section 30.5.3.3.1, “TableLookup_FourWayHash PCD” |
| VLAN Specific Header Manipulation Command Descriptor | | Section 31.1.11.2 “VLAN Specific Header Manipulation Command Descriptor” |
| AAL2 CID MUX | | Section 12.3.1.2, “CID Multiplexing” |
| CAM Emulation Lookup Table (CELUT) for LookupKey Size of 2 Bytes | | Section 30.5.3.1.1, “CAM Emulation Lookup Table (CELUT) for LookupKey Size of 2 Bytes” |
| Ethernet Ethernet IW | This package does not include Ethernet Ethernet interworking. | |
| ATM Ethernet IW | This package does not include ATM Ethernet interworking. | |
| PPP Ethernet IW | This package does not include PPP Ethernet interworking. | |
| GCRA VP shaping (GCRA over GCRA) Scheduler the Auto VP on/off mode. | Added to GCRA VP shaping (GCRA over GCRA) Scheduler the Auto VP on/off mode. | Section 11.2.12.3, “GCRA VP Shaping—GCRA over APC or GCRA over GCRA,” |

## Revision History

**Table 4. Revision History for Release 1.4.1**

| Release Date: Jan 22, 2010<br>Revision Register Number: 0xBBA0C141 | |
|---|---|
| **New Features** | None |
| **Removed Features** | None |
| **Bug Fixes** | Possible Channel loss for ATM APC scheduler when issuing ATM transmit Host Command (Errata ID ATM5) |
| | AAL5 Auto-VC-Off with GBR may abort legal frames. (Errata ID ATM7) |
| | CSP mixed mode (both standard and extended CSP used in the same time) not working. (Errata ID MCC1) |
| | OCT and SUERM/EIM interrupts may not be issued in certain cases. (Errata ID MCC3) |

**Table 5. Revision History for Release 1.4.0**

| Release Date: May 4, 2009<br>Revision Register Number: 0xBBA0C140 | |
|---|---|
| **New Features** | ML/MC PPP, Flush WBD Command for flushing the WBD for a given class. This command can be used when the host is interested in limiting the time spent by the fragments the WBD ring.. |
| | Ethernet SNUM Emergency propagation |
| | ML/MC PPP, MRRU & RXFRM counters are now updated in IW mode. |
| | Improved support for ML/MC PPP null fragments: reception of a null fragment now will not assert a fragment loss event; null fragments received for each class are counted. |
| **Removed Features** | None |
| **Bug Fixes** | ML/MC PPP, FBP-RLI indication is not always correct. |
| | Wrong VBR contract shaping in ATM IMA when using APC scheduler. |
| | IEEE1588v2 PTP with VLAN insertion. |
| | In IMA system using the APC scheduler, VBR contract calculation is wrong in the case that the number of active IMA links in IMA group is more then 1 link. |

**Table 6. Revision History—Revision 1.3.0**

| Release 1.3.0, Revision Register Number 0xCEBAC130 | |
|---|---|
| **New Features** | New feature added to ATM MiniCAM function. VPSW Filter mode adds Filtering capabilities to VP switch CAM search. |
| | This package introduces enhancements for PPP Tx bandwidth use optimization. |
| | The number of PPP IW CPU queues were increased from four to eight. |
| **Bug Fixes** | None |

**Table 7. Revision History—Revision 1.2.0**

| Release 1.2.0, Revision Register Number 0xCEBAC120 | |
|---|---|
| **New Features** | Limited IW capabilities were added that allow parse, lookup and forward of the frames to CPU only or reject.<br>It is possible to configure Ethernet and PPP to operate in IW mode but under the following limitations:<br>Parser:<br>• Parser interrupts are not allowed. Meaning that (HIE, MIE, UIE and LIE) must be cleared<br>Ethernet:<br>• IW forwarding to ENET and PPP is not available. Usage of IWAD is not allowed. TAD, PLAD and RAD are the only possible configurations.<br>• No IWCT/HM/IWCS support, meaning that IWCT index on TAD must be zero.<br>PPP:<br>• IW forwarding to ENET is not available. IWAD with FwE=1 is not allowed. IWAD with CPU=1 and FwE=0, PLAD and RAD are the only possible configurations<br>• No IWCT/HM/IWCS support, meaning that IWCT index on IWAD must be zero. |
| **Bug Fixes** | A frame with packet length of 1518 bytes is not counted by EtherStatsPkts1024 counter. This counter should count all frames with a length that is between 1024 and 1518 octets in length inclusive (excluding framing bits but including FCS octets). Therefore EtherStatsPkts1024 counter is not compatible to RFC2819. |
| | Generally speaking an ATM transmit host command blocks the ATM SNUM when the host command task executes. In SAM only mode the SAM microcode jumps to ATM code without going through the scheduler. In this case ATM code can run simultaneously with Tx host command resulting in a wrong ATM scheduling. |

**Table 8. Revision History—Revision 1.1.0**

| Release 1.1.0 | |
|---|---|
| **New Features** | High-speed SS7 links support. |
| | Support for ITU-T Q.703 Annex A, Chinese National SS7 YDT 1125-2001. |
| **Bug Fixes** | In the 1588V2, the Timestamp is presented in little-endian instead of big endian. |
| | ML/MC PPP receiver has a synchronization flaw between the front-end and back-end processes that can cause the loss of received ML fragments. |
| | When working in Fast Ethernet Half Duplex and a collision error occurs the port might halt . |
| | In an Ethernet Rx in heavy traffic (when smoother is disabled) load or in case of an errored frame (CRC, IP Check Sum etc..) and the frame size is less than 128 bytes unexpected behavior may occur. |
| | Ethernet receiver can cause unpredictable memory corruption while discarding illegal short frames. |
| | Working with customized preamble is not supported for frames smaller then 64 bytes. |
| | In ATM GCRA scheduler, in the case that there is no Channel Code under one of the GCRA priority levels there is a possibility of wrong ATM traffic shaping. |
| | When the Ethernet receive is highly loaded with in coming frames it might stop functioning at all.<br>This bug is valid only if the next two conditions take place:<br>1. More than one threads are enabled.<br>2. The maximum length of the incoming frames is longer than 4 × (VFIFO block size). (VFIFO block size = 128 up to 248). QENET22 |

**Table 9. Revision History—Revision 1.0.0**

| Release 1.0.0 | |
|---|---|
| **New Features** | ESS7 functionality was added. |
| | The content of the package was changed. Ethernet to Ethernet interworking was removed. |
| **Bug Fixes** | When working with Ethernet, the LossLess flow control feature can be enabled by mistake and the transmitter may send a flow control frame. |

**Table 10. Revision History—Revision 0.1.1**

| Release 0.1.1 | |
|---|---|
| **New Features** | ML PPP—Adaptive Sequence Number Mechanism. This feature allows the microcode to synchronize on ML traffic in case of a temporary outage on the lines. In case of successful synchronization a special interrupt will be issued. This interrupt can be disabled by setting BMR[DisAdSeqInt] on BPT. |
| **Bug Fixes** | In PPP termination, if the interrupt bit in the TxBD is asserted it might cause memory corruption. |
| | A dynamic change of Ethernet Tx Rate limiter might cause the Ethernet Tx to halt. |
| | Errata of QENET 20 was fixed. In order for it to run properly the TEMODER[6] in the Tx Ethernet global parameter RAM has to be set for the Fast Ethernet Half Duplex UCC and the Tx RMONs have to be enabled and UPSMR[7] bit has to be set. |

**Table 11. Revision History—Revision 0.0.3**

| Release 0.0.3 | |
|---|---|
| **New Features** | none |
| **Bug Fixes** | When the Ethernet receive is highly loaded with in coming frames it might stop functioning at all.<br>This bug is valid only if the next two conditions take place:<br>1. More than one threads are enabled.<br>2. The maximum length of the incoming frames is longer than 4*(VFIFO block size). (VFIFO block size = 128 up to 248). |
| | When using Init_MUX/Init_DeMUX host command it might corrupt the page of anther thread. |

**Table 12. Revision History—Revision 0.0.2**

| Release 0.0.2 | |
|---|---|
| **New Features** | Ethernet Hierarchical schedule (HES) work conserving mode. Programing model would be released in the next specification document |
| | New bit was added in LMR register called RxMLDis which is located at position 4. If set, all frames which contain MLMC PPP PID will be dropped and ILLEGAL FRAME counter under this link will be incremented. |
| **Bug Fixes** | MLMC frame received with length =< 8 Bytes with ACC Error, may result in illegal DMA (Buss Error). |
| | MLMC frame received with length=< (expected header size + FCS) results in illegal DMA (Buss Error). |
| | MLMC frame with header = 9Bytes will result in an unexpected behavior. |
| | MLMC frame received with length =< 8 Bytes after long frame may result in losing the long frame. |
| | When FBPBusy, PRTBusy, Fragment loss conditions occurs, the rest of the MLMC frames arrive for that class will never be enqueued to the PRT. |
| | Copy2CPU option is not allowed. It might cause a halt of the system. |
| | In interworking the IW Error Interrupt in register IWEMODER has to be masked. {IWEMODER[26]==0}. |
| | In interworking, when an Ethernet frame is directed only to a termination queue {Only to CPU}  HM is not supported. |

**Table 13. Revision History—Revision 0.0.1**

| Release 0.0.1 | |
|---|---|
| **New Features** | A mechanism was added in PPP MUX programming model that allows performing a graceful stop of the MUX operation |
| | The maximum number of MUX Tx queues in ML PPP was increased to 32. In addition, a multi-threading mechanism was introduced for PPP MUX operation |

**Table 13. Revision History—Revision 0.0.1 (continued)**

| Release 0.0.1 | |
|---|---|
| **Bug Fixes** | Activating multiple instances of Virtual Port may cause memory corruptions. This mode should not be used. |
| | External request event register width in MPC8568E is 16 bits. Virtual Port uses this event register and the definition assumes 32 bits register (as in MPC8360E). Thus event registers do not function in MPC8568 |
| | The following Ethernet scheduler's wrong functionality has been fixed:<br>1. Long response time for rate limiter changes.<br>2. Scheduler inaccuracy of up to 6% for different frame lengths and band width rates. |
| | A frame which is forwarded from the Virtual Port to the Ethernet Tx port can pass Header Compression. |
| | In interworking, the driver always sets MAXD1 to be identical to Max Frame Length {MFL}. Microcode rounds up MAXD1 to multiples of MRBLR. |
| | In HES mode, adding LP's on Run time may cause other LP's to stop transmitting for a random period of time or stop at all. |

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Freescale Semiconductor Japan Ltd.
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ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
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