Soft UART for MPC8360E R2.1 Microcode Package Release 0.1.2

General

This release note reflects the new features for UART microcode available in the described RAM packages. The packages are available for the QUICC Engine devices MPC8360E Rev2.1. This release note reveals any exceptions to the features which are specified in the reference manual. The notes also describe any additions or any missing functionality in comparison to the reference manual.

Refer to the *QUICC Engine Microcode Errata* for all known issues related to this and other microcode packages.

Availability

Table 1 shows the currently available packages by device.

Table 1. Package Availability by Device

Device	Loader File Name (.h) / C function file name (.c)
MPC8360E rev 2.1	Soft_UART_mpc8360_r2.1.h

Package Content

The UART RAM package includes soft UART microcode. This package was built to solve the UCC UART hardware baud rate tolerance issue as described in the QE_UART6 erratum of the *MPC8360E Chip Errata*.

Revision History

Table 2. Revision History—Revision 0.1.2

	Release 0.1.2
New Features	N/A
Bug Fixes	1. Tx IRQ earlier than transmission complete.

Table 3. Revision History—Revision 0.1.1

	Release 0.1.1
New Features	N/A
Bug Fixes	1. The baud rate tolerance was not in –4%~+4%.
	2. Sending 7-bit BREAK back-to-back failure
	3. Frame error was not reported by QE.
	4. BREAK received unexpectedly when Rx baud rate larger than Tx.

Table 4. Revision History—Revision 0.1.0

	Release 0.1.0
New Features	1. UART Multi-drop functionality.
	2. Update of Shadow UPSMR[CL] description.
	3. Support 5-7 bit character Tx/Rx.
	4. Support 2 stop bits frame.
Bug Fixes	1. PREAMBLE and BREAK size could not be adjusted.
	2. Continuous BREAK couldn’t be received correctly.

Table 5. Revision History—Revision 0.0.0

	Release 0.0.0
New Features	Initial release
Bug Fixes	N/A

Technical Specification

In order to use UART/AHDLC with this patch, the following changes to the programming model need to be applied:

1. **Baud rate configuration:**
   - **Tx Clock x1 Mode:** 2 BRG are required, one for Rx and one for Tx. The UCC receiver's baud rate is set as usual (to x16). The UCC transmitter's baud rate is set to x1.
   - **Tx Clock x16 Mode:** 1 BRG is required for both Rx and Tx. And it should set for x16 baud rate (use if internal loopback is required or if there is a limitation in BRG allocation).
2. **UCC registers configuration extension:**
   - GUMR_L register, set mode=0010 (QMC).
   - Set GUMR_H[17] bit. (UART/AHDLC mode).
   - Set GUMR_H[19–20] (Transparent mode)
   - Clear GUMR_H[26] (RFW).
3. **UCC Parameter RAM configuration extension:**

   Table 8 describes the extension of parameter RAM for soft UART patch. The programming model needs to be applied.

Table 0-6. PRAM Extension Map

Offset	Name	With	Description
0x90	SoftUART_RxShadow_UPSMR	Hword	Shadow Reg for UPSMR
0x92	Reserved	Hword	Initialize to zero.
0x94	SoftUART_RxState	Word	QE internal, initialize to 0x04
0x98	SoftUART_RxCNT	Byte	QE internal, initialize to zero
0x99	Mybrkc	Byte	QE internal, initialize to zero
0x9A	Mytempd	Byte	QE internal, initialize to zero
0x9B	Myuartst	Byte	QE internal, initialize to zero
0x9C	SoftUART_RxChar_length	Byte	initialize to 1+CL+MultidropEN+PEN+1+SL
0x9D	SoftUART_RxBitmark	Byte	QE internal, initialize to 0x7
0X9E	SoftUART_RxTempdlst	Byte	QE internal, initialize to zero
0xA0	SoftUART_TxSpTemp	Word	Temporary tx sp when sending preamble, initialize to zero
0xA4	SoftUART_Sr2Temp	Word	Temp Ser – Receive, initialize to zero
0xA8	R_U_Ptr	Hword	Temp Receive Ucode pointer, initialize to zero
0xAA	T_U_Ptr	Hword	Temp Transmit Ucode pointer, initialize to zero
0xB0	SoftUART_St2Temp	Word	Temp Ser – Transmit, initialize to zero
0xC0	SoftUART_TxFrameRemTMP	Word	QE internal, initialize to zero
0xC4	SoftUART_TxFrameRemTMPSize	Byte	QE internal, initialize to zero

Table 0-6. PRAM Extension Map

Offset	Name	With	Description
0xC5	SoftUART_TxMode_Register	Byte	Protocol type. 0x00 - AHDLC (TX Clock x1 Mode) 0x80 - AHDLC (TX clock x16 Mode) 0x01 - UART (TX Clock x1 Mode) 0x81 - UART (TX Clock x16 Mode)
0xC6	SoftUART_TxState	Byte	QE internal, initialize to zero
0xC7	Reserved	Byte	Initialize to zero
0xC8	SoftUART_Cbrk7Sum	Word	Zero counter for all the 7-bit break chars, initialize to zero.
0xCC	Reserved	Byte	QE internal, initialize to zero
0xCD	TxIrqStatFlag	Byte	QE internal, initialize to zero
0xCE	CntFrmRmSize	Byte	QE internal, initialize to zero
0xCF	CntFrmRmSize2	Byte	QE internal, initialize to zero
0xD0	TxBdLenQ	8 Bytes	QE internal, initialize to zero
0xD8	TxBdLenQStorePtr	Byte	QE internal, initialize to zero
0XD9	TxBdLenQFetchPtr	Byte	QE internal, initialize to zero

4. SoftUART_RxShadow_UPSMR field description:

0	1 2	3	4 5	6	7	8 9	10 11	12	13	14	15
SL	RPM[0–1]	PEN	TPM[0–1]	0	FRZ	UM[0–1]	CL[0–1]]	0	0	0	0

Figure 1. SoftUART_RxShadow_UPSMR Definition

Table 7. SoftUART_RxShadow_UPSMR Field Description

Field	Name	Descriptions
0	SL	Stop length. Selects the number of stop bits the UCC sends. 0 – One stop bit 1 – Two stop bits
1–2, 4–5	RPM , TPM	Receiver/transmitter parity mode. Selects the type of parity check the receiver/transmitter performs; Receive parity errors can be ignored but not disabled. **00** – Odd parity. If a transmitter counts an even number of ones in the data word, it sets the parity bit so an odd number is sent. If a receiver receives an even number, a parity error is reported. **01** – Low parity (space parity). A transmitter sends a zero in the parity bit position. If a receiver does not read a 0 in the parity bit, a parity error is reported. **10** – Even parity. Like odd parity, the transmitter adjusts the parity bit, as necessary, to ensure that the receiver receives an even number of one bits; otherwise, a parity error is reported. **11** – High parity (mark parity). The transmitter sends a one in the parity bit position. If the receiver does not read a 1 in the parity bit, a parity error is reported.

Table 7. SoftUART_RxShadow_UPSMR Field Description

Field	Name	Descriptions
3	PEN	Parity enable. 0 – No parity. 1 – Parity is enabled and determined by the parity mode bits.
6	—	Reserved, should be cleared.
7	FRZ	Freeze transmission. Allows the UART transmitter to pause and later continue from that point. 0 – Normal operation. If the buffer was previously frozen, it resumes transmission from the next character in the same buffer that was frozen. 1 – The UCC completes transmission of the current character and then freezes. After FRZ is cleared, transmission resumes from the next character.
8–9	UM	UART mode. Selects the asynchronous channel protocol. UM can be modified on-the-fly. **00** – Normal UART operation. Multidrop mode is disabled and idle-line wake-up mode is selected. The UART receiver leaves hunt mode by receiving an idle character (all ones). **01** – Manual multidrop mode. An additional address/data bit is sent with each character. The receiver leaves hunt mode when the address/data bit is a one, indicating the received character is an address that all inactive processors must process. The controller receives the address character and writes it to a new buffer. The core then compares the written address with its own address and decides whether to ignore or process subsequent characters. **10** – Reserved **11** – Automatic multidrop mode. The QUICC Engine module compares the address of an incoming address character with UADDRx parameter RAM values; subsequent data is accepted only if a match occurs.
10–11	CL	Character length. Determines the number of data bits in the character, not including optional parity or multidrop address bits. If a character is less than 8 bits, most-significant bits are received as zeros and are ignored when the character is sent. **00** – 5 data bits **01** – 6 data bits **10** – 7 data bits **11** – 8 data bits
12–15	—	Reserved, should be cleared

5. **UART limitations:**
   - RZS – no support
   - Noise – no support
   - Auto baud – no support
   - DRT – no support.
   - Graceful stop host command: No support.
   - Fractional stop bit: No support
   - 5 data bits in normal mode on transmitter: Only 2 stop bits (1-5-0-0-1-1) can support. One stop bit (1-5-0-0-1-0) doesn't support, whatever the RxShadow_UPSMR[SL] bit is set or clear
6. **UART and AHDLC limitations:**
   - Internal loopback supported only in Tx Clock X16 mode.

— Receiver must use 16x over sampling.

— Modem lines flow control (UPSMR[FLC]=1) not supported. CTS should be always asserted. (To assert CTS internally, program the relevant QE I/O as general purpose input).

7. **INIT FLOW:**

1). Program UART/AHDLC according to normal flow as described in the RM, without enabling the UCC (ENT, ENR).

2). Program the new parameters as defined in this release note.

3). Issue Init Rx/Tx params host command through CECR (for transparent protocol) to enable the new mode.

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