TN00009

ADC design guidelines

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Document information

Info	Content
Keywords	ADC design guidelines
Abstract	This technical note provides common best practices for board layout required when Analog circuits (which are sensitive to digital noise) are combined with Digital circuits particularly when high-frequency or high-current circuits are involved

Revision history

Rev	Date	Description
1	20140508	Initial version.

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1. Introduction

The following Design Guidelines provide common best practice for board layout required when Analog circuits (which are sensitive to digital noise) are combined with Digital circuits particularly when high-frequency or high-current circuits are involved.

1.1 Component placement

- Analog circuits should be separated from digital circuits to isolate them from switching noise.
- Noisy and high-frequency components should be located closer to the connectors/power supply.

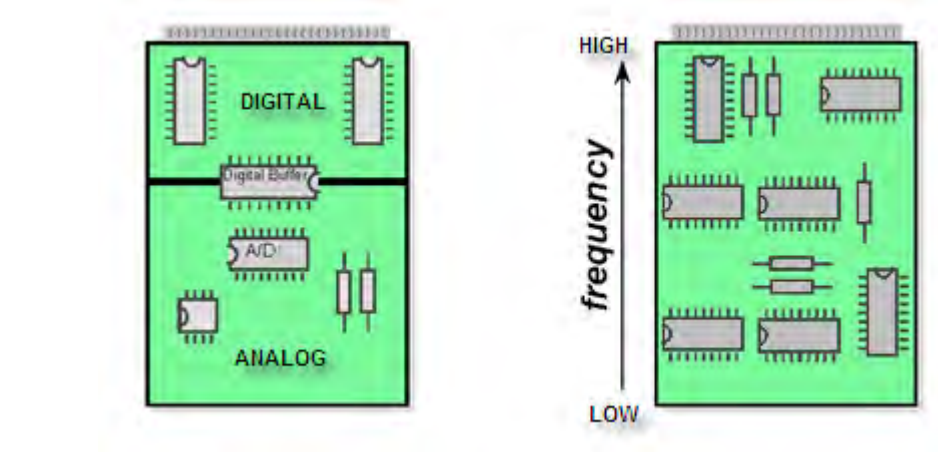

Fig 1. Recommended component placement

1.2 Ground strategy

- Use separate grounds for each domain (analog and digital)
- Use ground planes when possible
- If no ground plane is possible, use a “star” layout strategy for ground connections:
  - Provide independent ground current returns when possible.
  - Return paths can be shared (see U1 & U2) for low current/slow speed signals devices.
  - Make traces as wide as possible (the thinnest width will be the “effective” width for this trace, from this point to the end.
  - Avoid ground loops.
  - Digital currents should not pass across analog devices.
  - High-currents and High-speed currents should not pass across analog and lower speed parts.
  - In all cases, traces should be as short as possible, so effective inductance and resistance is low.

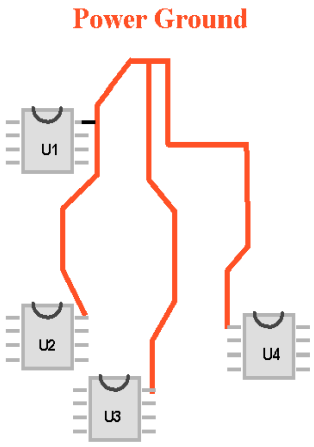

Fig 2. Star grounding layout

- When ground planes are used, use this as a current return path as much as possible.
- Create a separate ground plane for the analog parts, and have both analog and digital ground planes separated with a break.
- Avoid possible loops created between traces for ground return paths on the top-side and the ground plane at the bottom-side of the board.
- In the ground plane, ground currents will flow using the shortest path; if signal traces need to be inserted on the ground plane side of the board, they should be as short as possible and perpendicular to the ground current return paths.
- Even when separate grounds are used for analog and digital domains, only one electrical point should be referred to as the system-wide ground, i.e., both grounds should be connected together at a single point; this is commonly referred to as the chassis. A ferrite bead or inductor would work well for this connection while it will also decouple both circuits.

1.3 Bypass and decoupling capacitors

- A Bypass Capacitor offers a low impedance path to high frequency current flow, reducing the noise current on power supply lines. Usually, a 0.1 uF capacitor will suffice and it should be as close to the device as possible.
- A Decoupling Capacitor provides isolation of two circuits; this will prevent noise from being transmitted from one circuit to the other. It can be used with an inductor, forming a low pass filter. A 10 uF works well in these cases, and it should be connected close to the power supply.

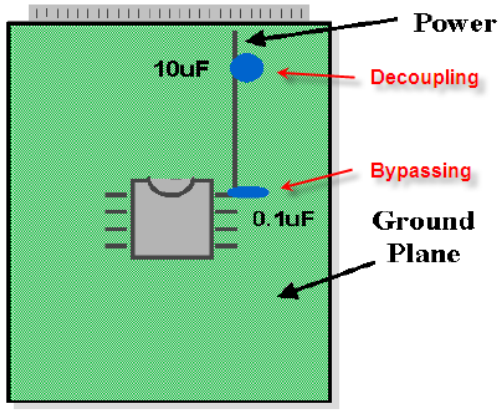

Fig 3. Bypass and decoupling capacitors

1.4 Power planes

- A Power plane is desirable although is not as critical as a ground plane.
- For two-layer boards, the power plane can be replaced by wider traces (two or three times wider than other traces on the board).

1.5 Multi-layer boards

- Critical and/or complex designs would require Multi-Layer boards.
- In this case, it's highly recommended to use different layers for ground and power planes.
- As many components are SMD (Surface Mounted Device), their connections need to be exposed on one of the external sides of the board (usually the top side), so internal layers can be dedicated to the power and ground planes, thus taking advantage from of the distributed capacitance.
- If more than four layers are used, higher speed signals can be shielded between the ground and power planes. Slower signals can be routed on the outer layers.

1.6 Routing signals

- Do not overlap signals/power/ground from different domains (analog and digital). Otherwise, the distributed capacitance between the overlapping portions will couple high-speed digital noise into the analog circuitry.

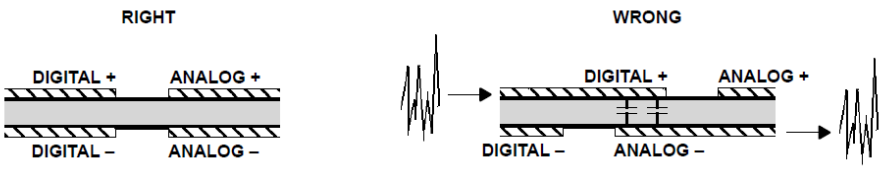

Fig 4. Routing signals

- Keep digital signals (especially high-frequency, noisy I/O or high-current) away from the analog signals. Even small capacitances between traces and planes could couple enough noise, not only for the fundamental frequency but also for the higher harmonics.
- High-impedance lines are the most sensitive to injected noise coupled through capacitance formed with close traces which have fast-changing voltages, such as digital clocks. In order to minimize this capacitance, the distance between the two traces should be increased, and both the length and thickness of the trace should be decreased.

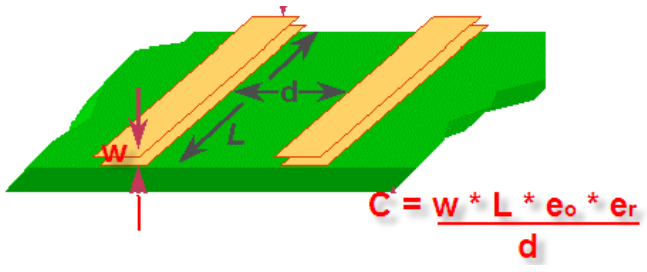

Fig 5. Recommended distance between traces

- Signal traces (in general) should be as short as possible, in order to minimize both parasitic inductance and capacitance.
- Avoid routing signal lines parallel to each other, in order to minimize crosstalk. If this is necessary, keep them separated by a gap of at least three times the signal trace width.
- Minimize loops between power and ground traces (when no ground plane is used), avoiding the “loop antenna” effect.

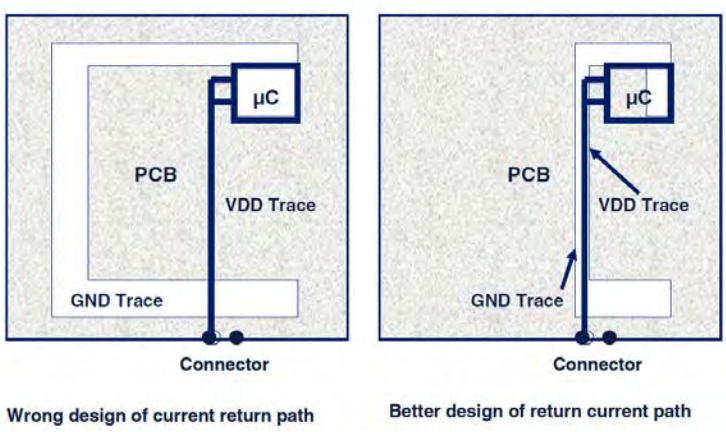

Fig 6. Recommended return current path

- Minimize reflection effect by rounding trace corners.

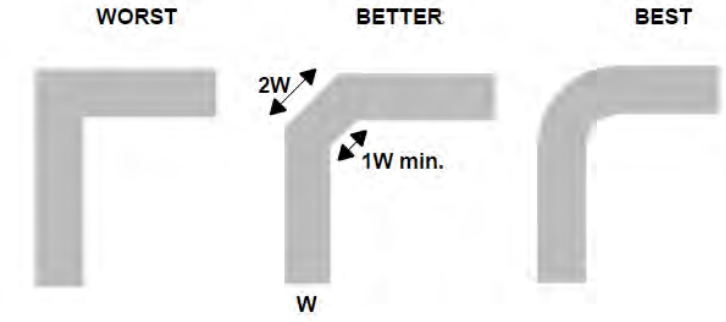

Fig 7. Minimize reflections by rounding the corners

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3. List of figures

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