Comparison of DDRx and SDRAM

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1 Overview

Dynamic random access memory (DRAM) evolved over the years into a synchronous version called synchronous dynamic random access memory (SDRAM). SDRAM has become extremely important because of its densities and relatively fast access times. Together with the improvements in processor speeds, SDRAM memory has now evolved into the state-of-the-art device arrays called double data rate (DDR) SDRAM.

The focus of this white paper is to provide the end user with high level design considerations and/or trade-offs associated with migrating from SDRAM to DDR SDRAM-based designs. For in-depth technical discussions please refer to the published application notes listed in Section 6, “References,” which are available on the Freescale.com website.

DDR SDRAM is a natural migration from PC100 & PC133 SDRAMs to a design that supplies data at a higher rate. DDR SDRAM doubles the data rate by providing data on both the rising and falling edge of a clock cycle.

Note that the consistency in TSOP-II packaging, command/address protocols, and the similarities in the DIMM and connector design between the two approaches allow customers to use existing SDRAM manufacturing infrastructure and testing techniques when migrating to DDR.

2 Typical Applications of DDRx Memories

DDR memory first came on the scene as a high-performance, low-cost memory solution targeted primarily at the personal computer and other cost-sensitive consumer markets. More recently, due to economic pressures squeezing the entire electronics industry, non-consumer products have also begun to incorporate DDR memory as shown in Figure 1. DDR is making major inroads into graphics, networking, servers, image and printing applications, PCs, laptop, and high-end workstations. DDR is well-suited to these applications because it offers the highest performance and has the cost structure to enable it to reach the same price points as current commodity DRAM. Market analysis indicates that DDR is currently used in over 50% of all electronic systems and usage is expected to increase to 80% over the next several years.

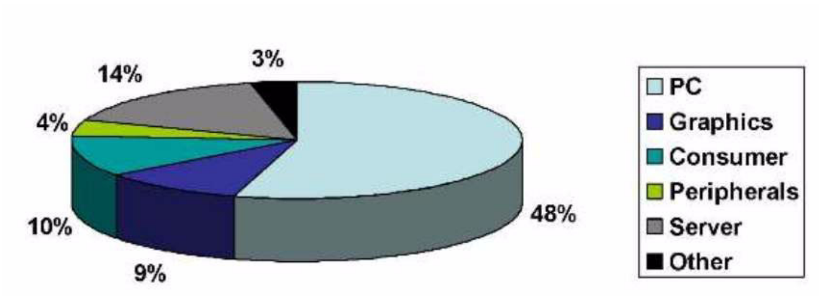

Figure 1. DDR Memory Usage by Application

2.1 Freescale Solutions

Depending upon the customer's application needs, Freescale provides a variety of processor and memory controller solutions. As shown in Figure 2, our evolving road map provides low-cost solutions with increasing performance. The following price-points illustrate examples of this migration.

- MPC8313E: 333 MHz, 16K/16K, DDR2, GigE @ $15.50
- MPC8248E: 333 MHz, 16K/16K, SDRAM, 10/100 @ $22
- MPC859T: 133 MHz, 4KB/4KB, SDRAM, 10/100 @ $26

NOTE

The above price-points are estimated cost in USD for a minimum quantity of 10KU and reflect pricing as of the date of publication of this document.To verify pricing information, go to www.freescale.com.

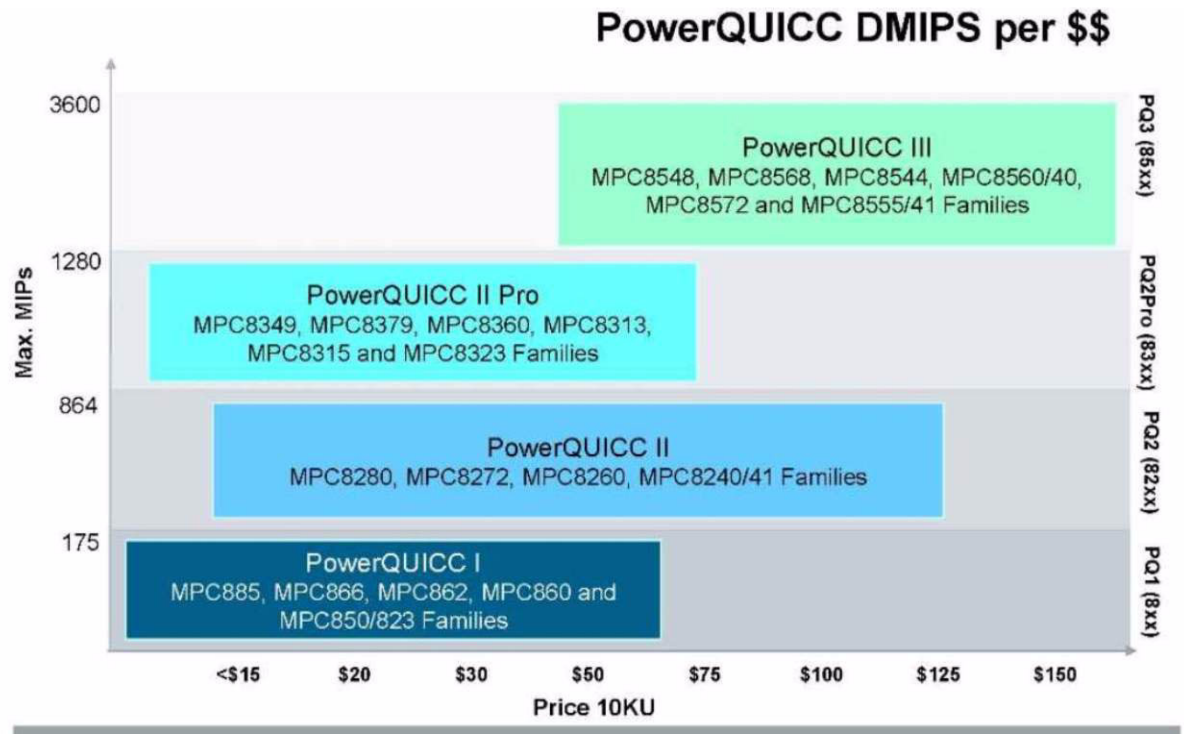

Figure 2. Freescale Solutions

Note 1: 8xx and 82xx products come with standard SDRAM interfaces.
Note 2: 83xx and 85xx products support DDR memories.

3 DDR Memory

DDR memory is identical to SDRAM internally. However, the important difference between DDR and SDRAM technology is the fact that DDR operates at twice the data rate as shown in Figure 3.

To attain a device data rate of 266 MHz, a DDR device transmits data on both positive and negative edges of the clock, reduces device input capacitance, adds on-chip delay locked loops (DLLs) to reduce access time uncertainty, adds data strobes to improve data capture reliability, and incorporates SSTL_2 signaling techniques.

DDR technology offers a number of key benefits to your design. For example, DDR reuses the existing DRAM infrastructure, four-bank core architecture, TSOP packaging, testers and printed circuit boards (for the modules). In addition, neither heat sinks nor continuity RIMMs are required; standard DIMMs are used. Figure 3 shows data rates for SDRAM and DDR SDRAM arrays.

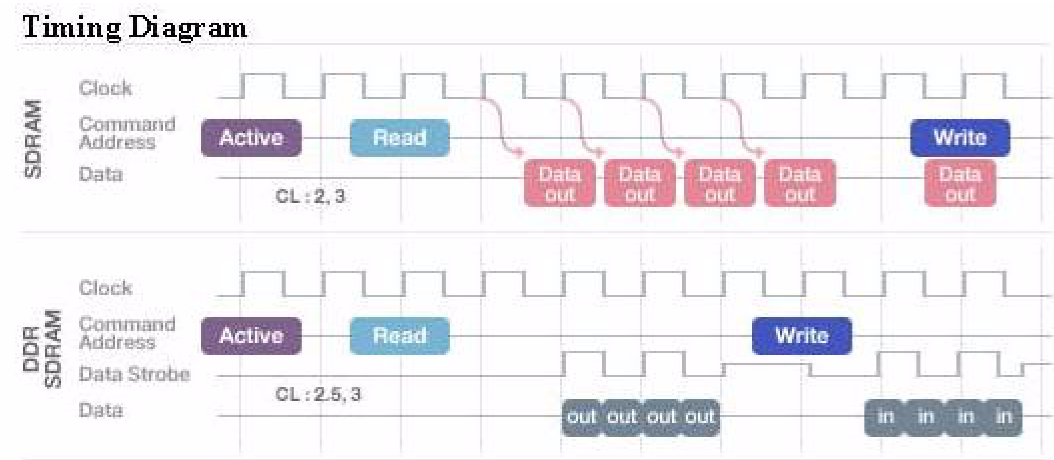

Figure 3. Timing Diagram

3.1 Types of DDR Memory

This section briefly discusses the various types of memory interfaces available to customers in today's market:

- DDR1 memory, with a maximum clock rate of 400 MHz and a 64-bit data bus
- DDR2 memory, with data rates ranging from 400 MHz to 800 MHz and a 64-bit data bus
- DDR3 memory, with data rates up to 1.6 GHz

Table 1 below highlights the performance improvements customers can achieve by migrating over to a DDR-based design.

Table 1. Functional Differences

Variables	SDRAM	DDR1	DDR2	DDR3
Clock	100/133/166 MHz	100/133/166/200 MHz	200/266/333/400 MHz	400/533/667/800 MHz
Transfer Data Rate	100/133/166 Mbps	200/266/333/400 Mbps	400/533/667/800 Mbps	800/1066/1333/1600 Mbps
I/O width	x16/x32	x4/x8/x16/x32	x4/x8/x16	x4/x8/x16/x32
Prefetch bit width	1 bit	2 bits	4 bits	8 bits
Clock Input	Single Clock	Differential Clock	Differential Clock	Differential Clock
Burst Length	1, 2, 4, 8, full page	2, 4, 8	4, 8	8, 4 (Burst chop)
Data Strobe	Unsupported	Single data strobe	Differential data strobe	Differential data strobe
Supply Voltage	3.3V/2.5V	2.5V	1.8V	1.5V
Interface	LVTTL	SSTL_2	SSTL_1.8	SSTL_1.5
$\overline{\text{CAS}}$ latency (CL)	2, 3 clock	2, 2.5, 3 clock	3, 4, 5, clock	5, 6, 7, 8, 9, 10 clock

Table 1. Functional Differences (continued)

Variables	SDRAM	DDR1	DDR2	DDR3
On Die Termination (ODT)	Unsupported	Unsupported	Supported	Supported
Package	TSOP(II)/FBGA	TSOP(II)/FBGA/LQFP	FBGA	FBGA

4 Design Considerations

Although integrating DDR will bring improved performance, designers need to take into consideration the following design elements during schematic and layout phases, in order to achieve desired performance:

- **Simulation**: Using simulation, identify optimal termination values, signal topology, along with trace lengths for each signal group in specific memory implementation.
- **Termination Scheme**: Identify optimal AC signaling parameters (voltage levels, slew rate, overshoot/undershoot) across all memory chips.
- **Routing:** Route DDR signal groups in the recommended order specified in Section 4.4, "Layout Order for the DDR Signal Groups."
- **Reference voltage (V_{REF}) generation**, see Section 4.2, "Reference Voltage Generation."
- **Terminal rail (V_{TT}) related items**.

4.1 SSTL_2 Signaling and Termination

The series stub termination logic (SSTL) used in DDR designs, leverages an active motherboard termination scheme. The most common SSTL termination is the class II single and parallel termination scheme shown in Figure 4. This scheme involves using one series resistor (R_S) from the controller to the memory and one termination resistor (R_T) attached to the termination rail (V_{TT}). Values for R_S and R_T are system-dependent and should be derived by board simulation. For further details refer to application note *AN2582 Hardware and Layout Design Considerations for DDR Memory Interfaces.*

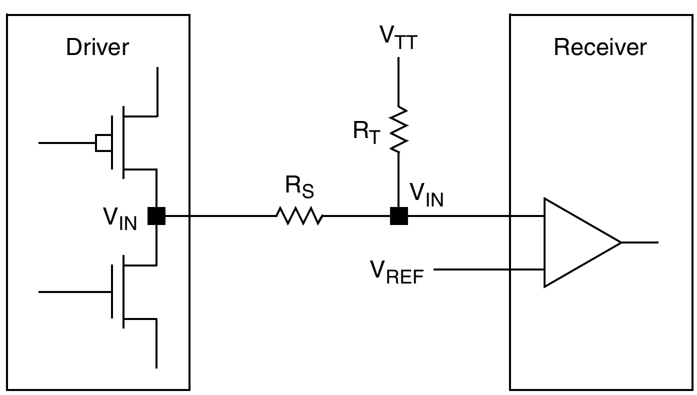

Figure 4. Typical Memory Interface Using Class II Option

4.2 Reference Voltage Generation

To avoid potential timing errors, jitter, and erratic memory bus behavior, the reference voltage V_{REF}, which controls the switching levels, must meet the following requirements:

- V_{REF} must track the midpoint of the signal voltage swing, generally $0.5 \times V_{DD}$ within 3 percent over all valid voltage, temperature, and noise level conditions.
- Each V_{REF} pin must use a proper decoupling scheme to keep the noise within the specified ranges by using 0.1 or 0.01 µF capacitors.
- A clearance of 20–25 mil should be kept between V_{REF} and other traces.
- The V_{REF} trace width should be routed to be a minimum of 20–25 mil.
- V_{REF} and V_{TT} must be on different planes due to the sensitivity of V_{REF} to the termination plane noise.
- V_{REF} and V_{TT} must share a common voltage supply. Several off-the-shelf power solutions provide both the V_{REF} and V_{TT} voltages from a common circuit. The MSC711xADS uses the Fairchild Semiconductor FAN1655 low dropout regulator to ensure regulation of V_{TT} to $0.5 \times V_{DDQ} \pm 40$ mV. Other potential V_{TT} power solutions include:
  - Fairchild FAN1655, FAN6555, ML6554
  - Philips NE57814, NE57810
  - TI TL5002
  - National Semiconductor LP2995, LP2994
  - Semtech SC1110

4.3 PCB Signal Routing

DDR signals must be properly routed to guarantee reliable operation at the maximum supported DDR frequency. The following PCB layout guidelines ensure that designs operate at the highest possible frequencies:

- Do not route DDR signals on any PCB layer that is not directly adjacent to a common reference plane.
- Signals within a data lane should be routed on the same layer as they traverse to the memory devices and to the V_{TT} termination end of the bus. This recommendation helps to ensure uniform signal characteristics for each data lane.
- All clock pairs should be routed on the same layer.
- Match the data, data strobe, and data mask signals in each data lane in trace lengths (± 25 mm) to propagation delays, and minimize the skew.
- Separate data and control nets by a minimum of 0.5 mm to minimize crosstalk.
- Isolate signal groups via different resistor packs. Place the termination resistors on a top layer. The R_S resistors should be close to the first memory bank. The R_T should directly tie into the V_{TT} island at the end of the memory bus. Each of the following groups should use a resistor pack:
  - Data signals and data strobes
  - Address and command signals

— Clock signals

- Route the data, address, and command signals in a daisy chain topology. Total trace lengths for any daisy-chained signal must not exceed 75 mm.
- Route control and clock signals point-to-point. Total trace lengths for any point-to-point signal must not exceed 50 mm.

4.4 Layout Order for the DDR Signal Groups

To help ensure that the DDR interface is properly optimized, Freescale recommends the following sequence for routing:

1. Power (V_{TT} island with termination resistors, V_{REF})
2. Pin swapping within resistor networks
3. Route data
4. Route address/command
5. Route control
6. Route clocks
7. Route feedback

The data group is listed before the command, address, and control group because it operates at twice the clock speed and its signal integrity is of higher concern. General layout guidelines for the above-mentioned signals groups can be found in application note *AN2582 Hardware and Layout Design Considerations for DDR Memory Interfaces*.

5 Summary

With every passing day, design teams all over the world are seeking newer and faster means to improve the performance of their products, keeping in mind the cost/performance benefits they can achieve. By migrating to DDR-based designs, engineers can realize a significant improvement in performance, while taking advantage of the cost savings of DDR memory prices relative to SDRAM memory prices.

5.1 Advantages of DDR SDRAM over SDRAM

- Double data rate, which translates to higher performance.
- Low device access latency.
- Lower supply voltage than SDRAM, which leads to less heat dissipation and improved power management.
- DDR-based devices provide improved performance at a device and system cost level similar to SDRAMs. Example: SDRAM 256MB, 32Mx8 @ 133 MHz costs $2.30 vs. DDR: 256MB, 32x8 ETT/UTT that costs $1.80 (Source DRAM Exchange 4/07/2008).

6 References

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- JEDEC STANDARD JESD79, June 2000, and JESD8-9 of September 1998
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- ELPIDA technical note on “Feature comparison of DDR2 SDRAM, DDR SDRAM and SDRAM.”
- Xilinx Inc., XAPP200 (v2.4), Synthesizable DDR SDRAM Controller, application note, July 18, 2002
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