White Paper

MPC826xSDRAMWP
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Timing Considerations when Interfacing the PowerQUICC II to SDRAM

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Abstract

The MPC826x (PowerQUICC II™) family devices all contain an integrated SDRAM memory controller which allows the devices to be interfaced ‘gluelessly’ to standard SDRAM devices. Due to certain timing specifications between the two devices some design considerations have to be taken into account when laying out a PCB. This White Paper discusses the interface of SDRAM memory devices using the on-chip SDRAM controller on the MPC826x family of devices.

1 Introduction

The SDRAM controller implemented in the MPC826x family allows standard SDRAM devices to be interfaced directly to the processor. All the required bus interface signals are generated automatically by the MPC826x devices. To improve the timing parameters associated with this interface, some parameters have been modified to allow better timing margins when interfacing to off-the-shelf SDRAM devices. However, certain design considerations must be taken into account when performing the PCB layout of SDRAM based designs. These timing changes and design considerations are described in this white paper.

2 Summary of PowerQUICC II Hardware Reference Manual Modifications

The SP10 timing parameter (hereafter sp10) is defined as the minimum input delay required by the PowerQUICC II for all bus input signals. Originally, the sp10 parameter was specified as 1 ns. This has been changed to 0.5 ns for all bus input signals. Please note that from a design perspective, this change of sp10 provides an overall improvement of the PowerQUICC II AC timing specification. This timing improvement is discussed further in Section 4.

The SP30 timing parameter (hereafter sp30) is defined as the minimum output delay guaranteed and is specified as 0.5 ns for all bus output signals.

The sp10/sp30 timing specifications and design guidelines described in this document apply to all current production versions of PowerQUICC II, on all pins:

- PowerQUICC II HiP3 (MPC826x): Rev A.1, B.1, B.2, B.3, C.2
- PowerQUICC II HiP4 (MPC826xA): Rev A.0, B.1

3 Background of sp10 Change: Potential Problem Description

Both the sp10 and sp30 timing specifications are particularly critical when interfacing the PowerQUICC II to SDRAM devices. Since most SDRAM devices available on the market today require a minimum hold time for input signals of 0.8 or 1 ns, the sp30 specification of 0.5 ns creates a mismatch between the minimum output delay obtainable from the PowerQUICC II and what is required from the SDRAM. Figure 1 and Figure 2 show the interaction of sp30 and sp10 (respectively) on several bus signals (including the SDRAM memory and control pins).

In order to address this mismatch and make it easier for hardware designers to implement a successful PowerQUICC II/SDRAM design, Motorola has tightened the sp10 specification (minimum input hold time delay) to 0.5 ns. The result of this new specification is that effectively more margin is added onto the existing sp30 specification.

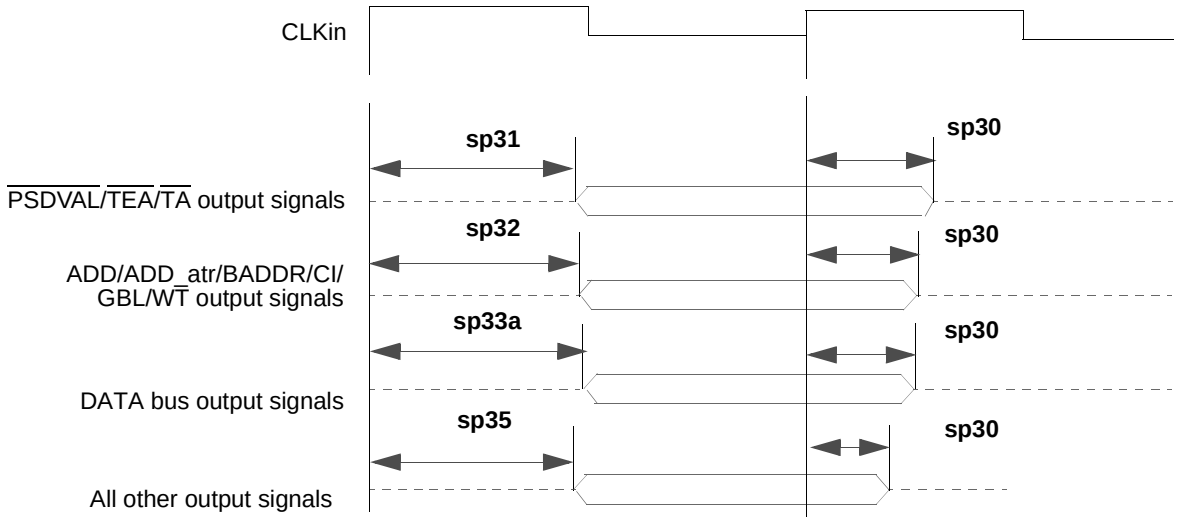

Figure 1. SP30 SIU Output Signals—Minimal Hold Time

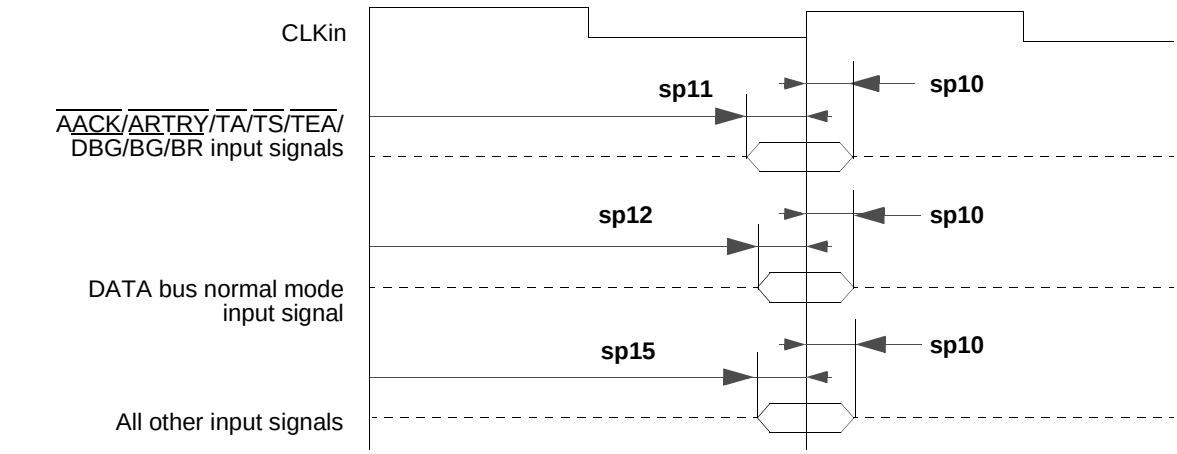

Figure 2. SP10 SIU Input Signals—Minimal Hold Time

In order to understand the reasoning behind these modifications, we will consider a typical PowerQUICC II-to-SDRAM interface. By investigating how the PowerQUICC II writes to and reads from SDRAM we will see the effect of the sp30 and sp10 AC timing specification.

4 PowerQUICC II Write to SDRAM

When a PowerQUICC II writes to SDRAM, the PowerQUICC II keeps its output signals (both data and control) stable during sp30 = 0.5 ns minimum. Typically, SDRAM requires its input data to be stable for 0.8 ns or 1 ns minimum (according to SDRAM manufacturers' device data-sheets). Thus, we have a theoretical 0.3 or 0.5 ns 'missing.' If you consider a wide 0.5-ns clock skew, then you come to 1 ns 'missing.' If in addition, the layout is such that the CLK input to SDRAM is delayed compared to PowerQUICC II clock input, then this 'missing' delay can become even worse.

Hence, in order to work around this possible mismatch, you may have to delay the clock input to the PowerQUICC II compared to the clock input to the SDRAM. In doing this, you make the SDRAM see the data input stable for a longer time, so in effect you compensate for the sp30 mismatch. Obviously this will vary depending on each design layout, although a reasonable clock delay could be anywhere between 1 and 2 ns.

Since we have created a delay between the clock inputs of the PowerQUICC II and the SDRAM using this proposed workaround, we must look at what it has changed when we consider the PowerQUICC II reading from the SDRAM. This is where the specification of sp10 becomes important.

5 PowerQUICC II Read from SDRAM

Let us now consider a PowerQUICC II read from SDRAM. Using typical SDRAM manufacturer's data, the data output from SDRAM should be maintained stable for at least 3 ns (note that the actual timing specification of tOH (time Output Hold) depends on the individual SDRAM device).

We stated that sp10 specifies the minimum input delay required by the PowerQUICC II. If we now consider the original sp10 specification of 1 ns, which looks reasonable in regard to the 3 ns guaranteed by our SDRAM example, it means that we have a 2-ns theoretical margin. The mismatch occurs when we obey sp30 by delaying the clock to the PowerQUICC II; then we reduce this margin. For example, if we consider a worst case PowerQUICC II clock delay of 2 ns, then it becomes immediately apparent that we are at the limit of the sp10 timing. This is why decreasing the sp10 specification to 0.5 ns (as in the new specification) gives more safety (or margin) to the designer who implements a solution for sp30 by delaying the PowerQUICC II Clock.

5.1 PowerQUICC II SDRAM Setup/Hold Time—83.33-Mhz Example

Figure 3 below shows an example of both the set-up and hold times associated with writes to and reads from an SDRAM at 83.33 Mhz.

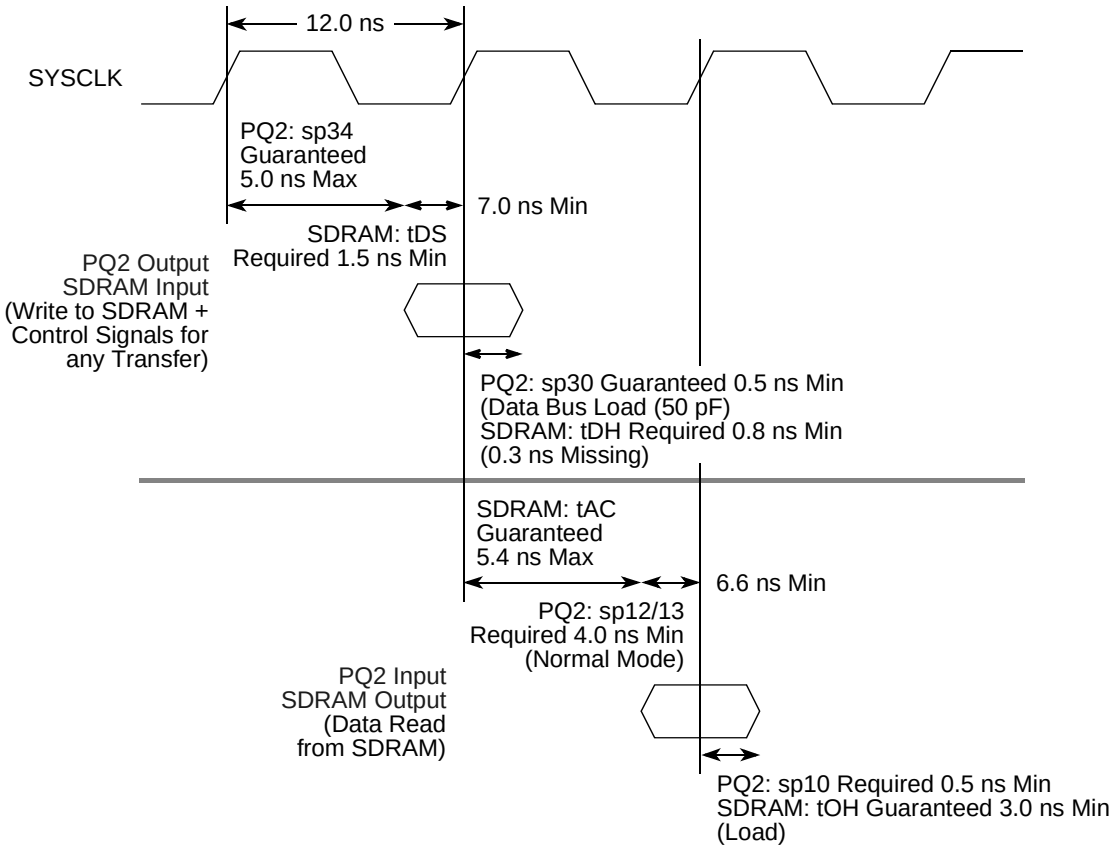

Figure 3. Setup/Hold Times for SDRAM Write/Read at 83.33Mhz

In this example, we use SDRAM parameters taken from the AC specification of a standard SDRAM device and we also assume theoretical margins, that is, we assume no clock skew or line delays. If we consider the first instance in the diagram for PowerQUICC II output/SDRAM input (that is, a write to the SDRAM) we have the following cases , shown in Table 1 below:

Table 1. SDRAM Setup/Hold Time Margins @ 83.33 MHz

Case	Hold time	Setup time	Load
PQ2 output/SDRAM input (write SDRAM)	No margin—out of spec (–0.3 ns)	5.5-ns margin	50 pF
PQ2 input/SDRAM output (read SDRAM)	2.5 ns	2.6-ns margin	50 pF

The following sections give some guidelines for implementing PowerQUICC II clock input delay compared to the SDRAM clock input.

6 Proposed Solutions

Customers who currently face tight SDRAM timings when designing their boards should consider the implementation of one of the following solutions in order to ensure that correct timings are achieved at the SDRAM input pins:

- Addition of trace length
- Use of an MPC9315 Clock Generator
- Use of the PLL in the MPC9315 Clock Generator

The following sections discuss these solutions.

6.1 Addition of Trace Length

This solution involves positively phase shifting the PowerQUICC II clock with respect to the clock of the SDRAM. This phase shift is accomplished by adding a trace length differential, such that the PowerQUICC II clock trace is significantly longer than the SDRAM clock trace. Note that this shift may also affect other circuits and components driven by the assumed bus frequency of 83.33 MHz that synchronously interact with the PowerQUICC II. The implementation utilizes a lengthened clock trace to the PowerQUICC II and an unchanged clock trace length to the SDRAM. Refer to Figure 4 for an implementation diagram.

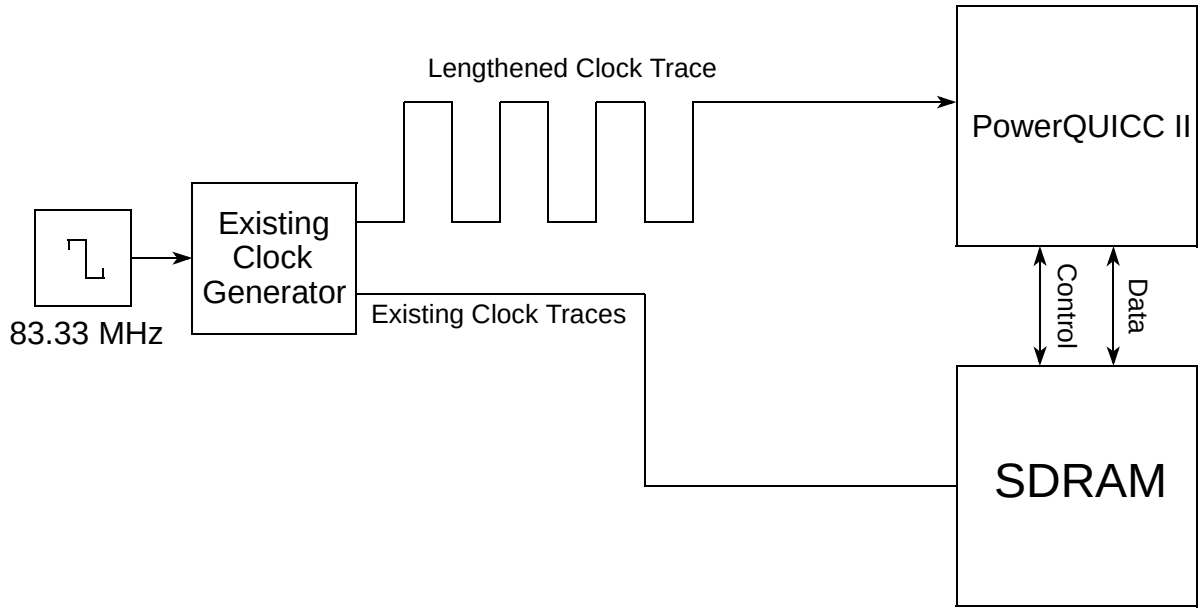

Figure 4. Extended Trace Length Implementation

Assuming that the clock traces on the existing board are of equal length, the PowerQUICC II trace needs to be lengthened to overcome the write hold time error margin, which is 0.3 ns, or 0.8 ns (SDRAM hold time requirement) – 0.5 ns (PowerQUICC II hold time provided).

The trace length must not exceed 2.5 ns, which is 3 ns (SDRAM data hold provided) – 0.5 ns (PowerQUICC II hold time requirement), otherwise a read timing violation will occur. The target window for trace length then becomes that which will provide 0.3 ns to 2.5 ns of delay. Should the traces not be of

equal length, the differential between the PowerQUICC II and SDRAM trace lengths must be such that the delay is provided within the target window.

For example, typical propagation delays for a PC board of FR4–type material are between 140–180 ps/in for a trace on an outer layer, and 180–192 ps/in for a trace on an inner layer.

Given the worst case propagation delays:

- minimum trace length differential = 300 ps / (140 ps/in) = 2.15 in,
- maximum trace length differential = 2500 ps / (192 ps/in) = 13.02 in.

Ultimately, the trace length used must be determined and calculated based on each board design in question, since adding trace lengths improves hold times, but can degrade setup times. While in principle the change of the trace length is a very precise method, it requires careful planning during the design/netlist stages as there is no means to adjust to the actual resulting board behaviour later on as with the following examples.

6.2 Use of an MPC9315 Clock Generator

If we consider implementing a Motorola MPC9315 clock generator with a guaranteed 120-ps output-to-output skew (80-ps if within one bank), the margin would increase and allow a shorter clock trace length differential. Implementation of this part results in a trace length window of:

- minimum trace length = (300 ps + 80 ps) / (140 ps/in) = 2.71 in,
- maximum trace length = (2500 ps – 80 ps) / (192 ps/in) = 12.60 in.

For the purposes of this example, a 3.5-in trace length differential would give a margin above the minimum delay required, yet does not ‘over-delay’ the signal such that read timing violations occur elsewhere. This produces the following result:

- minimum delay = 3.5 in × 140 ps/in = 490 ps.
- maximum delay = 3.5 in × 192 ps/in = 672 ps.

The positive phase shift provided by the extended clock trace length to the PowerQUICC II allows us to hit the target window where both the read and write hold times are within specification. Utilization of an MPC9315 clock generator also gives us more margin, and the ability to shorten the clock trace length differential, since this generator has a low output-to-output skew specification. Additional analysis would need to be performed to determine the effect of the PowerQUICC II time shift with respect to other synchronous circuits that interface with the PowerQUICC II. This configuration is shown in Figure 5.

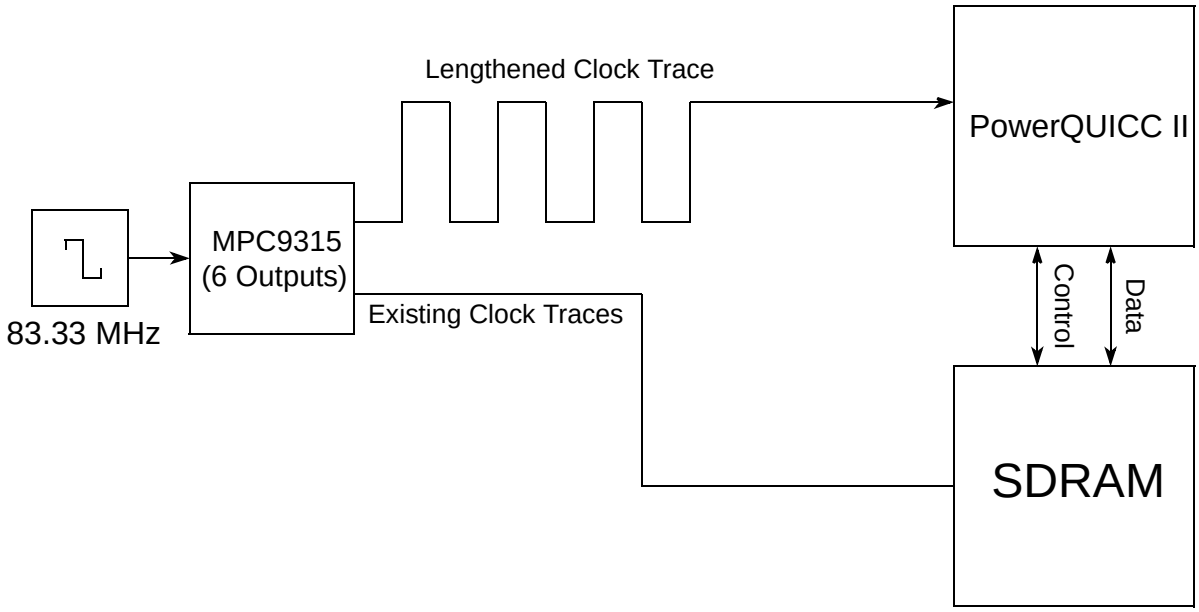

Figure 5. SDRAM Clock Skew Implementation Utilizing MPC9315

6.3 Use of the PLL in the MPC9315 Clock Generator

Another solution is to negatively shift the SDRAM clock with respect to the clock to the PowerQUICC II. This phase shift is accomplished by using the PLL synthesizer in the clock generator device. As the bus specifications are valid in general, other components should also benefit from the better margins achieved.

The implementation investigated in this proposal again utilizes the MPC9315 PLL Clock Generator. The device would be configured in zero-delay buffer mode with the input clock used to also drive the PowerQUICC II device directly. A configurable delay would be added to the feedback path to effectively put a negative delay on the output of the clock driver. This is because in zero-delay mode the internal PLL synchronizes the output clock with the input clock and since we have added a delay to the feedback path the output clock must be ahead of the input clock.

The net result of this approach is that the very low output-to-output skew of the MPC9315 leads to precise clocking of multiple attached SDRAM devices, while the delay for the PowerQUICC II clock is well-defined by the input-to-output delay of the clock driver and the negative effective delay introduced by the configurable delay path. It is expected that for a negative PLL phase shift, an accuracy of 5% of the calculated delay can be achieved without expensive components, which is possible even with an RC combination. This is shown below in Figure 6.

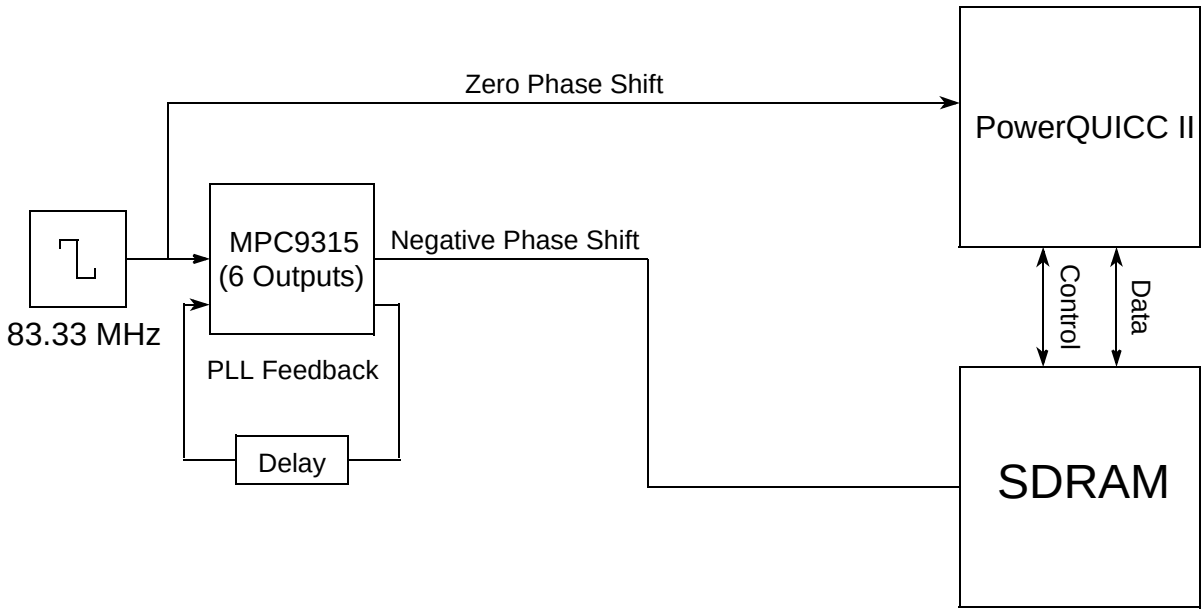

Figure 6. SDRAM Clock Skew Implementation Utilizing MPC9315 PLL

7 XFC Filter Stabilization

The sp30 hold time can be exacerbated by poor clock signals and/or voltage droop. The most likely factor is induced jitter from the PLL clock. If PLL jitter is observed (that is, > 2 ns as per specification) in an existing board design, changing the XFC filter design to a 3rd-order filter can help to stabilise the PLL clock output arising from this voltage droop. In order to keep the internal PLL of the PowerQUICC II stable under all conditions, a 2.5-KΩ resistor is added (in series) with the existing capacitor on the XFC pin. The resistor should be connected to the Vccsyn side of the XFC capacitor as illustrated in Figure 7. (The value of the series resistance may have to be adjusted slightly depending on the actual board design).

In general the XFC value should be calculated according to the normal formula and the resistor value does not change.

It should be verified that even under system load, the PLL and core power supply do not ever drop below the nominal value at the PowerQUICC II component. Voltage drops may affect PLL stability and introduce excessive jitter, which in turn can affect the bus timings.

For more information, the interested reader should refer to the application note *Effects of Clock Jitter on the MPC8260 (HiP3 and HiP4)*, located at http://www.motorola.com/semiconductors/.

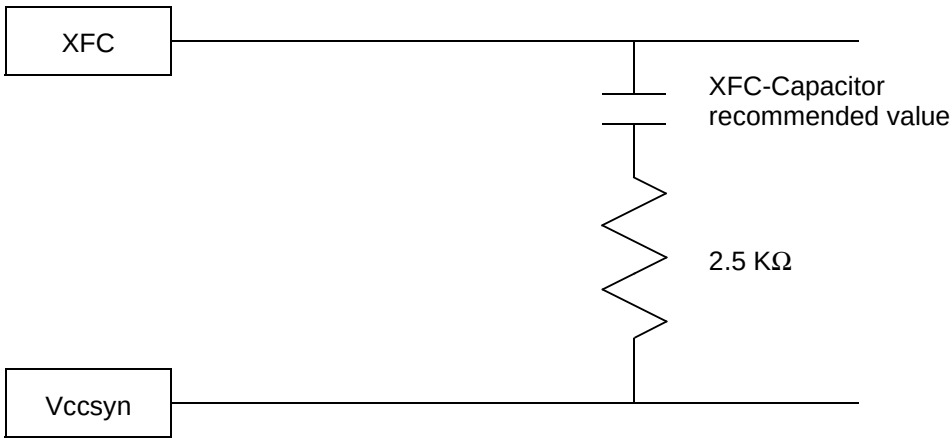

Figure 7. Recommended XFC/VCCsyn Configuration

8 Additional Reference Material

The following materials are all available at http://www.motorola.com/semiconductors/:

- *MPC8260 PowerQUICC II™ Family Reference Manual* (Motorola Document No. MPC8260UM)
- *Effects of Clock Jitter on the MPC8260 (HiP3 and HiP4)* (Motorola Application Note No. AN2638)
- *MPC8260 PowerQUICC II Design Checklist* (Motorola Application Note No. AN2290)
- *MPC8260 SDRAM Timing Diagram* (Motorola Application Note No. AN2178)

8.1 HIP3 Documents

- *MPC8260 PowerQUICC II Family Device Errata* (Motorola Document No. MPC8260CE)
- *MPC8260 HiP3 Hardware Specifications* (Motorola Document No. MPC8260EC)

8.2 HIP4 Documents

- *MPC8260 PowerQUICC II Family Device Errata* (Motorola Document No. MPC8260CE)
- *MPC8260A HiP4 Family Hardware Specifications* (Motorola Document No. MPC8260AEC)

NOTE

Hardware reference manuals are subject to change without notice.

9 Conclusion

This white paper has shown a number of different approaches for improving SDRAM setup and hold times. (Simulation and timing analysis has not been performed due to the number of possible board layout combinations.) It has been shown that with careful design layout it is possible to implement a ‘glueless’ interface between the MPC826x family devices and standard SDRAM devices. It has also been shown that the use of a DLL-based clock driver device gives the ability to fine tune the interface timing by simply changing the value of delay components and does not depend on accurate PCB trace length differences.

The details and calculations performed in this document are based on the PowerQUICC II and typical SDRAM timing specifications. End users should ensure that the timing of their own designs are completely robust by performing appropriate levels of timing analysis and/or simulation, prior to final PCB fabrication.

10 Revision History

Table 1 provides a revision history for this Document.

Table 1. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial document.
0.1	Added reference to AN2638 (*Effects of Clock Jitter on the MPC8260 (HiP3 and HiP4)*)

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