AN12423

LPC5460x 在 SDRAM 中执行代码的方法介绍

版本 0 — 2019 年 4 月 20 日 应用笔记

目录

1 简介

本文介绍了在同步动态随机存取存储器（SDRAM）中执行代码的方法以及 LPC5460x 的性能基准。在嵌入式系统设计中，由于内存占用太大而无法存放在片上 flash/RAM 时，会经常使用 SDRAM。在 SDRAM 中执行程序是 SDRAM 的一种典型用法。

1.1 SDRAM

微控制器应用中使用的 SDRAM 是单数据速率（single data rate），它可以接收一个命令，并在每个时钟周期传输一个数据字。通常，在微控制器应用中，SDRAM 的时钟频率为 100 MHz 或 133 MHz。

1.2 外部存储器控制器

在 LPC5460x 中，有一个支持外部存储器访问的外部存储器控制器（EMC）。可以支持不同的 SDRAM。

2 使用 SDRAM

2.1 SDRAM 初始化

当系统启动时，SDRAM 尚未初始化，必须在使用前进行配置。在 SDRAM 初始化函数中，应配置 EMC 寄存器中的 SDRAM 时钟频率、字节顺序和时序参数。

可以在 MCU 启动后随时进行 SDRAM 初始化，但是，开发人员更喜欢在 MCU 启动初期初始化 SDRAM，此时有一些注意事项。

1. SDRAM 初始化可能使用 STACK 或全局变量，开发人员必须确保 STACK 或全局变量所在的物理内存已上电。
2. 如果在主函数之前执行了 SDRAM 初始化，全局变量在主函数启动之前没有初始化或清零，那么，开发人员必须手动设置相关数据。

在文件 board.c 中，函数 BOARD_InitSDRAM 用于初始化 SDRAM，此函数可以在函数 SystemInit 中调用，而此函数由程序入口 Reset_Handler 调用。如下面的代码片段所示，如果需要将程序 STACK 或 SDRAM 相关的变量放在 SRAM 区域中，则在 Reset_Handler 中，要将 AHBCLKCTRLSET0 寄存器设置为 0x38 以启用 SRAM1/SRAM2/SRAM3 时钟。

```
Reset_Handler PROC
EXPORT Reset_Handler [WEAK]
IMPORT SystemInit
IMPORT __main
; clock control SRAM1/SRAM2/SRAM3 for stack
LDR r0, = 0x40000220
MOV r1, #0x38
STR r1, [r0]
LDR r0, =SystemInit
BLX r0
LDR r0, =__main
```

```
BX r0
ENDP
```

2.2 内存分配

考虑到 SDRAM 芯片选择具有四种类型，SDRAM 可以从四个可能的地址启动，如 表 1 所示。

表 1. SDRAM 内存地址

SDRAM 地址范围	SDRAM 芯片选择
0xA0000000 – 0xA7FFFFFF	SDRAM Chip Select 0 (Up to 256 MB)
0xA8000000 – 0xAFFFFFFF	SDRAM Chip Select 1 (Up to 256 MB)
0xB0000000 – 0xB7FFFFFF	SDRAM Chip Select 2 (Up to 256 MB)
0xB8000000 – 0xBFFFFFFF	SDRAM Chip Select 3 (Up to 256 MB)

开发人员可以使用链接脚本将代码或数据分配到 SDRAM 中，不同 IDE 的链接脚本是不同的。

以 KEIL 环境为例，在下面的链接脚本中：

1. 定义了 SDRAM 区域，从 0xA0000000 开始，大小为 0x80000。
2. 具有 SDRAM_Data 和 SDRAM_Function 属性的数据或代码位于 SDRAM 区域。
3. core_list_join.c，core_matrix.c，core_state.c，和 core_util.c 中的数据和代码位于 SDRAM 区域。

```
#define m_sdram_start 0xA0000000
#define m_sdram_size 0x80000
LR_m_sdram_text m_sdram_start m_sdram_size {
   *(SDRAM_Data)
   *(SDRAM_Function)
   core_list_join.o
   core_matrix.o
   core_state.o
   core_util.o
}
```

2.3 MPU 配置

如《Cortex™-M4 设备通用用户指南》中所述，内存 0xA0000000–0xDFFFFFFF 的默认配置不可执行。在禁用 MPU 的情况下执行 SDRAM 中的代码时，默认配置生效，Arm CM4 会发出带有指令访问冲突标志的 HardFault，该标志位位于 SCB-> CFSR 的第 1 比特位。请参见 图 1。

该故障表明，处理器试图从不允许执行的位置提取指令。

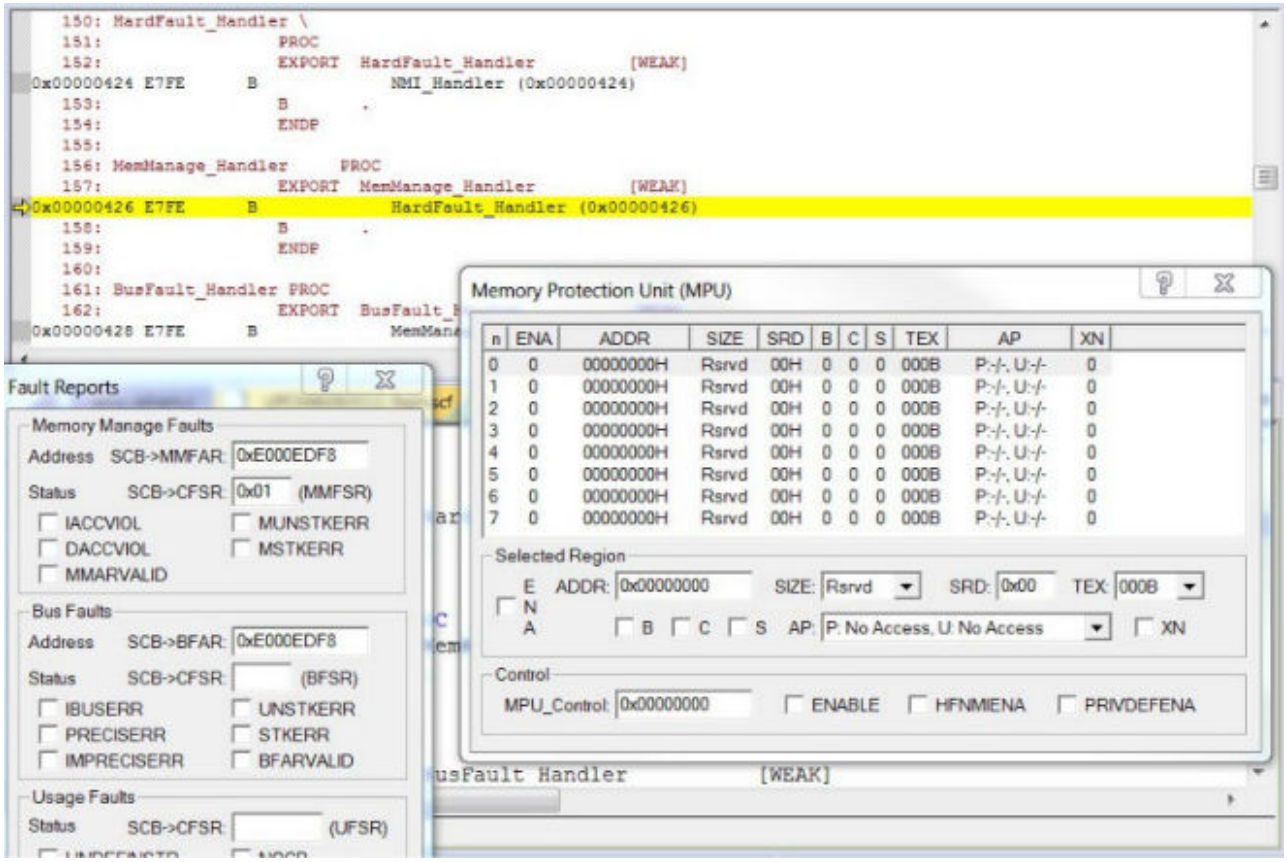

图 1. IACCVIOL hard fault

因此，如果开发人员要在 SDRAM 中执行代码，必须更改 MPU 配置。在下面的代码片段中，配置了 MPU，使得从 0xA0000000 到 0xA0100000 的内存区域是可执行的。

MPU->RNR = 0; //Region number 0

MPU->RBAR = 0xA0000000;//Region base address

/ Full Access | TEX: 000 | S: 0 | C: 0 | B:0 (No cacheable, no shareable)| 1M SIZE | ENABLE */*

MPU->RASR = (0 << 28) | (0x3 << 24) | (0x0 << 19) | (0 << 18) | (0 << 17) | (0 << 16) | (0xFF < 8) | (0x13 << 1) | (1 << 0); //Region size and enable

MPU->CTRL = MPU_CTRL_ENABLE_Msk | MPU_CTRL_PRIVDEFENA_Msk;

3 SDRAM 性能基准

SDRAM 代码的执行性能基准是通过 CoreMark 测试得到的，请见 表 2。通过测量，我们可以得出以下结论：

1. SDRAM 中的代码执行性能仅达到 SRAMX（可访问 ICODE）SRAM 中的 40%，达到片上 FLASH 中的约 50%。
2. 当代码在 SDRAM 中运行时，较高的 CPU 频率对提高性能没有帮助，SDRAM 带宽会成为瓶颈。

表 2. 使用 CoreMark 对 SDRAM 性能基准进行测量

基本信息
CoreMark Size: 666

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表 2. 使用 CoreMark 对 SDRAM 性能基准进行测量 (续上页)

迭代次数: 4000 编译器版本: Arm C/C++ Compiler, 5.24.2 [Build 528] 编译器标志: --c99 -c --cpu Cortex-M4.fp -D__MICROLIB -g -O3 -Otime --apcs=interwork 内存位置: STATIC	
内存配置	**每次迭代时间 (ms)**
Code executing in SRAMX, Arm CM4@96 MHz	4.015
Code executing in SRAMX, Arm CM4@180 MHz	2.141
Code executing in On-Chip FLASH, Arm CM4@96 MHz	4.869
Code executing in On-Chip FLASH, Arm CM4@180 MHz	3.228
Code executing in SDRAM@96MHz, Arm CM4@96 MHz	10.050
Code executing in SDRAM@180MHz, Arm CM4@90 MHz	10.458

4 参考文献

来源	标题
NXP Semiconductors	LPC5460x data sheet
NXP Semiconductors	LPC5460x user manual
NXP Semiconductors	OM13090 user manual
ARM Ltd.	Cortex-M4_ReferenceManual
ARM Ltd.	Cortex-M4 Technical Reference Manual Revision r0p1

5 修订记录

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