MCIMX6SLEVK board

Table of Content

Revision History

Rev. Code	Date	Description
A	2012/05/11	Rev A
B	2012/09/27	ENGR00225877. Replaced D24 with BAT54C-7-F ENGR00225876. DNP standoffs H1, H2, H3 and H4 ENGR00225878. Replaced R11, R129 and R130 with SH14, SH15 and SH16 respectively ENGR00225879. 1. Replaced U3 - MMPF0100NPEP with MMPF0100F1EP 2. Replaced C23 (0.1uF, 0402) with 0.22uF, 0201 3. Added C410, C412 per PMIC datasheet 4. Replaced C40 (0.1uF, 0402) with 0.22uF, 0201 5. Replaced C27, C28 and C32 (0.1uF) with 0.22uF 6. Replaced C70 (22uF, 0603, 6.3V) with 47uF, 0805, 10V ENGR00226044. Replaced P4 - WM-64PNT with WM-64PCT ENGR00226043. Replaced U2 - K4P8G304EB-AGC1 with MT42L256M32D2LG-25WT ENGR00225880. 1. Replaced C146 (10uF) with 47uF 2. Replaced C159 and C160 (0402, 6.3V) with 0603, 10V ENGR00225881. 1. Move PMIC SW1AB feedback to the load side of SH2 to compensate for SH2 voltage drops during current measurement. 2. Move PMIC SW1C feedback to the load side of SH3 to compensate for SH3 voltage drops during current measurement. 3. Move PMIC SW2 feedback to the load side of SH1 to compensate for SH1 voltage drops during current measurement. 4. Move PMIC SW3 feedback to the load side of SH5 to compensate for SH5 voltage drops during current measurement. ENGR00225088. Connected J12.117 to POR_B ENGR00226215. Renamed PFUSE_VIN net to PF0100_VIN ENGR00227037. Replaced all capacitors in PF0100_VIN net whose voltage rating is less than 10V with 10V capacitors: C46, C47, C65, C41, C48, C63, C58. ENGR00227038. Flipped the capacitors whose polarity was inverted: C4, C2, C11, C21, C36, C46, C47, C58, C66, C156, C166, C178, C218, C200. ENGR00223967: 1. Added test points TP42, 43, 44 and 45 2. The following pins were changed to NC in J8: CLKREQ#, UIM_C8, UIM_C4W, SMB_CLK, SMB_DATA, LED_WLAN#, LED_WPAN#, Reserved1-8, Reserved10 3. DNP C140, C191, C192 and C210 ENGR00229277: Y1 (CC7V-T1A) 9pF is selected as default/preferred part. However, 12pF version may be used for production board. ENGR229701: 1. Removed R195. 2. Replaced C152 (150uF) with 2.2uF

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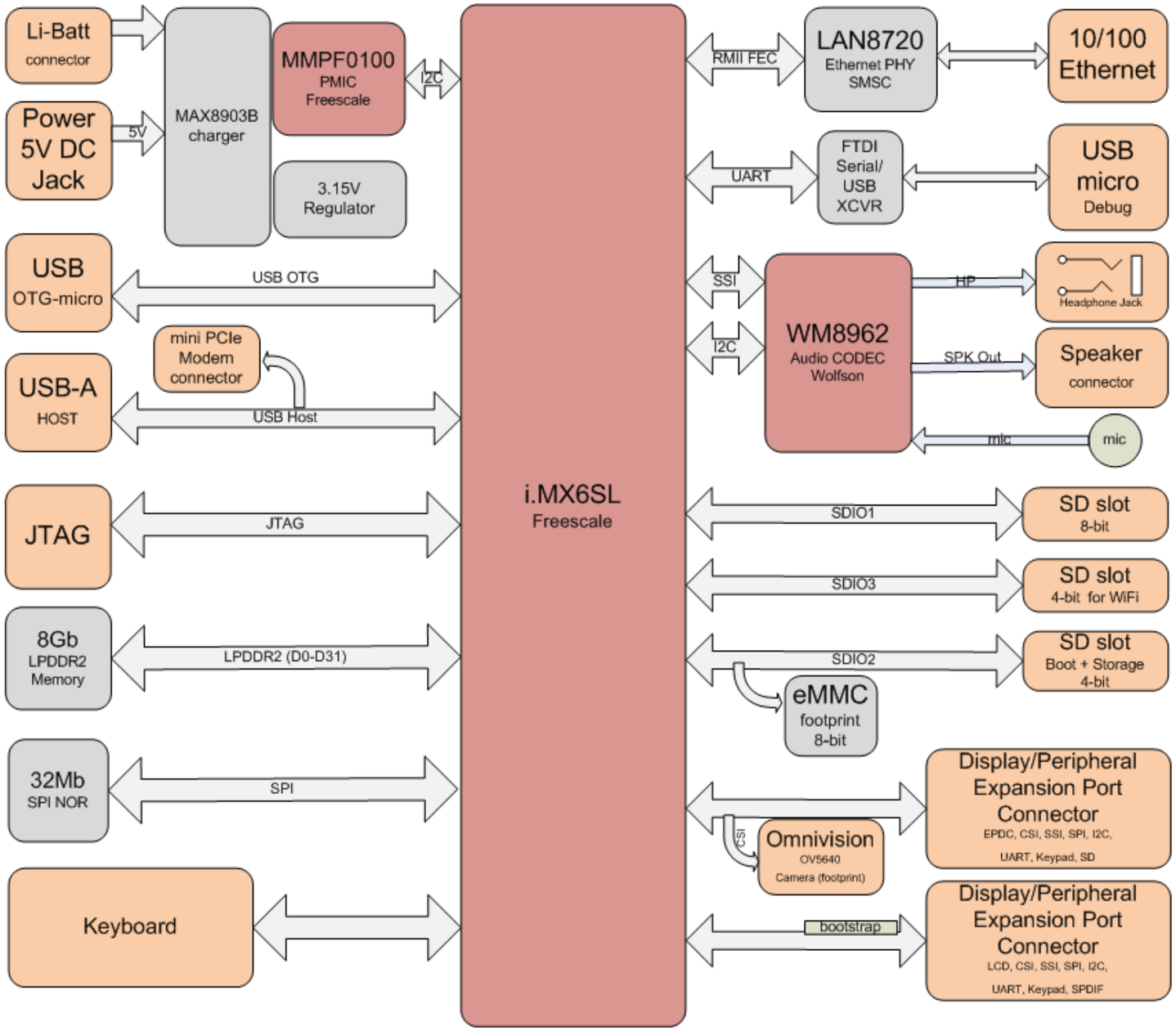
MCIMX6SLEVK board Diagram



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MCIMX6SLEVK board

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Block Diagram

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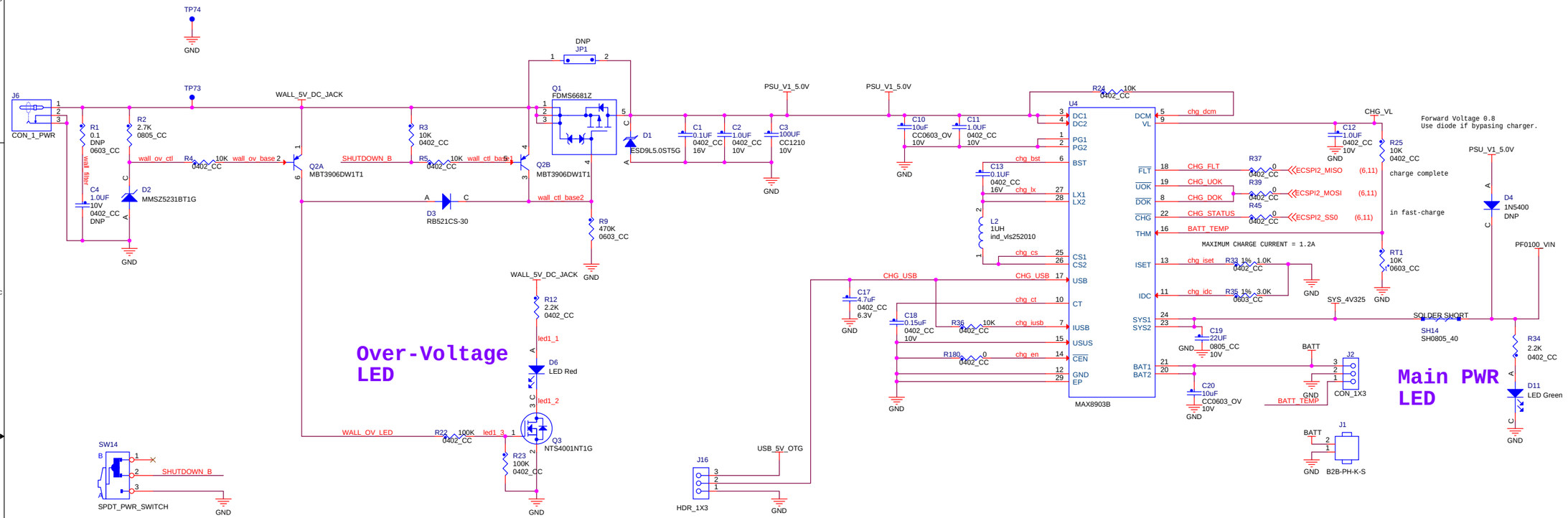
DC JACK 5V

Over Voltage Protection

Lithium Charger



PWR Cut Switch For SW Development

Secondary Charge Source USB or Wireless Charger

Note:
Shunt 2-3 to experiment with USB charging.

Use cable to pins 1 and 2 to experiment with wireless charging

Lithium single cell battery connectors

NEED TO FIGURE OUT THIS BETTER

PWRCTRL3 is the capacitive touch interrupt.
MISO and SSO might be OK.
must permanently decide to eliminate ability to use ECSPI2
Also should use pullups inside the processor

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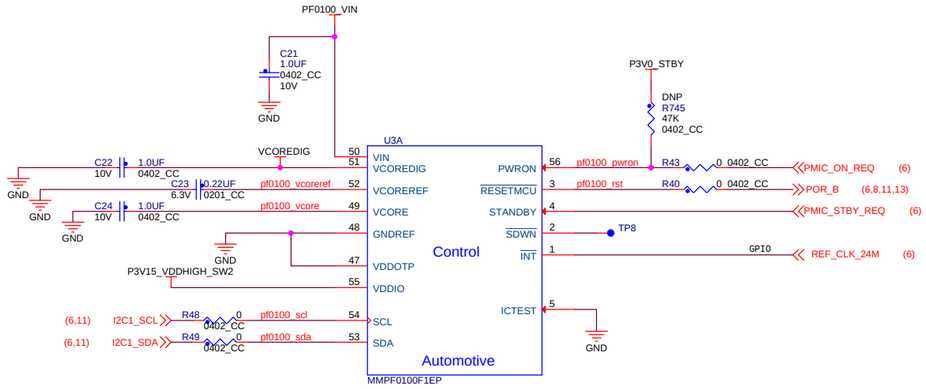
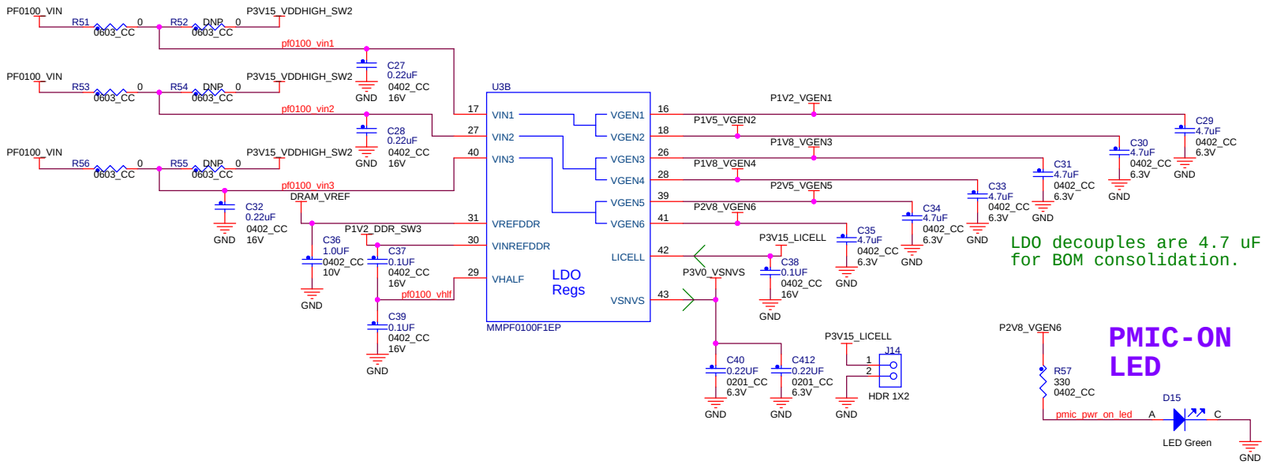
…itum ER19 can affect some of the systems, depending on the …eristics. Please check this erratum and its workaround to see if applies.

Freescale MMPF0100NPEP PMIC

Note:
This device is factory configurable for voltage and timings.
This reference design is configured to run from factory pre-programmed parts.
Ordering selections with common i.MX6SL voltages/timings are available.
Please check the device datasheet for latest ordering info.



With low-inductive paths between VIN the voltage sources, either 0.22 uF or 0.47 uF may be used.

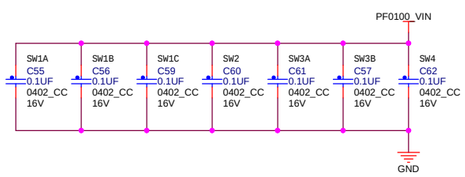


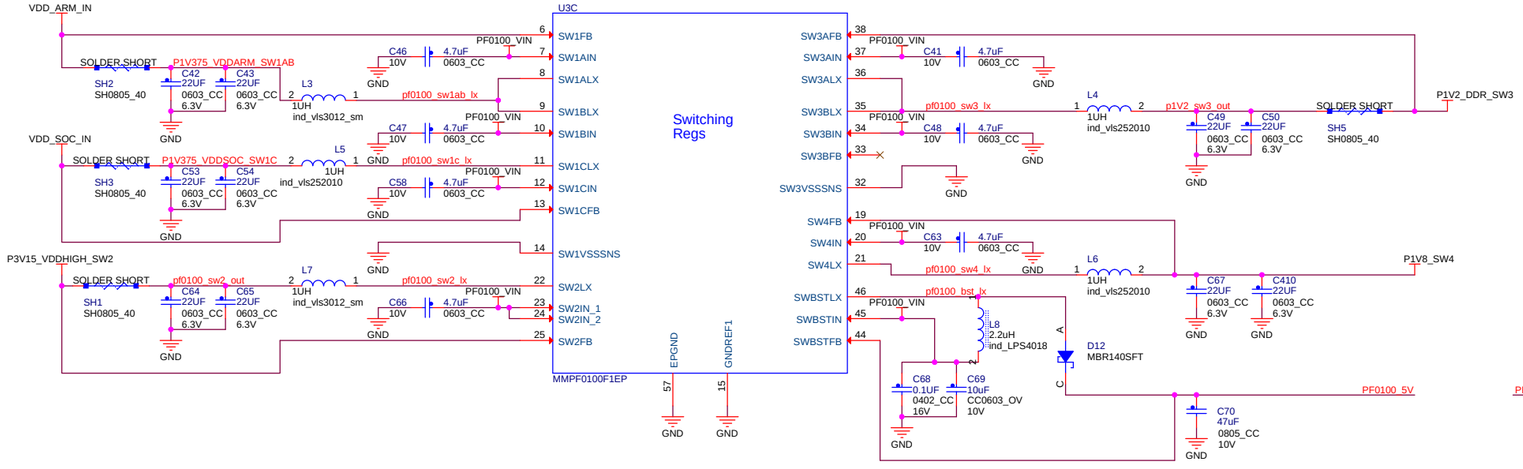
LDO decouples are 4.7 uF for BOM consolidation.

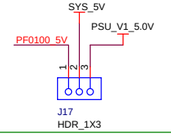
PMIC output rails

PF0100	Voltage(V)	Current(A)	Power up sequence	Note
SW1A/B	1.375	2.5	1	
SW1C	1.375	1.7	1	
SW2	3.15	2	2	
SW3A/B	1.2	2.5	4	
SW4	1.8	1	3	
SWBST	5	0.6		
VGEN1	1.2	0.1	4	
VGEN2	1.5	0.25		
VGEN3	1.8	0.1		
VGEN4	1.8	0.35	3	
VGEN5	2.5	0.1	5	LED
VGEN6	2.8	0.2		
VSNVS	3	0.0002	0	
VREFDDR	0.6	0.01	4	

SW1A/B = 1.375 V for boot-up at ~800 MHz.
Recommend that software increase SW1A/B to 1.425 V for 1 GHz operation.







Note:
Switcher currents and optimum inductor sizes vary depending on application.
Please refer to the latest part datasheet for inductor recommendations.

Note: J17
Shunt 1-2 for SYS_5V from PMIC: 600mA limited
Shunt 2-3 for SYS_5V from wall adapter

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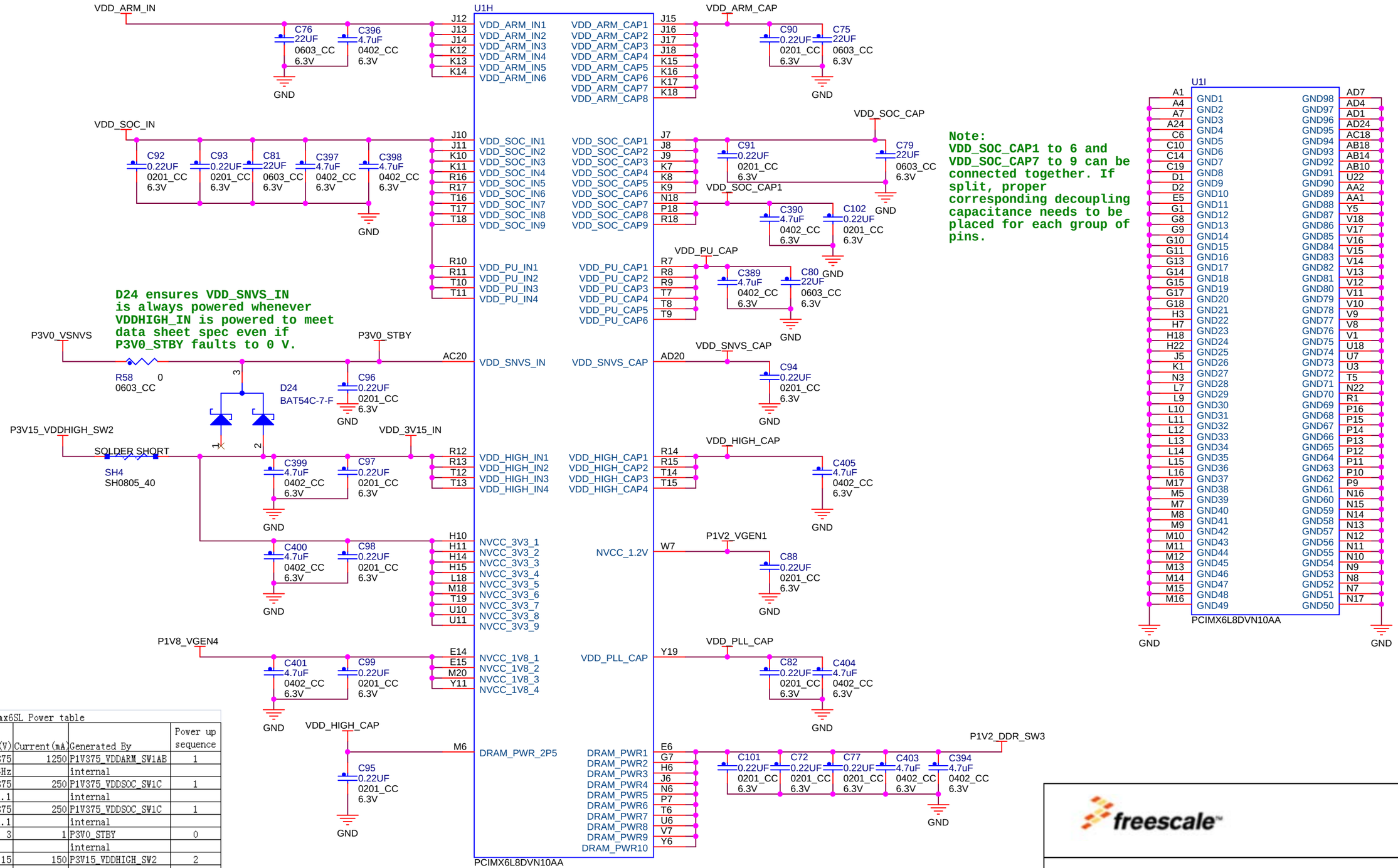

i.mx6SL Power table

i.mx6SL Voltage Rail	Voltage(V)	Current(mA)	Generated By	Power up sequence
VDD_ARM_IN	1.375	1250	P1V375_VDDARM_SW1AB	1
VDD_ARM_CAP	1.2@1GHz		internal	
VDD_SOC_IN	1.375	250	P1V375_VDDSOC_SW1C	1
VDD_SOC_CAP	1.1		internal	
VDD_PU_IN	1.375	250	P1V375_VDDSOC_SW1C	1
VDD_PU_CAP	1.1		internal	
VDD_SNVS_IN	3	1	P3V0_STBY	0
VDD_SNVS_CAP			internal	
VDD_HIGH_IN	3.15	150	P3V15_VDDHIGH_SW2	2
VDD_HIGH_CAP	2.5		internal	
NVCC_3V3	3.15	150	P3V15_VDDHIGH_SW2	2
NVCC_1V8	1.8	125	P1V8_VGEN4	3
NVCC_1.2V	1.2		P1V2_VGEN1	4
VDD_PLL_CAP	1.1		internal	
VDD_USB_CAP	3		internal	
DARM_PWR_2P5	2.5		VDD_HIGH_CAP	2
DRAM_PWR	1.2	200	P1V2_DDR_SW3	4
DRAM_VREF	0.6		P0V6_VREFDDR	4

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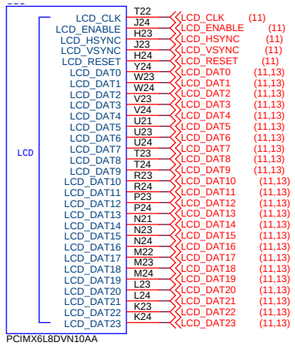
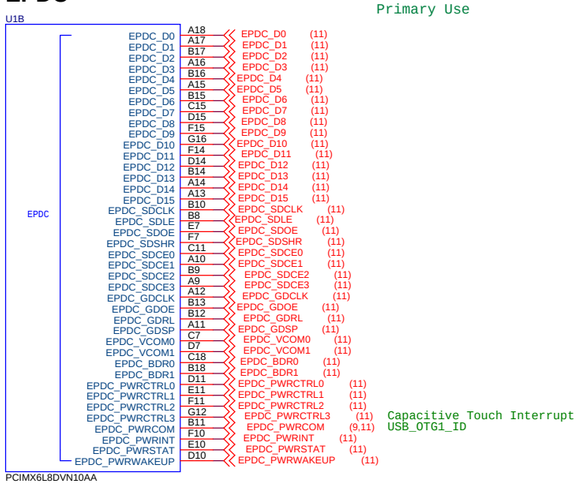
LCD



EPDC

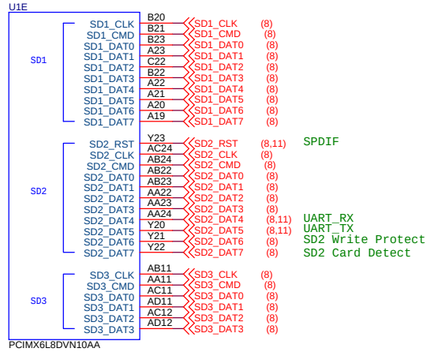
Primary Use



Capacitive Touch Interrupt
USB_OTG1_ID

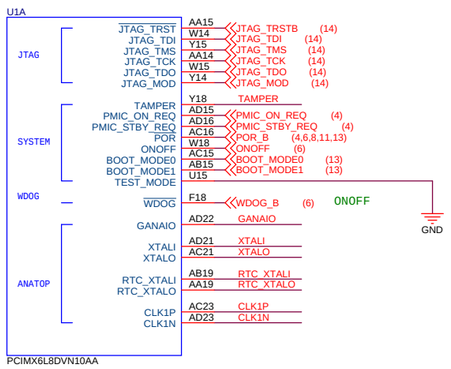
SD

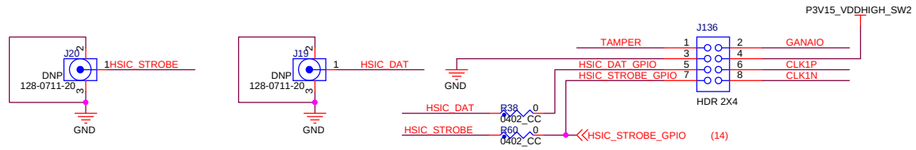
Primary Use



SPDIF
UART_RX
UART_TX
SD2 Write Protect
SD2 Card Detect

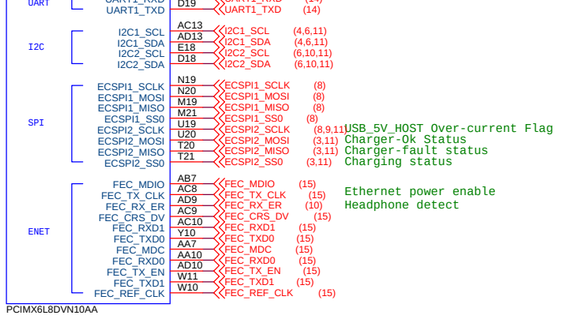
Control





Audio,UART,FEC

Primary Use



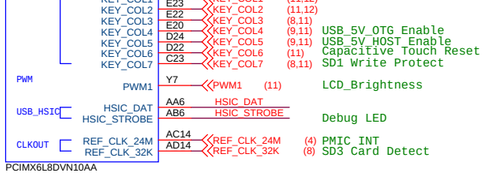
3G Card Enable
3G Card Reset

USB_5V_HOST Over-current Flag
Charger-Ok Status
Charger-fault status
Charging status

Ethernet power enable
Headphone detect

Keypad,HSIC,PWM

Primary Use



USB_5V_OTG Over-current Flag
LCD_Power_EN
Accelerometer Interrupt
SD1 Card Detect

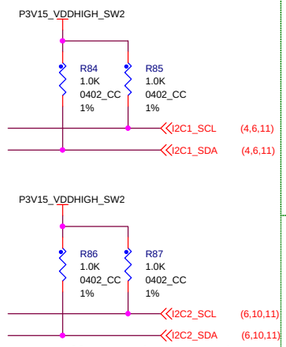
USB_5V_OTG Enable
USB_5V_HOST Enable
Capacitive Touch Reset
SD1 Write Protect

LCD_Brightness

Debug LED

PMIC INT
SD3 Card Detect

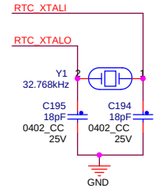
I2C pullups



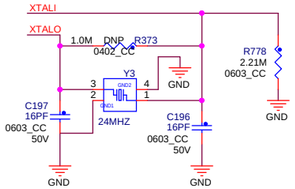
Note: Pull-up resistor must be sized to meet the signal rise times and also the Vil spec of all the bus components.

Due to board loadings this resistor was reduced. Validate your design, with the largest allowable resistor to reduce current usage.

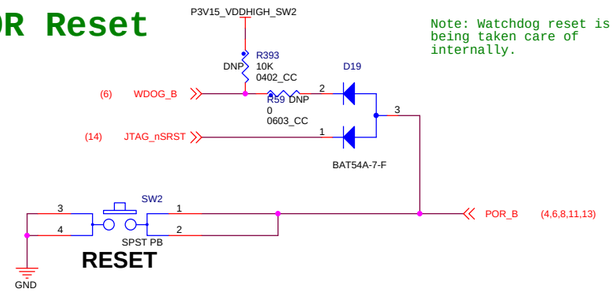
32.768kHz



24MHz

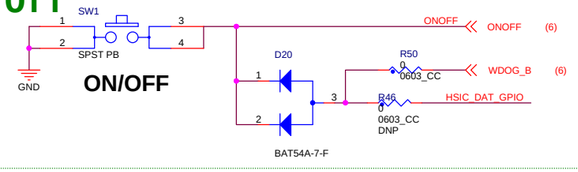


POR Reset



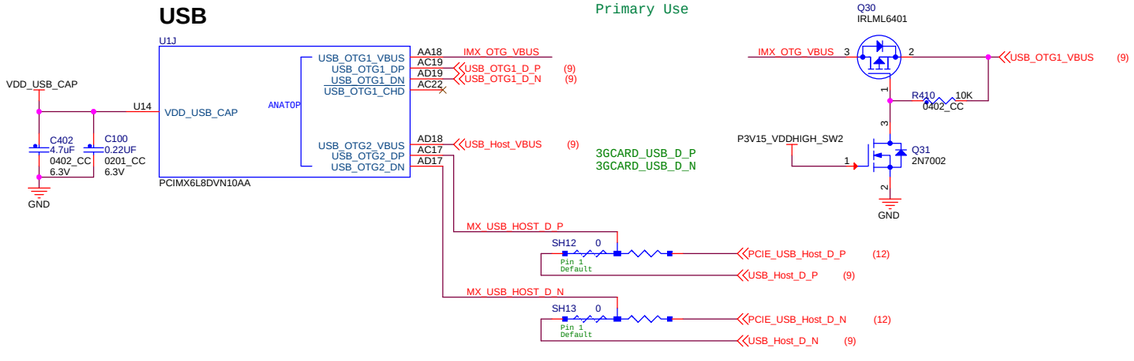
Note: Watchdog reset is being taken care of internally.

On/Off



USB

Primary Use



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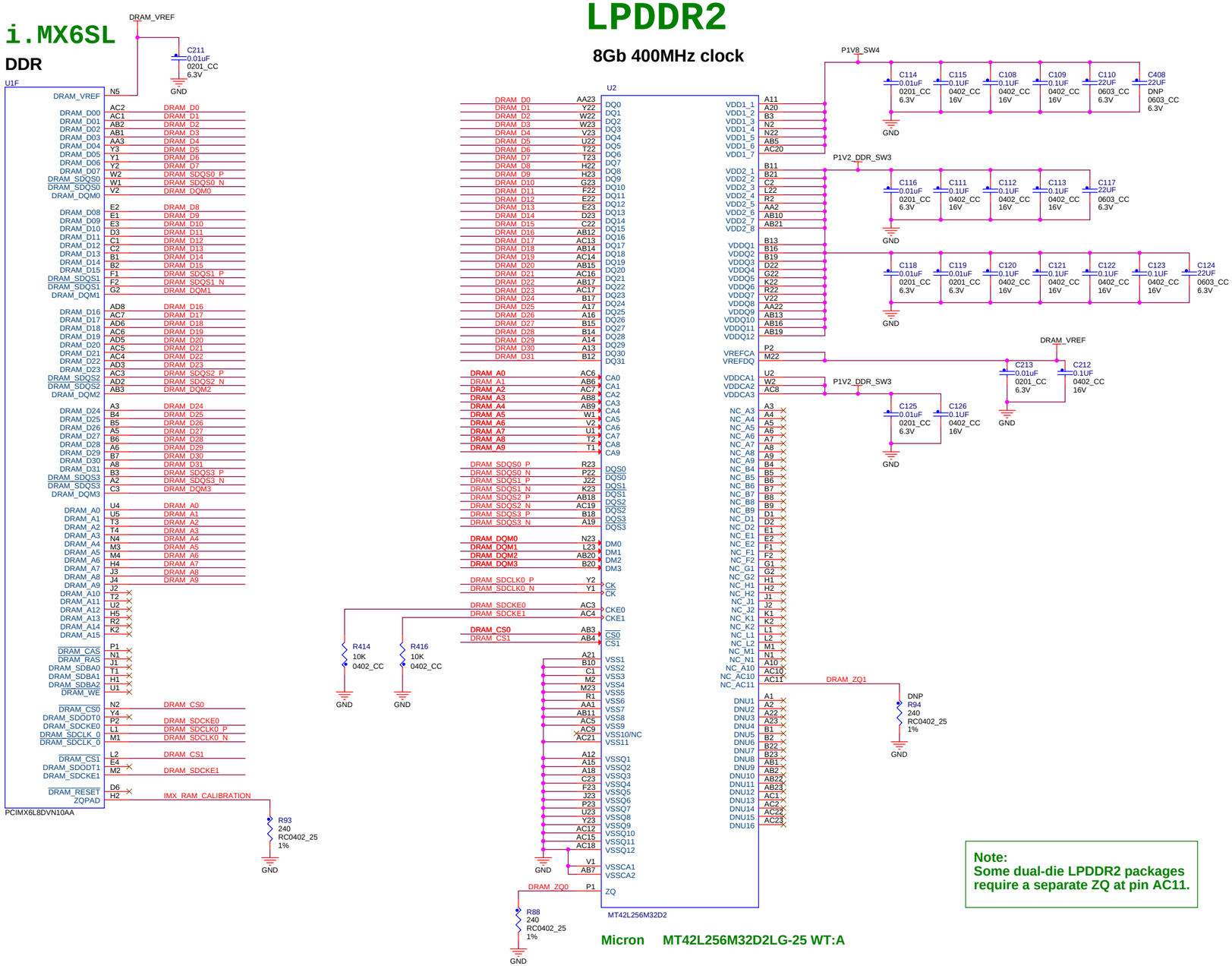
i.MX6SL

DDR

LPDDR2

8Gb 400MHz clock



Micron MT42L256M32D2LG-25 WT:A

Note:
Some dual-die LPDDR2 packages require a separate ZQ at pin AC11.

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Page Title: **LPDDR2**

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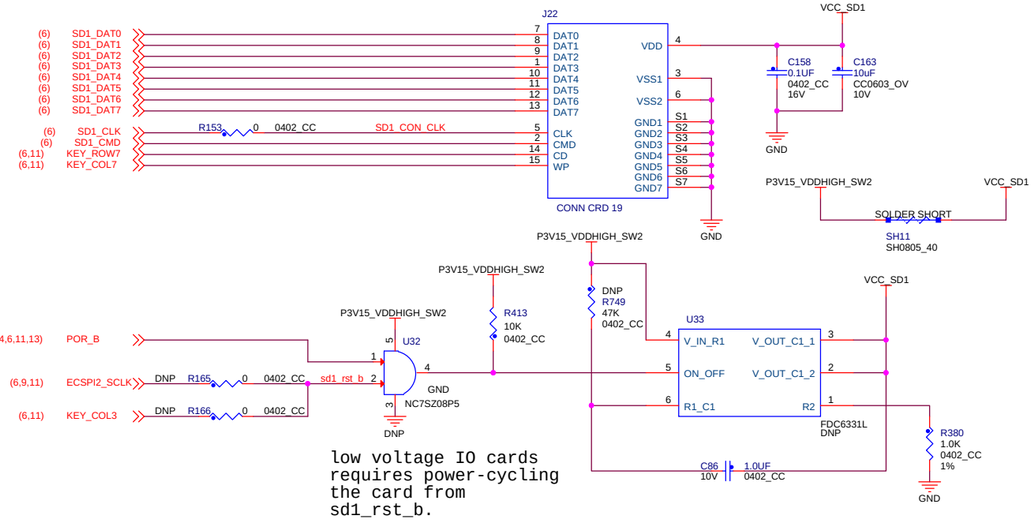
SD1 - For Primary External Card Slot

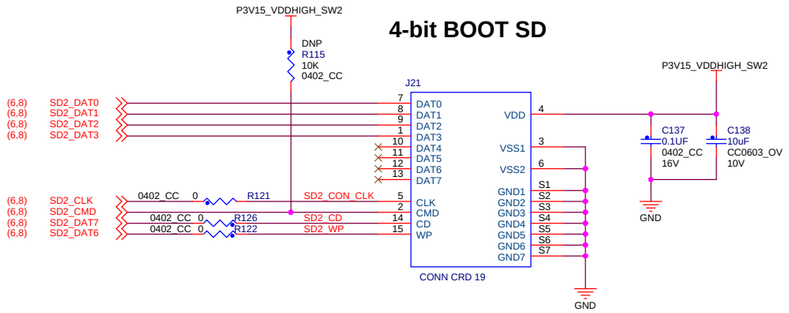
8-bit SD



low voltage IO cards requires power-cycling the card from sd1_rst_b.

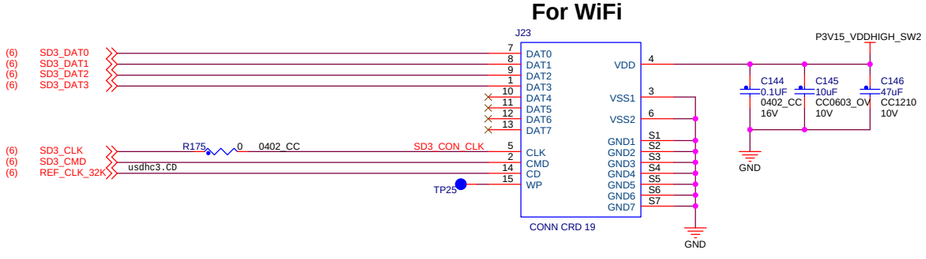
SD2 - For Boot Code

4-bit BOOT SD



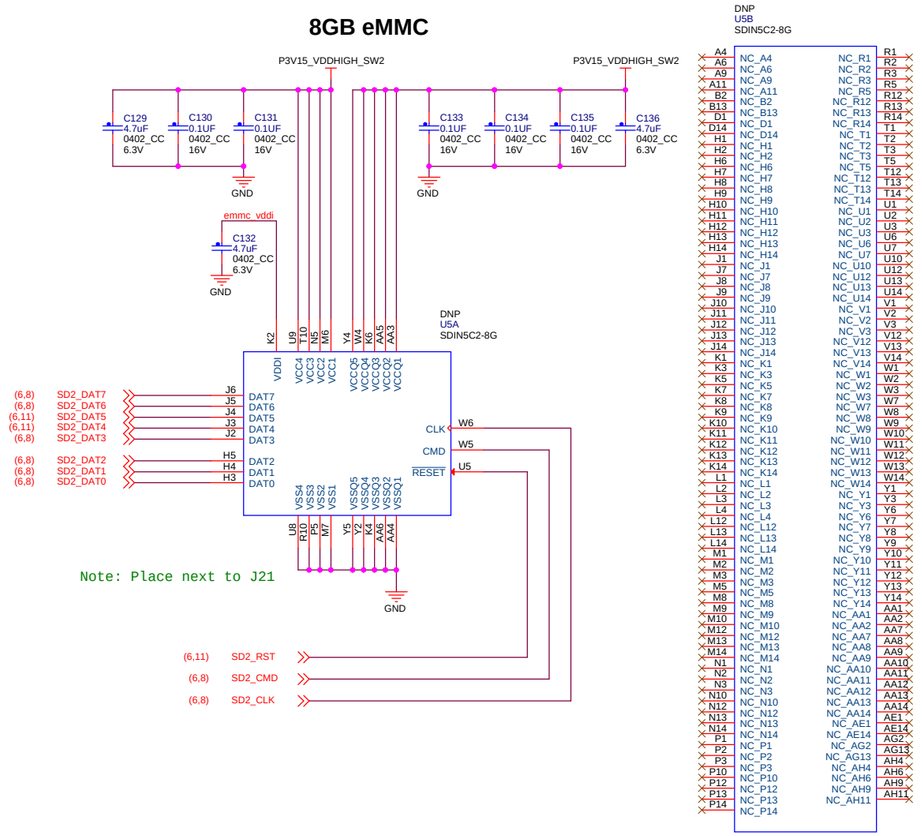
SD3 - for WiFi and SD Accessories

For WiFi

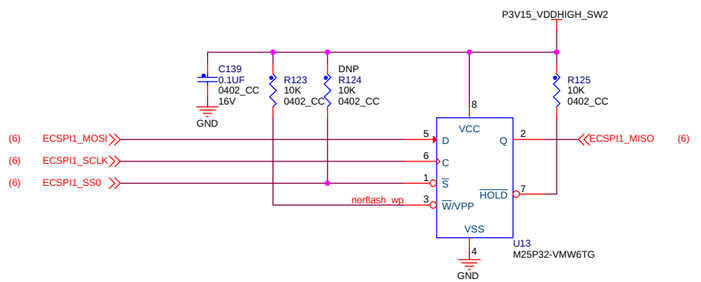


eMMC Footprint

8GB eMMC



4MB SPI NOR FLASH



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Page Title: **EMMC, SD and SPI NOR**

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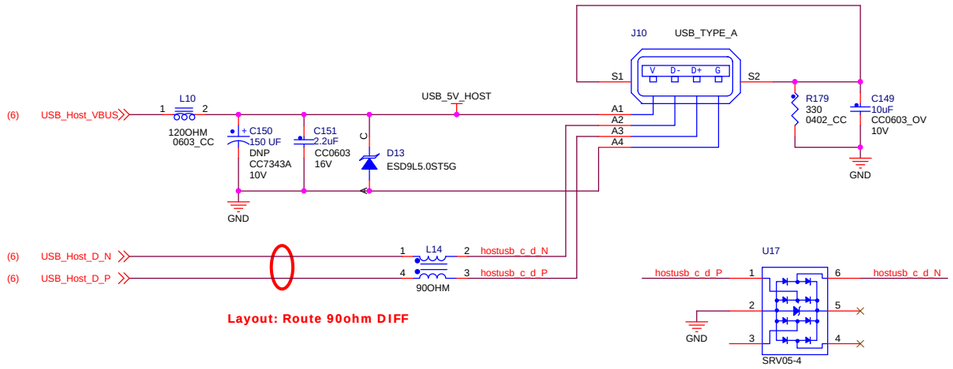
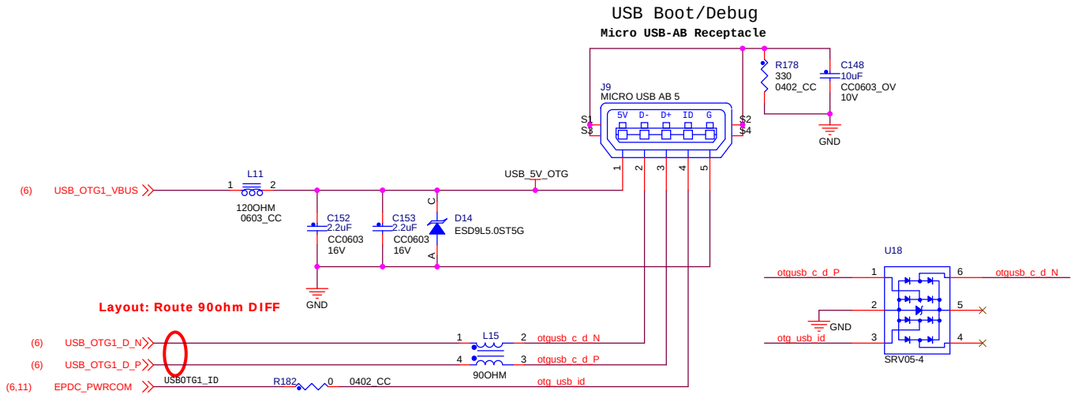
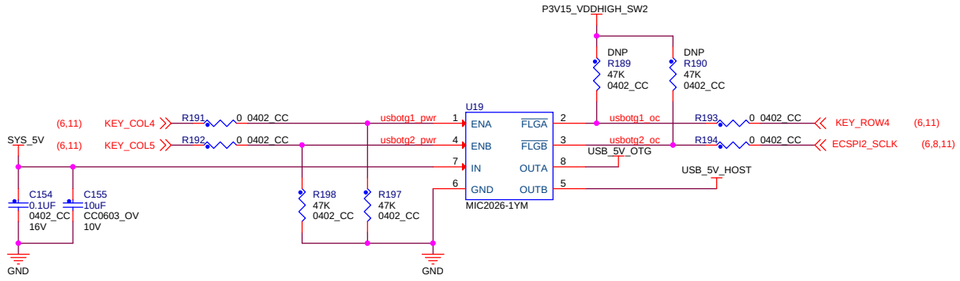
USB Host Port



USB Boot/Host/Device Port



USB 5V Control



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Audio CODEC

layout note:
Widen the trace SPKVDD
Max ~0.6A

PF0100_VIN → L18 120OHM 0603_CC → SPKVDD
C159 4.7uF 0603_CC 10V, C160 4.7uF 0603_CC 10V → GND
SPKVDD → U6 SPKVDD1, SPKVDD2

CODEC_1V8, CODEC_3V15
R779 DNP 0 0603_CC
R780 0 0603_CC → DBVDD
C215 0.1UF 0402_CC 16V → GND

P3V15_VDDHIGH_SW2 → SOLDER SHORT SH15 SH0805_40 → L19 120OHM 0603_CC → MICVDD
C165 4.7uF 0402_CC 6.3V → GND
MICVDD → A3 MICVDD

CODEC_1V8 → G2 DCVDD
C174 0.1UF 0402_CC 16V → GND

P1V8_VGEN3 → SOLDER SHORT SH16 SH0805_40 → L17 120OHM 0603_CC
CODEC_1V8
C164 4.7uF 0402_CC 6.3V, C161 4.7uF 0402_CC 6.3V, C162 4.7uF 0402_CC 6.3V → GND
A_CODEC_1V8 → D6 AVDD, C6 CPVDD, G4 PLLVDD

AGND D7, DGND F3, CPGND C7 → GND
SPKGND1 B1, SPKGND2 C1
PLLGND G5 → GND

When bypassing the I2C level shifter you must :
- change the DBVDD supply voltage to 3V15
- change the MX6SL IO pin supply voltage for all the codec digital pins
  - I2C2_SCL, & SDA
  - AUD_TXC, TXFS, TXD, RDX, & MCLK

MICBIAS → R720 2.2K 0402_CC
P4 OUT, GND → WM-64PCT
or WM-63PR
or CMC-2242PBL-A
C166 1.0UF 0402_CC 10V → GND
C147 0402_CC 1.0UF 10V
IN3R
IN1L C4, IN1R D4, IN2L D5, IN2R E5, IN3L F5, IN3R F6, IN4L E6, IN4R E7

CODEC_3V15, CODEC_1V8
C406 0.22UF 0201_CC 6.3V → GND
C407 0.22UF 0201_CC 6.3V → GND
U34 TXS0102 (VCCB, VCCA, GND, OE)
(6,11) I2C2_SCL → I2C2_SCL 8 B1 → A1 5 → codec_i2c_scl → SCLK F1
(6,11) I2C2_SDA → I2C2_SDA 1 B2 → A2 4 → codec_i2c_sda → SDA E2
CIFMODE F2 → GND
OE 6 → CODEC_1V8
R781 1.0K DNP 1% 0402_CC, R782 1.0K DNP 1% 0402_CC
I2C2_SCL → R216 DNP 0 0402_CC
I2C2_SDA → R215 DNP 0 0402_CC

(6) AUD_TXC → BCLK E1
(6) AUD_TXFS → LRCLK D3
(6) AUD_TXD → DACDAT D1
(6) AUD_RXD → ADCDAT D2
(6) AUD_MCLK → MCLK/XTI G7
XTO F7
WM8962

If you do not have any other devices at greater than 1.8V on the I2C bus, you can set the powers to 1.8V and bypass the level shifter. You will need to remove the 3V15 pull-ups on sheet 6 (R86 and R87).

HeadPhone

CODEC_3V15 → DNP R206 10K 0402_CC
J130 Audio Jack
(6) FEC_RX_ER → HP_DET → HPOUTL 6 4
HPOUTL B5 → HPOUTR 1 5
HPOUTR A5, HPOUTFB B4 → GND
C216 0.1UF 0402_CC 16V, C217 0.1UF 0402_CC 16V → GND
HPOUTL_ZOBEL → R771 20 RC0603 → GND
HPOUTR_ZOBEL → R772 20 RC0603 → GND
HPOUTL → DNP R204 10K 0402_CC → GND
HPOUTR → DNP R205 10K 0402_CC → GND

Layout note:
Zobel Networks(c216,c217,r771,r772) close to WM8962

Speaker Out

CON4 HDR 1X4 DNP
4 SPKOUTLP, 3 SPKOUTLN, 2 SPKOUTRP, 1 SPKOUTRN
CON500 SM04B-SRSS-TB
SIDE2, SIDE1, MECH

SPKOUTLN B3, SPKOUTLP A1
SPKOUTRN C3, SPKOUTRP B2

CPCA B6 → C374 2.2uF CC0603 16V → GND
layout note:
the positioning of C374 is very important
should be as close to the WM8962 as possible.
CPCB B7, CPVOUTN A7, CPVOUTP A6
C375 2.2uF CC0603 16V → GND
C376 2.2uF CC0603 16V → GND

CLKOUT2/GPIO2 E4, CLKOUT3/GPIO3 F4, GPIO5 G1, CS/GPIO6 E3
R207 10K 0402_CC → GND
CLKOUT5 G6

VMIDC C5 → GND
MICBIAS A4 → codec_vmidc → MICBIAS
C156 1.0UF 0402_CC 10V → GND
C157 4.7UF 0402_CC 6.3V → GND

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___
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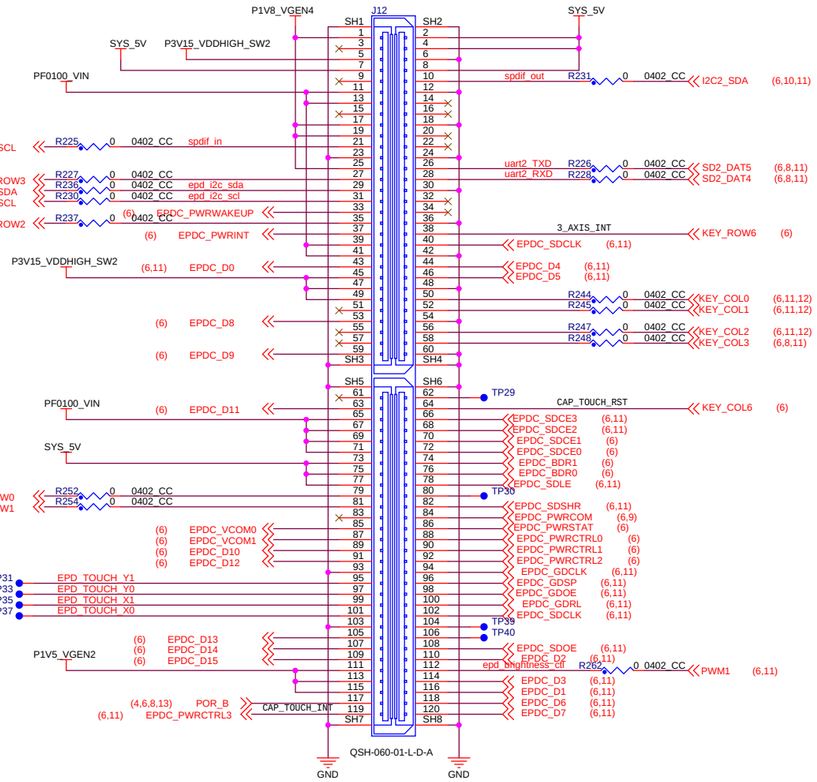
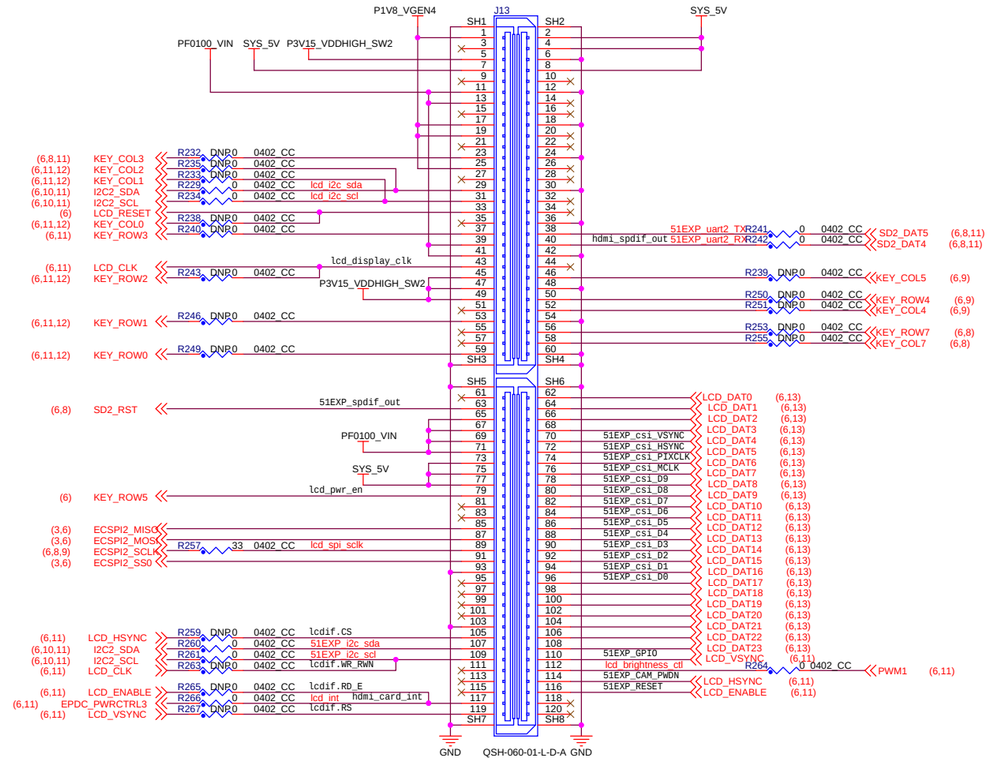
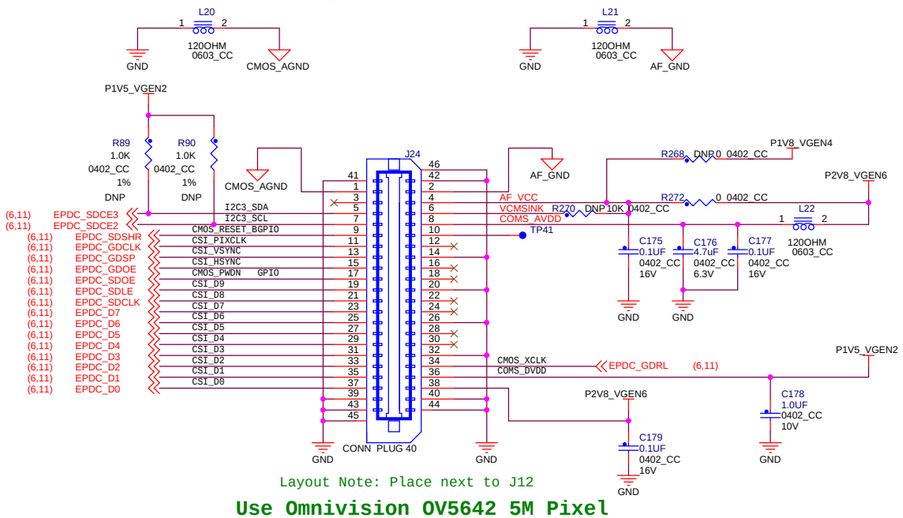
EPDC Expansion Port



LCD Expansion Port



Camera Expansion Connector



Layout Note: Place next to J12

Use Omnivision OV5642 5M Pixel Sensor with this connector (not included)

Important Note:

The camera connector (J24) and the EPDC connector (J12) share the same signals and CANNOT be used at the same time.

One of these two peripherals MUST BE REMOVED when a developer wishes to use the other.

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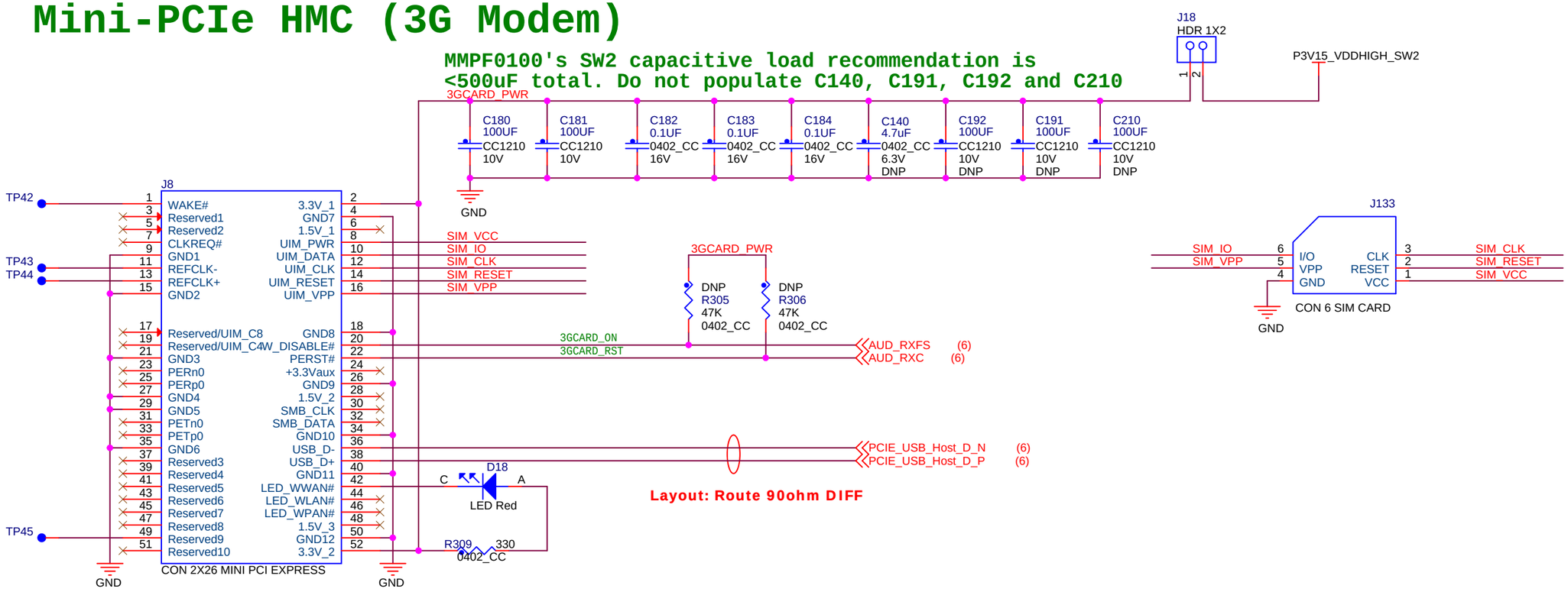
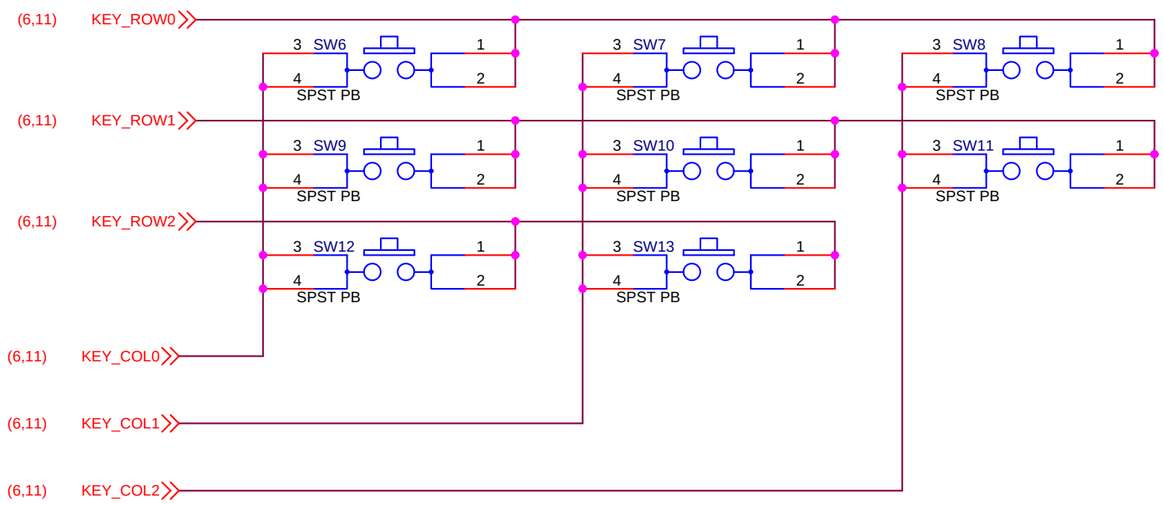
Mini-PCIe HMC (3G Modem)

MMPF0100's SW2 capacitive load recommendation is <500uF total. Do not populate C140, C191, C192 and C210



Button Matrix



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Drawing Title: **MCIMX6SLEVK board**

Page Title: **Wireless**

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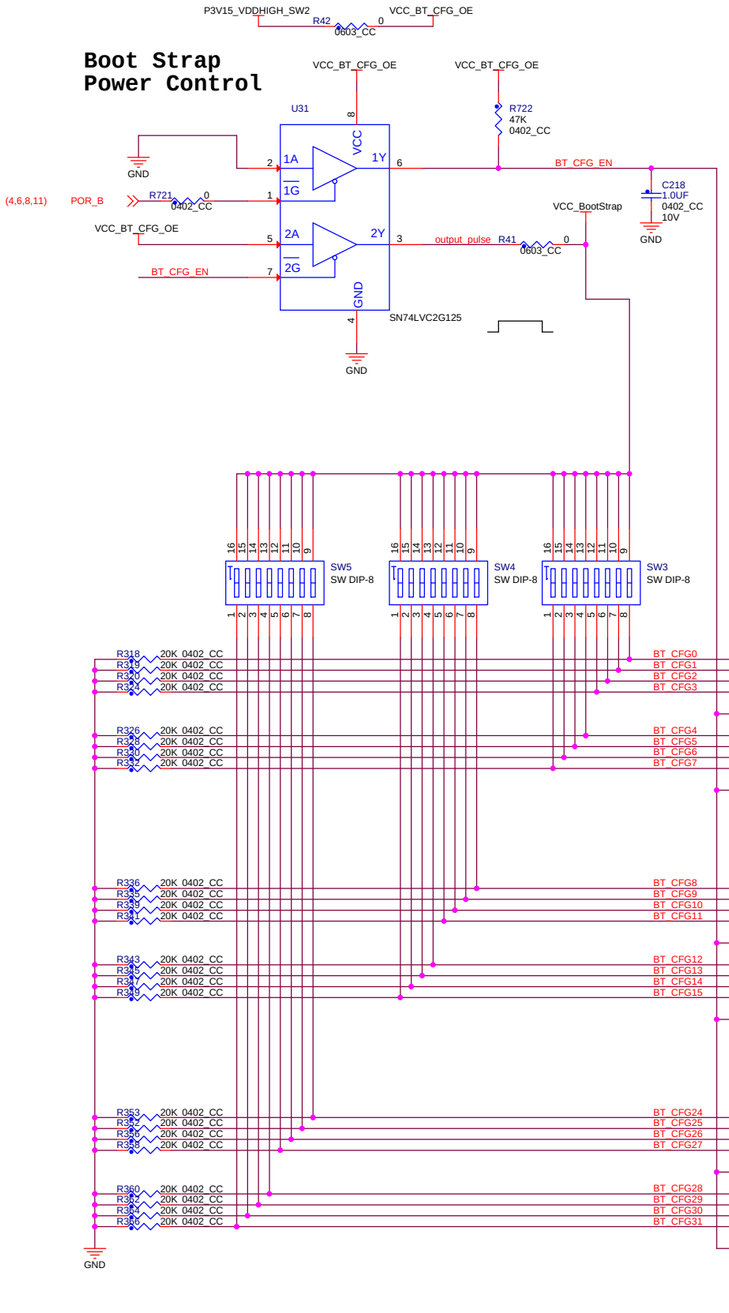
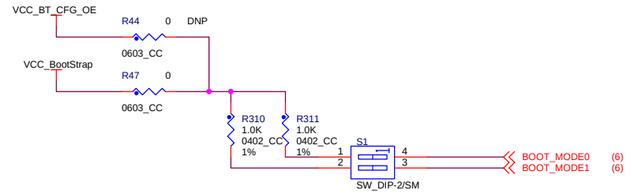
ot Strap

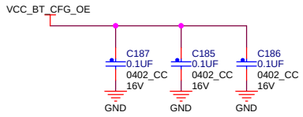
Boot Strap Power Control



Note:
i.MX6SL reads values approximately 300uS to 1mS after reset released. Buffers are active while unit is in reset and 1ms-10ms after reset is released.

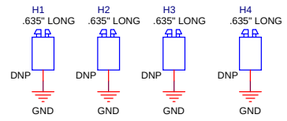
Boot Strap Primary Switches





Bus isolation

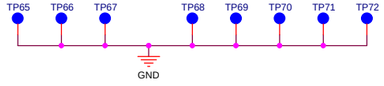
Board Mounting Holes for 4-40 Screws



IMPORTANT NOTE :

Use non metalic or non conducting standoff to avoid board damage due to GND potential difference with chasis.

GND TEST POINTS



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Drawing Title: **MCIMX6SLEVK board**

Page Title: **MISC**

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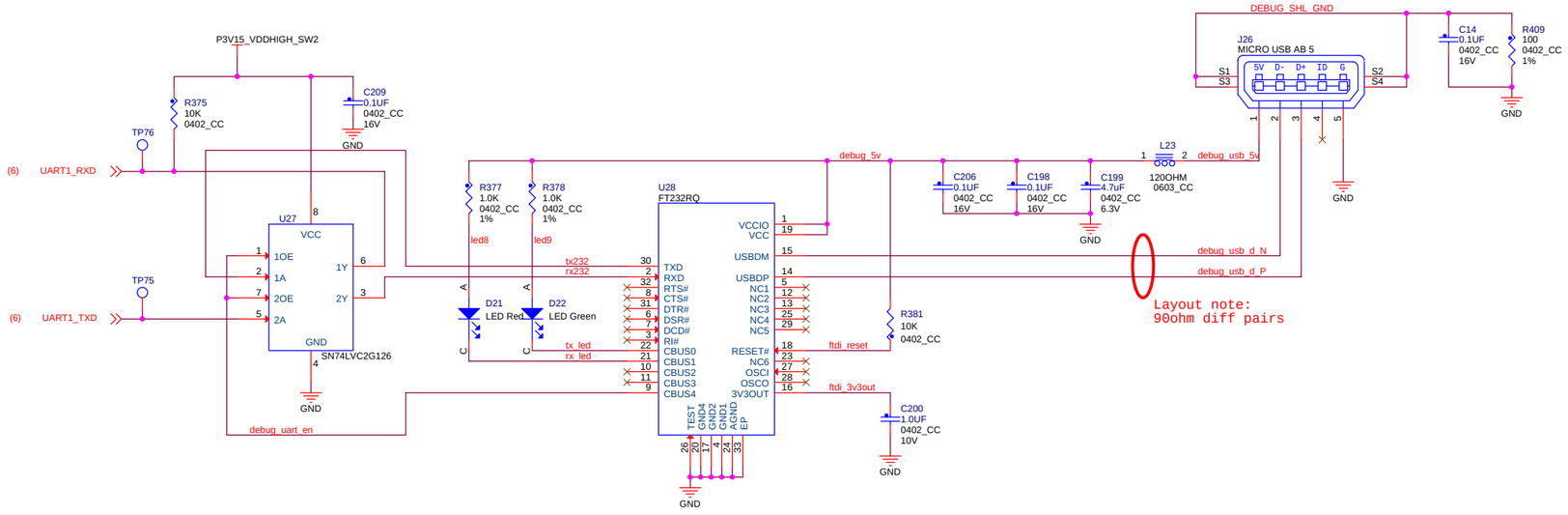
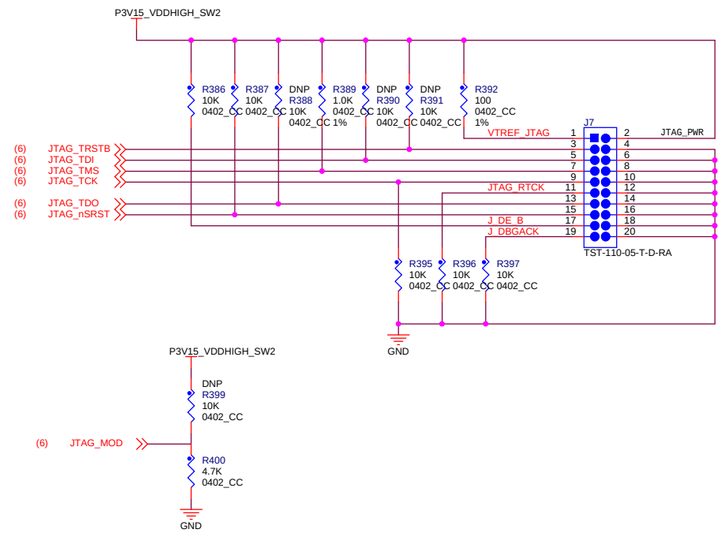
Debug UART2USB Converter

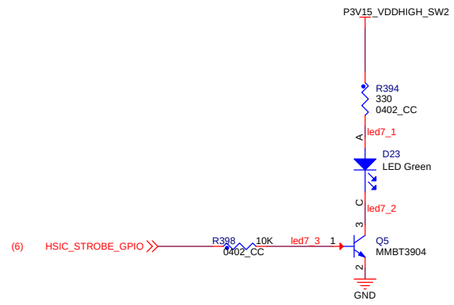


For driver installation, please refer to
http://www.ftdichip.com/Documents/InstallGuides.htm

JTAG



Debug LED



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ICAP Classification: FCP: ___ FIUO: X PUBI: ___			
Drawing Title: MCIMX6SLEVK board			
Page Title: UART & JTAG			
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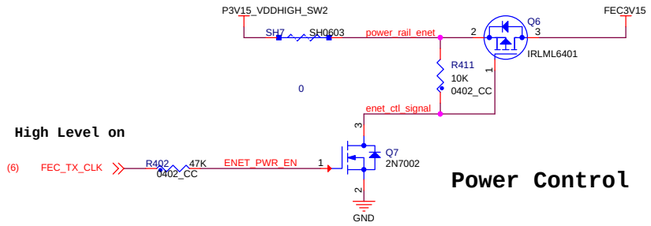
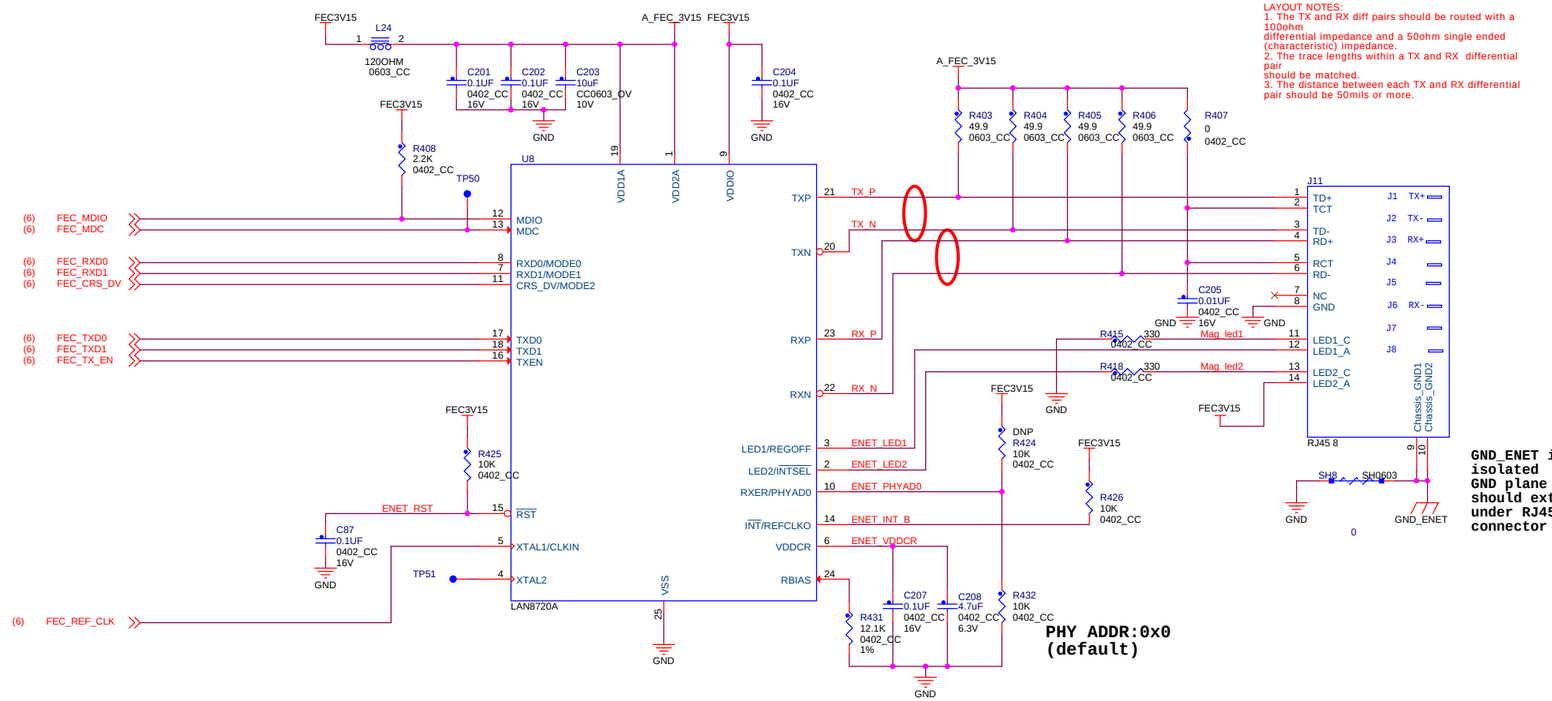


Ethernet



freescale		
ICAP Classification: FCP: ___ FIUO: X PUBI: ___		
Drawing Title: MCIMX6SLEVK board		
Page Title: ENET		
Size: C	Document Number: SCH-27452 PDF: SPF-27452	Rev: B
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IOMUX Table

PIN NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
WDOG_B	wdog1.WDOG_B	wdog1.WDOG_RST_B_DEB	uart5.RI			gpio3.GPIO[18]		observe_mux.OUT[2]
HSIC_DAT	usb.H_DATA	i2c1.SCL	pwm1.PWMO	anatop.ANATOP_24M_OUT	osc32k.32K_OUT	gpio3.GPIO[19]		
HSIC_STROBE	usb.H_STROBE	i2c1.SDA	pwm2.PWMO	anatop.ANATOP_32K_OUT		gpio3.GPIO[20]		
REF_CLK_24M	anatop.ANATOP_24M_OUT	i2c3.SCL	pwm3.PWMO	anatop.USBOTG2_ID	ccm.PMIC_RDY	gpio3.GPIO[21]	usdhc3.WP	mmdc.MMDC_DEBUG[49]
REF_CLK_32K	anatop.ANATOP_32K_OUT	i2c3.SDA	pwm4.PWMO	anatop.USBOTG1_ID	usdhc1.LCTL	gpio3.GPIO[22]	usdhc3.CD	observe_mux.OUT[3]
PWM1	pwm1.PWMO	ccm.CLKO	audmux.AUDIO_CLK_OUT	fec.REF_OUT	csi.MCLK	gpio3.GPIO[23]	epit1.EPITO	observe_mux.OUT[4]
KEY_COL0	kpp.COL[0]	i2c2.SCL	lcdif.DAT[0]	weim.WEIM_DA_A[0]	usdhc1.CD	gpio3.GPIO[24]		tpsmp.HDATA[0]
KEY_ROW0	kpp.ROW[0]	i2c2.SDA	lcdif.DAT[1]	weim.WEIM_DA_A[1]	usdhc1.WP	gpio3.GPIO[25]		tpsmp.HDATA[1]
KEY_COL1	kpp.COL[1]	ecspi4.MOSI	lcdif.DAT[2]	weim.WEIM_DA_A[2]	usdhc3.DAT4	gpio3.GPIO[26]		tpsmp.HDATA[2]
KEY_ROW1	kpp.ROW[1]	ecspi4.MISO	lcdif.DAT[3]	weim.WEIM_DA_A[3]	usdhc3.DAT5	gpio3.GPIO[27]		tpsmp.HDATA[3]
KEY_COL2	kpp.COL[2]	ecspi4.SS0	lcdif.DAT[4]	weim.WEIM_DA_A[4]	usdhc3.DAT6	gpio3.GPIO[28]		tpsmp.HDATA[4]
KEY_ROW2	kpp.ROW[2]	ecspi4.SCLK	lcdif.DAT[5]	weim.WEIM_DA_A[5]	usdhc3.DAT7	gpio3.GPIO[29]		tpsmp.HDATA[5]
KEY_COL3	kpp.COL[3]	audmux.AUD6_RXFS	lcdif.DAT[6]	weim.WEIM_DA_A[6]	usdhc4.DAT6	gpio3.GPIO[30]	usdhc1.RST	tpsmp.HDATA[6]
KEY_ROW3	kpp.ROW[3]	audmux.AUD6_RXC	lcdif.DAT[7]	weim.WEIM_DA_A[7]	usdhc4.DAT7	gpio3.GPIO[31]	usdhc1.VSELECT	tpsmp.HDATA[7]
KEY_COL4	kpp.COL[4]	audmux.AUD6_RXD	lcdif.DAT[8]	weim.WEIM_DA_A[8]	usdhc4.CLK	gpio4.GPIO[0]	usb.USBOTG1_PWR	tpsmp.HDATA[8]
KEY_ROW4	kpp.ROW[4]	audmux.AUD6_TXC	lcdif.DAT[9]	weim.WEIM_DA_A[9]	usdhc4.CMD	gpio4.GPIO[1]	usb.USBOTG1_OC	tpsmp.HDATA[9]
KEY_COL5	kpp.COL[5]	audmux.AUD6_TXFS	lcdif.DAT[10]	weim.WEIM_DA_A[10]	usdhc4.DAT0	gpio4.GPIO[2]	usb.USBOTG2_PWR	tpsmp.HDATA[10]
KEY_ROW5	kpp.ROW[5]	audmux.AUD6_TXD	lcdif.DAT[11]	weim.WEIM_DA_A[11]	usdhc4.DAT1	gpio4.GPIO[3]	usb.USBOTG2_OC	tpsmp.HDATA[11]
KEY_COL6	kpp.COL[6]	uart4.RXD_MUX	lcdif.DAT[12]	weim.WEIM_DA_A[12]	usdhc4.DAT2	gpio4.GPIO[4]	usdhc3.RST	tpsmp.HDATA[12]
KEY_ROW6	kpp.ROW[6]	uart4.TXD_MUX	lcdif.DAT[13]	weim.WEIM_DA_A[13]	usdhc4.DAT3	gpio4.GPIO[5]	usdhc3.VSELECT	tpsmp.HDATA[13]
KEY_COL7	kpp.COL[7]	uart4.RTS	lcdif.DAT[14]	weim.WEIM_DA_A[14]	usdhc4.DAT4	gpio4.GPIO[6]	usdhc1.WP	tpsmp.HDATA[14]
KEY_ROW7	kpp.ROW[7]	uart4.CTS	lcdif.DAT[15]	weim.WEIM_DA_A[15]	usdhc4.DAT5	gpio4.GPIO[7]	usdhc1.CD	tpsmp.HDATA[15]
EPDC_D0	epdc.SDDO[0]	ecspi4.MOSI	lcdif.DAT[24]	csi.D[0]	tcon.E_DATA[0]	gpio1.GPIO[7]	anatop.USBPHY1_TSTI_TX_HS_MODE	observe_mux.OUT[0]
EPDC_D1	epdc.SDDO[1]	ecspi4.MISO	lcdif.DAT[25]	csi.D[1]	tcon.E_DATA[1]	gpio1.GPIO[8]	anatop.USBPHY1_TSTI_TX_LS_MODE	observe_mux.OUT[1]
EPDC_D2	epdc.SDDO[2]	ecspi4.SS0	lcdif.DAT[26]	csi.D[2]	tcon.E_DATA[2]	gpio1.GPIO[9]	anatop.USBPHY1_TSTI_TX_DN	tpsmp.HDATA[28]
EPDC_D3	epdc.SDDO[3]	ecspi4.SCLK	lcdif.DAT[27]	csi.D[3]	tcon.E_DATA[3]	gpio1.GPIO[10]	anatop.USBPHY1_TSTI_TX_DP	tpsmp.HDATA[29]
EPDC_D4	epdc.SDDO[4]	ecspi4.SS1	lcdif.DAT[28]	csi.D[4]	tcon.E_DATA[4]	gpio1.GPIO[11]	anatop.USBPHY1_TSTI_TX_EN	tpsmp.HDATA[30]
EPDC_D5	epdc.SDDO[5]	ecspi4.SS2	lcdif.DAT[29]	csi.D[5]	tcon.E_DATA[5]	gpio1.GPIO[12]	anatop.USBPHY1_TSTI_TX_HIZ	tpsmp.HDATA[31]
EPDC_D6	epdc.SDDO[6]	ecspi4.SS3	lcdif.DAT[30]	csi.D[6]	tcon.E_DATA[6]	gpio1.GPIO[13]	anatop.USBPHY2_TSTO_RX_DISCON_DET	mmdc.MMDC_DEBUG[40]
EPDC_D7	epdc.SDDO[7]	ecspi4.RDY	lcdif.DAT[31]	csi.D[7]	tcon.E_DATA[7]	gpio1.GPIO[14]	anatop.USBPHY2_TSTO_RX_FS_RXD	mmdc.MMDC_DEBUG[32]
EPDC_D8	epdc.SDDO[8]	ecspi3.MOSI	epdc.PWRCTRL[0]	weim.WEIM_A[16]	tcon.E_DATA[8]	gpio1.GPIO[15]	usdhc4.RST	mmdc.MMDC_DEBUG[31]
EPDC_D9	epdc.SDDO[9]	ecspi3.MISO	epdc.PWRCTRL[1]	weim.WEIM_A[17]	tcon.E_DATA[9]	gpio1.GPIO[16]	usdhc4.VSELECT	mmdc.MMDC_DEBUG[30]
EPDC_D10	epdc.SDDO[10]	ecspi3.SS0	epdc.PWRCTRL[2]	weim.WEIM_A[18]	tcon.E_DATA[10]	gpio1.GPIO[17]	usdhc4.WP	mmdc.MMDC_DEBUG[29]
EPDC_D11	epdc.SDDO[11]	ecspi3.SCLK	epdc.PWRCTRL[3]	weim.WEIM_A[19]	tcon.E_DATA[11]	gpio1.GPIO[18]	usdhc4.CD	mmdc.MMDC_DEBUG[28]
EPDC_D12	epdc.SDDO[12]	uart2.RXD_MUX	epdc.PWRCOM	weim.WEIM_A[20]	tcon.E_DATA[12]	gpio1.GPIO[19]	ecspi3.SS1	mmdc.MMDC_DEBUG[27]
EPDC_D13	epdc.SDDO[13]	uart2.TXD_MUX	epdc.PWRIRQ	weim.WEIM_A[21]	tcon.E_DATA[13]	gpio1.GPIO[20]	ecspi3.SS2	mmdc.MMDC_DEBUG[26]
EPDC_D14	epdc.SDDO[14]	uart2.RTS	epdc.PWRSTAT	weim.WEIM_A[22]	tcon.E_DATA[14]	gpio1.GPIO[21]	ecspi3.SS3	mmdc.MMDC_DEBUG[25]
EPDC_D15	epdc.SDDO[15]	uart2.CTS	epdc.PWRWAKE	weim.WEIM_A[23]	tcon.E_DATA[15]	gpio1.GPIO[22]	ecspi3.RDY	mmdc.MMDC_DEBUG[24]
EPDC_SDCLK	epdc.SDCLK	ecspi2.MOSI	i2c2.SCL	csi.D[8]	tcon.CL	gpio1.GPIO[23]	anatop.USBPHY2_TSTO_RX_HS_RXD	mmdc.MMDC_DEBUG[23]
EPDC_SDLE	epdc.SDLE	ecspi2.MISO	i2c2.SDA	csi.D[9]	tcon.LD	gpio1.GPIO[24]	anatop.USBPHY2_TSTO_RX_SQUELCH	mmdc.MMDC_DEBUG[22]
EPDC_SDOE	epdc.SDOE	ecspi2.SS0	tcon.XDIOR	csi.D[10]	tcon.XDIOL	gpio1.GPIO[25]	anatop.USBPHY2_TSTO_PLL_CLK20DIV	mmdc.MMDC_DEBUG[21]
EPDC_SDSHR	epdc.SDSHR	ecspi2.SCLK	epdc.SDCE[4]	csi.D[11]	tcon.XDIOR	gpio1.GPIO[26]	anatop.USBPHY1_TSTO_RX_DISCON_DET	mmdc.MMDC_DEBUG[20]
EPDC_SDCE0	epdc.SDCE[0]	ecspi2.SS1	pwm3.PWMO	weim.WEIM_CS[2]	tcon.YCKR	gpio1.GPIO[27]	anatop.USBPHY1_TSTO_PLL_CLK20DIV	mmdc.MMDC_DEBUG[19]
EPDC_SDCE1	epdc.SDCE[1]	wdog2.WDOG_B	pwm4.PWMO	weim.WEIM_LBA	tcon.YOER	gpio1.GPIO[28]	anatop.USBPHY1_TSTO_RX_FS_RXD	mmdc.MMDC_DEBUG[18]
EPDC_SDCE2	epdc.SDCE[2]	i2c3.SCL	pwm1.PWMO	weim.WEIM_EB[0]	tcon.YDIOUR	gpio1.GPIO[29]	anatop.USBPHY1_TSTO_RX_HS_RXD	mmdc.MMDC_DEBUG[17]
EPDC_SDCE3	epdc.SDCE[3]	i2c3.SDA	pwm2.PWMO	weim.WEIM_EB[1]	tcon.YDIODR	gpio1.GPIO[30]	anatop.USBPHY1_TSTO_RX_SQUELCH	mmdc.MMDC_DEBUG[16]
EPDC_GDCLK	epdc.GDCLK	ecspi2.SS2	tcon.YCKR	csi.PIXCLK	tcon.YCKL	gpio1.GPIO[31]	usdhc2.RST	mmdc.MMDC_DEBUG[15]
EPDC_GDOE	epdc.GDOE	ecspi2.SS3	tcon.YOER	csi.HSYNC	tcon.YOEL	gpio2.GPIO[0]	usdhc2.VSELECT	mmdc.MMDC_DEBUG[14]
EPDC_GDRL	epdc.GDRL	ecspi2.RDY	tcon.YDIOUR	csi.MCLK	tcon.YDIOUL	gpio2.GPIO[1]	usdhc2.WP	mmdc.MMDC_DEBUG[13]
EPDC_GDSP	epdc.GDSP	pwm4.PWMO	tcon.YDIODR	csi.VSYNC	tcon.YDIODL	gpio2.GPIO[2]	usdhc2.CD	mmdc.MMDC_DEBUG[12]
EPDC_VCOM0	epdc.VCOM[0]	audmux.AUD5_RXFS	uart3.RXD_MUX	weim.WEIM_A[24]	tcon.VCOM[0]	gpio2.GPIO[3]	epdc.SDCE[5]	mmdc.MMDC_DEBUG[11]
EPDC_VCOM1	epdc.VCOM[1]	audmux.AUD5_RXD	uart3.TXD_MUX	weim.WEIM_A[25]	tcon.VCOM[1]	gpio2.GPIO[4]	epdc.SDCE[6]	mmdc.MMDC_DEBUG[10]
EPDC_BDR0	epdc.BDR[0]	usdhc4.CLK	uart3.RTS	weim.WEIM_A[26]	tcon.RL	gpio2.GPIO[5]	epdc.SDCE[7]	mmdc.MMDC_DEBUG[9]
EPDC_BDR1	epdc.BDR[1]	usdhc4.CMD	uart3.CTS	weim.WEIM_CRE	tcon.UD	gpio2.GPIO[6]	epdc.SDCE[8]	mmdc.MMDC_DEBUG[8]
EPDC_PWRCTRL0	epdc.PWRCTRL[0]	audmux.AUD5_RXC	lcdif.DAT[16]	weim.WEIM_RW	tcon.YCKL	gpio2.GPIO[7]	usdhc4.RST	mmdc.MMDC_DEBUG[7]
EPDC_PWRCTRL1	epdc.PWRCTRL[1]	audmux.AUD5_TXFS	lcdif.DAT[17]	weim.WEIM_OE	tcon.YOEL	gpio2.GPIO[8]	usdhc4.VSELECT	mmdc.MMDC_DEBUG[6]
EPDC_PWRCTRL2	epdc.PWRCTRL[2]	audmux.AUD5_TXD	lcdif.DAT[18]	weim.WEIM_CS[0]	tcon.YDIOUL	gpio2.GPIO[9]	usdhc4.WP	mmdc.MMDC_DEBUG[5]
EPDC_PWRCTRL3	epdc.PWRCTRL[3]	audmux.AUD5_TXC	lcdif.DAT[19]	weim.WEIM_CS[1]	tcon.YDIODL	gpio2.GPIO[10]	usdhc4.CD	mmdc.MMDC_DEBUG[4]
EPDC_PWRCOM	epdc.PWRCOM	usdhc4.DAT0	lcdif.DAT[20]	weim.WEIM_BCLK	anatop.USBOTG1_ID	gpio2.GPIO[11]	usdhc3.RST	mmdc.MMDC_DEBUG[3]
EPDC_PWRINT	epdc.PWRIRQ	usdhc4.DAT1	lcdif.DAT[21]	weim.ACLK_FREERUN	anatop.USBOTG2_ID	gpio2.GPIO[12]	usdhc3.VSELECT	mmdc.MMDC_DEBUG[2]
EPDC_PWRSTAT	epdc.PWRSTAT	usdhc4.DAT2	lcdif.DAT[22]	weim.WEIM_WAIT	kitten.EVENTI	gpio2.GPIO[13]	usdhc3.WP	mmdc.MMDC_DEBUG[1]
EPDC_PWRWAKEUP	epdc.PWRWAKE	usdhc4.DAT3	lcdif.DAT[23]	weim.WEIM_DTACK_B	kitten.EVENTO	gpio2.GPIO[14]	usdhc3.CD	mmdc.MMDC_DEBUG[0]
LCD_CLK	lcdif.CLK	usdhc4.DAT4	lcdif.WR_RWN	weim.WEIM_RW	pwm4.PWMO	gpio2.GPIO[15]	src.EARLY_RST	tpsmp.HTRANS[0]
LCD_ENABLE	lcdif.ENABLE	usdhc4.DAT5	lcdif.RD_E	weim.WEIM_OE	uart2.RXD_MUX	gpio2.GPIO[16]	ocotp_ctrl_wrapper.FUSE_LATCHED	tpsmp.HTRANS[1]
LCD_HSYNC	lcdif.HSYNC	usdhc4.DAT6	lcdif.CS	weim.WEIM_CS[0]	uart2.TXD_MUX	gpio2.GPIO[17]	kitten.TRCLK	tpsmp.HDATA[16]
LCD_VSYNC	lcdif.VSYNC	usdhc4.DAT7	lcdif.RS	weim.WEIM_CS[1]	uart2.RTS	gpio2.GPIO[18]	kitten.TRCTL	tpsmp.HDATA[17]
LCD_RESET	lcdif.RESET	weim.WEIM_DTACK_B	lcdif.BUSY	weim.WEIM_WAIT	uart2.CTS	gpio2.GPIO[19]	ccm.PMIC_RDY	tpsmp.HDATA_DIR
LCD_DAT0	lcdif.DAT[0]	ecspi1.MOSI	anatop.USBOTG2_ID	pwm1.PWMO	uart5.DTR	gpio2.GPIO[20]	kitten.TRACE[0]	src.BT_CFG[0]
LCD_DAT1	lcdif.DAT[1]	ecspi1.MISO	anatop.USBOTG1_ID	pwm2.PWMO	audmux.AUD4_RXFS	gpio2.GPIO[21]	kitten.TRACE[1]	src.BT_CFG[1]
LCD_DAT2	lcdif.DAT[2]	ecspi1.SS0	epit2.EPITO	pwm3.PWMO	audmux.AUD4_RXC	gpio2.GPIO[22]	kitten.TRACE[2]	src.BT_CFG[2]
LCD_DAT3	lcdif.DAT[3]	ecspi1.SCLK	uart5.DSR	pwm4.PWMO	audmux.AUD4_RXD	gpio2.GPIO[23]	kitten.TRACE[3]	src.BT_CFG[3]
LCD_DAT4	lcdif.DAT[4]	ecspi1.SS1	csi.VSYNC	wdog2.WDOG_RST_B_DEB	audmux.AUD4_TXC	gpio2.GPIO[24]	kitten.TRACE[4]	src.BT_CFG[4]
LCD_DAT5	lcdif.DAT[5]	ecspi1.SS2	csi.HSYNC	weim.WEIM_CS[3]	audmux.AUD4_TXFS	gpio2.GPIO[25]	kitten.TRACE[5]	src.BT_CFG[5]
LCD_DAT6	lcdif.DAT[6]	ecspi1.SS3	csi.PIXCLK	weim.WEIM_D[0]	audmux.AUD4_TXD	gpio2.GPIO[26]	kitten.TRACE[6]	src.BT_CFG[6]
LCD_DAT7	lcdif.DAT[7]	ecspi1.RDY	csi.MCLK	weim.WEIM_D[1]	audmux.AUDIO_CLK_OUT	gpio2.GPIO[27]	kitten.TRACE[7]	src.BT_CFG[7]
LCD_DAT8	lcdif.DAT[8]	kpp.COL[0]	csi.D[9]	weim.WEIM_D[2]	ecspi2.SCLK	gpio2.GPIO[28]	kitten.TRACE[8]	src.BT_CFG[8]
LCD_DAT9	lcdif.DAT[9]	kpp.ROW[0]	csi.D[8]	weim.WEIM_D[3]	ecspi2.MOSI	gpio2.GPIO[29]	kitten.TRACE[9]	src.BT_CFG[9]
LCD_DAT10	lcdif.DAT[10]	kpp.COL[1]	csi.D[7]	weim.WEIM_D[4]	ecspi2.MISO	gpio2.GPIO[30]	kitten.TRACE[10]	src.BT_CFG[10]
LCD_DAT11	lcdif.DAT[11]	kpp.ROW[1]	csi.D[6]	weim.WEIM_D[5]	ecspi2.SS1	gpio2.GPIO[31]	kitten.TRACE[11]	src.BT_CFG[11]
LCD_DAT12	lcdif.DAT[12]	kpp.COL[2]	csi.D[5]	weim.WEIM_D[6]	uart5.RTS	gpio3.GPIO[0]	kitten.TRACE[12]	src.BT_CFG[12]
LCD_DAT13	lcdif.DAT[13]	kpp.ROW[2]	csi.D[4]	weim.WEIM_D[7]	uart5.CTS	gpio3.GPIO[1]	kitten.TRACE[13]	src.BT_CFG[13]
LCD_DAT14	lcdif.DAT[14]	kpp.COL[3]	csi.D[3]	weim.WEIM_D[8]	uart5.RXD_MUX	gpio3.GPIO[2]	kitten.TRACE[14]	src.BT_CFG[14]
LCD_DAT15	lcdif.DAT[15]	kpp.ROW[3]	csi.D[2]	weim.WEIM_D[9]	uart5.TXD_MUX	gpio3.GPIO[3]	kitten.TRACE[15]	src.BT_CFG[15]
LCD_DAT16	lcdif.DAT[16]	kpp.COL[4]	csi.D[1]	weim.WEIM_D[10]	i2c2.SCL	gpio3.GPIO[4]	kitten.TRACE[16]	src.BT_CFG[24]
LCD_DAT17	lcdif.DAT[17]	kpp.ROW[4]	csi.D[0]	weim.WEIM_D[11]	i2c2.SDA	gpio3.GPIO[5]	kitten.TRACE[17]	src.BT_CFG[25]
LCD_DAT18	lcdif.DAT[18]	kpp.COL[5]	csi.D[15]	weim.WEIM_D[12]	gpt.CAPIN1	gpio3.GPIO[6]	kitten.TRACE[18]	src.BT_CFG[26]
LCD_DAT19	lcdif.DAT[19]	kpp.ROW[5]	csi.D[14]	weim.WEIM_D[13]	gpt.CAPIN2	gpio3.GPIO[7]	kitten.TRACE[19]	src.BT_CFG[27]
LCD_DAT20	lcdif.DAT[20]	kpp.COL[6]	csi.D[13]	weim.WEIM_D[14]	gpt.CMPOUT1	gpio3.GPIO[8]	kitten.TRACE[20]	src.BT_CFG[28]
LCD_DAT21	lcdif.DAT[21]	kpp.ROW[6]	csi.D[12]	weim.WEIM_D[15]	gpt.CMPOUT2	gpio3.GPIO[9]	kitten.TRACE[21]	src.BT_CFG[29]
LCD_DAT22	lcdif.DAT[22]	kpp.COL[7]	csi.D[11]	weim.WEIM_EB[3]	gpt.CMPOUT3	gpio3.GPIO[10]	kitten.TRACE[22]	src.BT_CFG[30]
LCD_DAT23	lcdif.DAT[23]	kpp.ROW[7]	csi.D[10]	weim.WEIM_EB[2]	gpt.CLKIN	gpio3.GPIO[11]	kitten.TRACE[23]	src.BT_CFG[31]
AUD_RXFS	audmux.AUD3_RXFS	i2c1.SCL	uart3.RXD_MUX	fec.MDIO	i2c3.SCL	gpio1.GPIO[0]	ecspi3.SS0	pl301_sim_mx6sl_per1.HPROT[1]
AUD_RXC	audmux.AUD3_RXC	i2c1.SDA	uart3.TXD_MUX	fec.TX_CLK	i2c3.SDA	gpio1.GPIO[1]	ecspi3.SS1	pl301_sim_mx6sl_per1.HREADYOUT
AUD_RXD	audmux.AUD3_RXD	ecspi3.MOSI	uart4.RXD_MUX	fec.RX_ER	usdhc1.LCTL	gpio1.GPIO[2]	src.INT_BOOT	pl301_sim_mx6sl_per1.HRESP
AUD_TXC	audmux.AUD3_TXC	ecspi3.MISO	uart4.TXD_MUX	fec.RX_DV	usdhc2.LCTL	gpio1.GPIO[3]	src.SYSTEM_RST	tpsmp.HDATA[24]
AUD_TXFS	audmux.AUD3_TXFS	pwm3.PWMO	uart4.RTS	fec.RDATA[1]	usdhc3.LCTL	gpio1.GPIO[4]	anatop.ANATOP_TESTI[0]	tpsmp.HDATA[25]
AUD_TXD	audmux.AUD3_TXD	ecspi3.SCLK	uart4.CTS	fec.TDATA[0]	usdhc4.LCTL	gpio1.GPIO[5]	anatop.ANATOP_TESTI[1]	tpsmp.HDATA[26]
AUD_MCLK	audmux.AUDIO_CLK_OUT	pwm4.PWMO	ecspi3.RDY	fec.MDC	wdog2.WDOG_RST_B_DEB	gpio1.GPIO[6]	spdif.SPDIF_EXT_CLK	tpsmp.HDATA[27]
UART1_RXD	uart1.RXD_MUX	pwm1.PWMO	uart4.RXD_MUX	fec.COL	uart5.RXD_MUX	gpio3.GPIO[16]	anatop.ANATOP_TESTI[2]	tpsmp.CLK
UART1_TXD	uart1.TXD_MUX	pwm2.PWMO	uart4.TXD_MUX	fec.RX_CLK	uart5.TXD_MUX	gpio3.GPIO[17]	anatop.ANATOP_TESTI[3]	uart5.DCD
I2C1_SCL	i2c1.SCL	uart1.RTS	ecspi3.SS2	fec.RDATA[0]	usdhc3.RST	gpio3.GPIO[12]	ecspi1.SS1	pl301_sim_mx6sl_per1.HSIZE[0]
I2C1_SDA	i2c1.SDA	uart1.CTS	ecspi3.SS3	fec.TX_EN	usdhc3.VSELECT	gpio3.GPIO[13]	ecspi1.SS2	pl301_sim_mx6sl_per1.HSIZE[1]
I2C2_SCL	i2c2.SCL	audmux.AUD4_RXFS	spdif.IN1	fec.TDATA[1]	usdhc3.WP	gpio3.GPIO[14]	ecspi1.RDY	pl301_sim_mx6sl_per1.HSIZE[2]
I2C2_SDA	i2c2.SDA	audmux.AUD4_RXC	spdif.OUT1	fec.REF_OUT	usdhc3.CD	gpio3.GPIO[15]	anatop.ANATOP_TESTO[0]	pl301_sim_mx6sl_per1.HWRITE
ECSPI1_SCLK	ecspi1.SCLK	audmux.AUD4_TXD	uart5.RXD_MUX	epdc.VCOM[0]	usdhc2.RST	gpio4.GPIO[8]	usb.USBOTG2_OC	tpsmp.HDATA[18]
ECSPI1_MOSI	ecspi1.MOSI	audmux.AUD4_TXC	uart5.TXD_MUX	epdc.VCOM[1]	usdhc2.VSELECT	gpio4.GPIO[9]	ccm.PLL2_BYP	tpsmp.HDATA[19]
ECSPI1_MISO	ecspi1.MISO	audmux.AUD4_TXFS	uart5.RTS	epdc.BDR[0]	usdhc2.WP	gpio4.GPIO[10]	ccm.PLL3_BYP	tpsmp.HDATA[20]
ECSPI1_SS0	ecspi1.SS0	audmux.AUD4_RXD	uart5.CTS	epdc.BDR[1]	usdhc2.CD	gpio4.GPIO[11]	usb.USBOTG2_PWR	pl301_sim_mx6sl_per1.HADDR[23]
ECSPI2_SCLK	ecspi2.SCLK	spdif.SPDIF_EXT_CLK	uart3.RXD_MUX	csi.PIXCLK	usdhc1.RST	gpio4.GPIO[12]	usb.USBOTG2_OC	tpsmp.HDATA[21]
ECSPI2_MOSI	ecspi2.MOSI	sdma.SDMA_EXT_EVENT[1]	uart3.TXD_MUX	csi.HSYNC	usdhc1.VSELECT	gpio4.GPIO[13]	anatop.ANATOP_TESTO[1]	tpsmp.HDATA[22]
ECSPI2_MISO	ecspi2.MISO	sdma.SDMA_EXT_EVENT[0]	uart3.RTS	csi.MCLK	usdhc1.WP	gpio4.GPIO[14]	usb.USBOTG1_OC	tpsmp.HDATA[23]
ECSPI2_SS0	ecspi2.SS0	ecspi1.SS3	uart3.CTS	csi.VSYNC	usdhc1.CD	gpio4.GPIO[15]	usb.USBOTG1_PWR	pl301_sim_mx6sl_per1.HADDR[24]
SD1_CLK	usdhc1.CLK	fec.MDIO	kpp.COL[0]	epdc.SDCE[4]	mshc.SCLK	gpio5.GPIO[15]	anatop.ANATOP_TESTO[2]	pl301_sim_mx6sl_per1.HADDR[25]
SD1_CMD	usdhc1.CMD	fec.TX_CLK	kpp.ROW[0]	epdc.SDCE[5]	mshc.BS	gpio5.GPIO[14]	anatop.ANATOP_TESTO[3]	pl301_sim_mx6sl_per1.HADDR[26]
SD1_DAT0	usdhc1.DAT0	fec.RX_ER	kpp.COL[1]	epdc.SDCE[6]	mshc.DATA[0]	gpio5.GPIO[11]	anatop.ANATOP_TESTO[4]	pl301_sim_mx6sl_per1.HADDR[27]
SD1_DAT1	usdhc1.DAT1	fec.RX_DV	kpp.ROW[1]	epdc.SDCE[7]	mshc.DATA[1]	gpio5.GPIO[8]	anatop.ANATOP_TESTO[5]	pl301_sim_mx6sl_per1.HADDR[28]
SD1_DAT2	usdhc1.DAT2	fec.RDATA[1]	kpp.COL[2]	epdc.SDCE[8]	mshc.DATA[2]	gpio5.GPIO[13]	anatop.ANATOP_TESTO[6]	pl301_sim_mx6sl_per1.HADDR[29]
SD1_DAT3	usdhc1.DAT3	fec.TDATA[0]	kpp.ROW[2]	epdc.SDCE[9]	mshc.DATA[3]	gpio5.GPIO[6]	anatop.ANATOP_TESTO[7]	pl301_sim_mx6sl_per1.HADDR[30]
SD1_DAT4	usdhc1.DAT4	fec.MDC	kpp.COL[3]	epdc.SDCLKN	uart4.RXD_MUX	gpio5.GPIO[12]	anatop.ANATOP_TESTO[8]	pl301_sim_mx6sl_per1.HADDR[31]
SD1_DAT5	usdhc1.DAT5	fec.RDATA[0]	kpp.ROW[3]	epdc.SDOED	uart4.TXD_MUX	gpio5.GPIO[9]	anatop.ANATOP_TESTO[9]	pl301_sim_mx6sl_per1.HPROT[3]
SD1_DAT6	usdhc1.DAT6	fec.TX_EN	kpp.COL[4]	epdc.SDOEZ	uart4.RTS	gpio5.GPIO[7]	anatop.ANATOP_TESTO[10]	pl301_sim_mx6sl_per1.HPROT[2]
SD1_DAT7	usdhc1.DAT7	fec.TDATA[1]	kpp.ROW[4]	ccm.PMIC_RDY	uart4.CTS	gpio5.GPIO[10]	anatop.ANATOP_TESTO[11]	pl301_sim_mx6sl_per1.HMASTLOCK
SD2_RST	usdhc2.RST	fec.REF_OUT	wdog2.WDOG_B	spdif.OUT1	csi.MCLK	gpio4.GPIO[27]	anatop.ANATOP_TESTO[12]	pl301_sim_mx6sl_per1.HBURST[2]
SD2_CLK	usdhc2.CLK	audmux.AUD4_RXFS	ecspi3.SCLK	csi.D[0]	osc32k.32K_OUT	gpio5.GPIO[5]	anatop.ANATOP_TESTO[13]	pl301_sim_mx6sl_per1.HPROT[1]
SD2_CMD	usdhc2.CMD	audmux.AUD4_RXC	ecspi3.SS0	csi.D[1]	epit1.EPITO	gpio5.GPIO[4]	anatop.ANATOP_TESTO[14]	pl301_sim_mx6sl_per1.HADDR[21]
SD2_DAT0	usdhc2.DAT0	audmux.AUD4_RXD	ecspi3.MOSI	csi.D[2]	uart5.RTS	gpio5.GPIO[1]	anatop.ANATOP_TESTO[15]	pl301_sim_mx6sl_per1.HPROT[0]
SD2_DAT1	usdhc2.DAT1	audmux.AUD4_TXC	ecspi3.MISO	csi.D[3]	uart5.CTS	gpio4.GPIO[30]	mmdc.MMDC_DEBUG[39]	pl301_sim_mx6sl_per1.HBURST[1]
SD2_DAT2	usdhc2.DAT2	audmux.AUD4_TXFS	fec.COL	csi.D[4]	uart5.RXD_MUX	gpio5.GPIO[3]	mmdc.MMDC_DEBUG[38]	pl301_sim_mx6sl_per1.HADDR[22]
SD2_DAT3	usdhc2.DAT3	audmux.AUD4_TXD	fec.RX_CLK	csi.D[5]	uart5.TXD_MUX	gpio4.GPIO[28]	mmdc.MMDC_DEBUG[37]	pl301_sim_mx6sl_per1.HBURST[0]
SD2_DAT4	usdhc2.DAT4	usdhc3.DAT4	uart2.RXD_MUX	csi.D[6]	spdif.OUT1	gpio5.GPIO[2]	mmdc.MMDC_DEBUG[36]	pl301_sim_mx6sl_per1.HADDR[10]
SD2_DAT5	usdhc2.DAT5	usdhc3.DAT5	uart2.TXD_MUX	csi.D[7]	spdif.IN1	gpio4.GPIO[31]	mmdc.MMDC_DEBUG[35]	pl301_sim_mx6sl_per1.HADDR[20]
SD2_DAT6	usdhc2.DAT6	usdhc3.DAT6	uart2.RTS	csi.D[8]	usdhc2.WP	gpio4.GPIO[29]	mmdc.MMDC_DEBUG[34]	pl301_sim_mx6sl_per1.HADDR[19]
SD2_DAT7	usdhc2.DAT7	usdhc3.DAT7	uart2.CTS	csi.D[9]	usdhc2.CD	gpio5.GPIO[0]	mmdc.MMDC_DEBUG[33]	pl301_sim_mx6sl_per1.HADDR[16]
SD3_CLK	usdhc3.CLK	audmux.AUD5_RXFS	kpp.COL[5]	csi.D[10]	wdog1.WDOG_RST_B_DEB	gpio5.GPIO[18]	usb.USBOTG1_PWR	pl301_sim_mx6sl_per1.HADDR[13]
SD3_CMD	usdhc3.CMD	audmux.AUD5_RXC	kpp.ROW[5]	csi.D[11]	anatop.USBOTG2_ID	gpio5.GPIO[21]	usb.USBOTG2_PWR	pl301_sim_mx6sl_per1.HADDR[18]
SD3_DAT0	usdhc3.DAT0	audmux.AUD5_RXD	kpp.COL[6]	csi.D[12]	anatop.USBOTG1_ID	gpio5.GPIO[19]	sjc.JTAG_ACT	pl301_sim_mx6sl_per1.HADDR[11]
SD3_DAT1	usdhc3.DAT1	audmux.AUD5_TXC	kpp.ROW[6]	csi.D[13]	usdhc1.VSELECT	gpio5.GPIO[20]	sjc.DE_B	pl301_sim_mx6sl_per1.HADDR[17]
SD3_DAT2	usdhc3.DAT2	audmux.AUD5_TXFS	kpp.COL[7]	csi.D[14]	epit1.EPITO	gpio5.GPIO[16]	usb.USBOTG2_OC	pl301_sim_mx6sl_per1.HADDR[14]
SD3_DAT3	usdhc3.DAT3	audmux.AUD5_TXD	kpp.ROW[7]	csi.D[15]	epit2.EPITO	gpio5.GPIO[17]	usb.USBOTG1_OC	pl301_sim_mx6sl_per1.HADDR[12]
FEC_MDIO	fec.MDIO	usdhc4.CLK	audmux.AUD6_RXFS	ecspi4.SS0	gpt.CAPIN1	gpio4.GPIO[20]	kitten.TRACE[26]	pl301_sim_mx6sl_per1.HADDR[15]
FEC_TX_CLK	fec.TX_CLK	usdhc4.CMD	audmux.AUD6_RXC	ecspi4.SCLK	gpt.CAPIN2	gpio4.GPIO[21]	kitten.TRACE[27]	pl301_sim_mx6sl_per1.HADDR[4]
FEC_RX_ER	fec.RX_ER	usdhc4.DAT0	audmux.AUD6_RXD	ecspi4.MOSI	gpt.CMPOUT1	gpio4.GPIO[19]	kitten.TRACE[25]	pl301_sim_mx6sl_per1.HADDR[5]
FEC_CRS_DV	fec.RX_DV	usdhc4.DAT1	audmux.AUD6_TXC	ecspi4.MISO	gpt.CMPOUT2	gpio4.GPIO[25]	kitten.TRACE[31]	pl301_sim_mx6sl_per1.HADDR[3]
FEC_RXD1	fec.RDATA[1]	usdhc4.DAT2	audmux.AUD6_TXFS	ecspi4.SS1	gpt.CMPOUT3	gpio4.GPIO[18]	fec.COL	pl301_sim_mx6sl_per1.HADDR[9]
FEC_TXD0	fec.TDATA[0]	usdhc4.DAT3	audmux.AUD6_TXD	ecspi4.SS2	gpt.CLKIN	gpio4.GPIO[24]	kitten.TRACE[30]	pl301_sim_mx6sl_per1.HADDR[2]
FEC_MDC	fec.MDC	usdhc4.DAT4	audmux.AUDIO_CLK_OUT	usdhc1.RST	usdhc3.RST	gpio4.GPIO[23]	kitten.TRACE[29]	pl301_sim_mx6sl_per1.HADDR[8]
FEC_RXD0	fec.RDATA[0]	usdhc4.DAT5	anatop.USBOTG1_ID	usdhc1.VSELECT	usdhc3.VSELECT	gpio4.GPIO[17]	kitten.TRACE[24]	pl301_sim_mx6sl_per1.HADDR[7]
FEC_TX_EN	fec.TX_EN	usdhc4.DAT6	spdif.IN1	usdhc1.WP	usdhc3.WP	gpio4.GPIO[22]	kitten.TRACE[28]	pl301_sim_mx6sl_per1.HADDR[1]
FEC_TXD1	fec.TDATA[1]	usdhc4.DAT7	spdif.OUT1	usdhc1.CD	usdhc3.CD	gpio4.GPIO[16]	fec.RX_CLK	pl301_sim_mx6sl_per1.HADDR[6]
FEC_REF_CLK	fec.REF_OUT	usdhc4.RST	wdog1.WDOG_B	pwm4.PWMO	ccm.PMIC_RDY	gpio4.GPIO[26]	spdif.SPDIF_EXT_CLK	pl301_sim_mx6sl_per1.HADDR[0]